Experimental Evidence for Voltage Driven Breakdown Models in Ultrathin Gate Oxides

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ABSTRACT

We have performed an experiment proving that the widely accepted E-field TDDB model is a **physically incorrect** description of breakdown in ultrathin gate oxides. Although interface traps are the dominant SILC mechanism below 5 V stress, breakdown remains limited by bulk trap generation and is voltage-driven. It has been recently proposed that the anode hole injection model is still operative at low voltages. Although we will show that holes do generate bulk traps and cause breakdown in ultrathin oxides, hole injection does not completely account for all of the trap generation mechanisms observed during direct tunneling stress.

INTRODUCTION

Historically, a controversy regarding the use of the E-model [1,2] vs. the 1/E model [3] for the analysis of TDDB data has raged on in the literature. Both models have a range of voltage and thickness where they have been shown to be empirically valid [4,5]. It is generally accepted that the 1/E model, which results in the most optimistic projections, is appropriate only at high voltages in thick oxides. Accordingly, the E-field model is now widely utilized for oxide lifetime projections in state of the art technologies.

One of difficulties with the E-field model is that it does not explain the polarity dependence of the charge to breakdown (QBD) in ultrathin oxides [6], where devices stressed at the same field have higher QBD for $+V_G$ compared to $-V_G$. The generation rate of traps that cause stress-induced-leakage-current (SILC) shows a similar polarity gap [7]. It was subsequently shown that the SILC generation rate is determined by voltage rather than by field. Plotted against voltage, the polarity gap in the SILC generation rate disappears [8]. Since QBD is determined by the SILC generation rate, QBD is also controlled by voltage rather than field [8]. This is the origin of voltage driven models, where the breakdown process is controlled by electrons that dissipate the maximum energy at the anode. In contrast, field driven models are operative when electrons gain enough energy from the field during F-N tunneling so that the average energy dissipated at the anode is sufficient to cause trap generation and breakdown. Voltage-driven breakdown also accounts for the polarity gap in nMOS TDDB data [9].

The trap states generated during stress that cause SILC also result in dielectric breakdown [8]. Accordingly, since reliability projections can be obtained from SILC data [10], the information contained in SILC measurements is of considerable interest. SILC is due to trap-assisted tunneling through bulk trap states [7,11]. As the energy threshold for bulk trap generation is about 5 V [7], SILC effects are greatly diminished at lower stress voltages. However, interface trap generation remains significant, and tunneling via interfacial traps becomes the dominant SILC mechanism below 5 V stress [12]. This raises the question as to whether it is bulk or interface traps that control breakdown in ultrathin oxides.

Although the E-model vs. 1/E model issue appears to be largely resolved, another controversy has emerged. While it is generally accepted that degradation mechanisms are activated through the absorption of the energy of hot electrons entering the anode material, two different models have been proposed. One camp claims that the precursor to breakdown is anode hydrogen release (AHR) [7,13], where the migration of a hydrogen species into the oxide results in the generation of bulk traps and interface states. The other camp claims that trap generation and breakdown are due to anode hole injection (AHI) [14,15] into the gate oxide. Both AHR and AHI models predict voltage driven breakdown at low operating voltages.

In this work, we will briefly review transport, degradation mechanisms, and the energy concepts needed to understand breakdown in ultrathin oxides. Although the field and voltage models result in similar lifetime projections [16], we will prove that the E-field model is a physically incorrect description of breakdown in ultrathin gate oxides. Although interface traps are the dominant SILC mechanism below 5 V stress, we will show that breakdown remains limited by bulk trap generation. We then proceed to examine whether gate voltage driven breakdown is a consequence of anode hole injection or anode hydrogen release. We obtain a measurable hole current in our experiments to superimpose on the "nominal" trap evolution process. Although holes are indeed shown to result in bulk trap creation and breakdown at low voltages in ultrathin oxides, the AHI model does not completely account for all of the trap generation mechanisms observed during stress.

Transport Mechanisms

There are three electrode limited thermal tunneling processes that are encountered in virgin, thermally grown

device grade SiO_2. The operative tunneling mechanism is determined by the film thickness and the voltage drop across the oxide. For oxide voltage (V_{OX}) less than the 3 V Si-SiO_2 barrier height, electrons tunnel through a trapezoidal barrier directly from the cathode to the anode, without appearing in the oxide conduction band, as shown in Figure 1. The direct tunneling process is ballistic, since electrons are not scattered until after they enter the anode. The average kinetic energy $<KE_{Si}>$ of electrons entering the anode (prior to any scattering process in the anode) is equal to qV_{OX}, and the maximum anode energy delivered to the anode is qV_G.

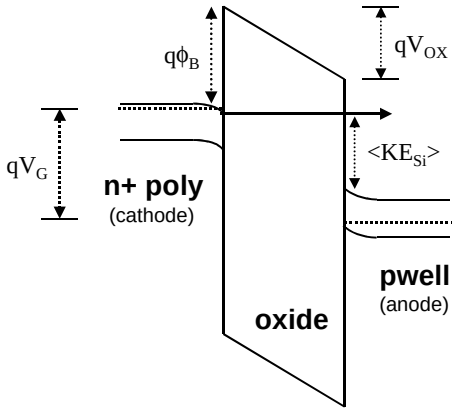

Figure 1. Ballistic Direct Tunneling. The dashed horizontal lines in the poly and pwell denote the respective Fermi levels.

For oxide voltages greater than 3 V, electrons undergo Fowler-Nordheim (FN) tunneling from the cathode conduction band to the oxide conduction band through a triangular barrier. The electrons move in the oxide conduction band and gain kinetic energy from the field as they traverse the dielectric. FN tunneling can be either ballistic or steady-state, depending on the oxide voltage and thickness. For oxides below 5.0 nm thickness, transport is ballistic until the oxide voltage exceeds 9 V, although the transition from ballistic to steady state transport occurs at much lower energies in thick oxides [17]. Ballistic FN tunneling is illustrated in Figure 2.

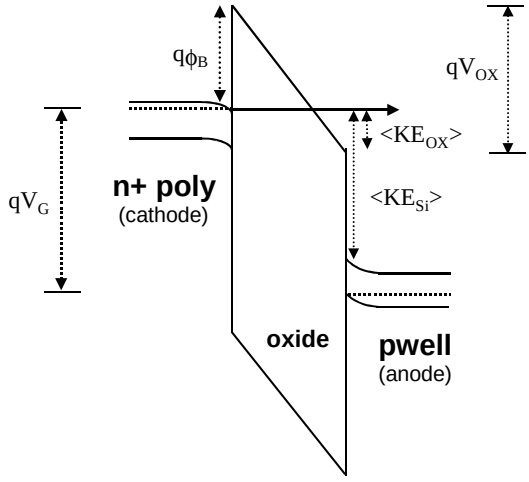

Figure 2. Ballistic Fowler-Nordheim Tunneling.

The average kinetic energy $<KE_{Si}>$ of electrons entering the anode is qV_{OX}, and is equal to the sum of the barrier height $q\phi_B$ and the average kinetic energy in the oxide $<KE_{OX}>$ at the anode interface. The maximum energy delivered to the anode is qV_G.

For oxide voltages that exceed 6 V, electron scattering with oxide phonons results in steady-state FN transport. Unlike direct and FN tunneling, $<KE_{Si}>$ will be less than qV_{OX}. Since this process is unimportant in ultrathin oxides, it will not be discussed further. The energies corresponding to these transport mechanisms are summarized in Table 1.

Table 1 - Tunneling Energies in Ultrathin Oxides.

Tunneling	qVox	<KEox>
	[eV]	[eV]
Direct	< 3	0
Ballistic FN	3 - 9	0 - 6
Steady-State FN	> 9	> 6

Trap Generation Mechanisms

Three processes have been identified that lead to trap generation and oxide breakdown: Impact ionization in the oxide, anode hole injection, and anode hydrogen release. Impact ionization in the oxide is insignificant in ultrathin oxides because it only occurs when carriers have been heated to kinetic energies exceeding the 9 eV SiO_2 bandgap during steady-state FN tunneling [17,18].

According to the original anode hole injection model [14], anode hole injection can occur when the oxide voltage exceeds about 6 V. In this process, an electron enters the anode, an electron-hole pair is created from impact ionization, and the hole is injected back into the oxide. The hole results in the generation of bulk and interface traps. The experimental evidence for this model is the constant hole flux to breakdown, independent of stress condition [14]. The two difficulties with the AHI model are explaining damage at low voltages, and the polarity gap. Recently, a model invoking minority carrier ionization has been proposed to correct these deficiencies [15].

Anode hydrogen release occurs when the oxide kinetic energy exceeds 2 eV, corresponding to a minimum oxide voltage of 5 V. The release of hydrogen into the oxide is believed to result in the generation of traps. The experimental findings supporting this model are the 5 V threshold common for both interface trap generation and hydrogen transport in oxide [19]. Also, exposing oxide to a hydrogen plasma results in a SILC increase similar to that observed during voltage stress [7]. The energy thresholds for trap generation mechanisms are summarized in Table 2. Note the similarities between AHI and AHR thresholds.

Table 2 – Threshold Energies for Trap Generation.

Mechanism	qVox	<KEox>
	[eV]	[eV]
Oxide Impact Ionization	>> 12	> 9
Anode Hole Injection	> 6	> 3
Anode Hydrogen Release	> 5	> 2

It would seem that there is insufficient energy for trap generation for either AHR or AHI below 5 V stress. However, trap generation has been observed down to gate voltages as low as 2 V [10], indicating that degradation of the oxide layer occurs well below the generation threshold energies. When the oxide voltage is greater than the energy thresholds shown in Table 2, the average kinetic energy of electrons entering the anode is sufficient to readily generate trap states. At voltages below threshold, electrons that dissipate the maximum energy at the anode will control trap generation rates [8].

EXPERIMENT

Constant voltage $+V_G$ stress is performed at room temperature on nMOS and pMOS devices fabricated using a dual poly cMOS process. The stress is periodically interrupted to perform an I-V sweep. The gate oxides are 2.0 nm – 3.0 nm thick SiO_2 films thermally grown in an O_2 ambient. Oxide areas are on the order of 10^{-5} cm^2 to 10^{-3} cm^2. Both capacitors and gate controlled diode structures were utilized. The gated diodes are used to perform carrier separation measurements. Band bending and electric field are obtained from quantum C-V device simulations [20]. Failure is determined from the first detected breakdown event (soft or hard).

RESULTS

E-field Model vs. Voltage Model

TDDB data for 2.7 nm nMOS and pMOS oxides are shown using the E-field model in Figure 3. The t50%'s are computed from 25 devices per stress condition using Weibull statistics. At a given field, the nMOS time to breakdown is much longer compared to pMOS. These data are re-plotted using the voltage model in Figure 4. The nMOS/pMOS "polarity gap" has been eliminated, as the time to failure is the same for both nMOS and pMOS devices at the same gate voltage, in agreement with the voltage model. Band diagrams for nMOS and pMOS at the same electric field are shown in Figure 5. The average anode energy is the same, but the maximum energy delivered to the anode is higher for pMOS.

It can be seen that the data fit a straight line in both Figures 3 and 4. Linearity is not a clear indicator of which lifetime model is physically correct. Straight lines result in both Figures 3 and 4 because of the linear relationship between V_{OX} and V_G in the region of interest [16]. However, inspection of Figures 3-5 suggests that the E-field and voltage models cannot both be physically correct.

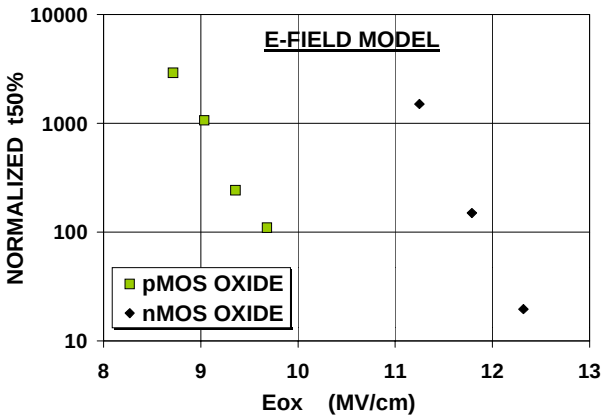

Figure 3. E-field model for 2.7 nm nMOS and pMOS oxides. At a given field, t50% is much larger for nMOS.

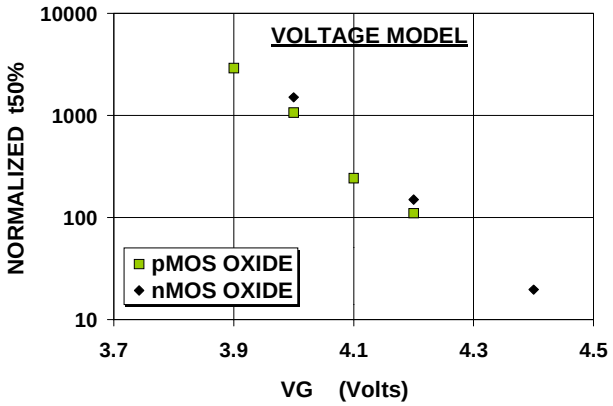

Figure 4. Voltage model for 2.7 nm nMOS and pMOS oxides. nMOS and pMOS t50% are the same at the same V_G.

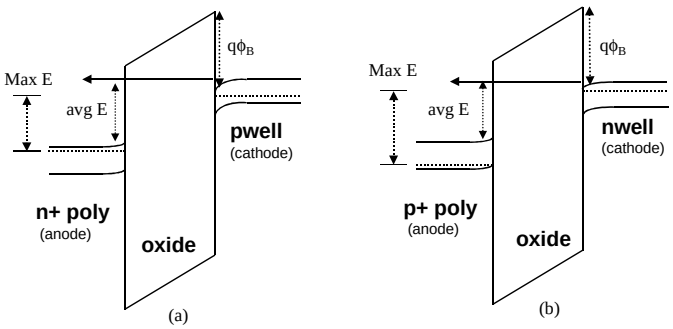

Figure 5. Band diagrams for (a) nMOS and (b) pMOS at the same oxide field. The average energy delivered to the anode is the same, but the maximum energy dissipated at the anode is higher for pMOS.

To resolve this issue, 2.6 nm nMOS oxides were fabricated with poly doping splits. The variations in poly doping allow the oxide field to be varied under stress at a fixed gate voltage and oxide thickness. Due to poly depletion, the oxide electric field can be modulated by 2.5 MV/cm under a fixed $+V_G$ stress condition over the space of this experiment, as shown in Figure 6. The E-field model predicts that the time to fail

will increase as the poly doping is reduced, while the voltage model predicts doping independent lifetime. The results of constant voltage direct tunneling stress at +3.6 V are shown in Figure 7. All data are normalized to the highest poly doping split. The lifetime is nearly independent of poly doping, whereas the E-field model predicts a 20,000X change. This proves that breakdown is NOT field-driven. Series resistance effects were verified to be insignificant by comparing the measured gate currents with direct tunneling fits, using the method in [14]. In all cases, the gate current was equal to or slightly greater than the expected value during stress.

Gate current varies more slowly with field for direct tunneling compared to F-N tunneling. It was previously shown that QBD is voltage driven [8]. In our experiment, both TDDB and QBD are voltage driven, since the stress current only varies by a factor of 4X between the lowest and highest poly doping splits.

The ramped breakdown voltage distributions for these devices are shown in Figure 8. The breakdown voltage is also independent of poly doping. This is also in contradiction to the E-field model, which predicts a 1 volt excursion in median breakdown voltage over the space of this experiment.

We have shown that the E-field model is a physically incorrect description of breakdown in ultrathin oxides. We will investigate the mechanisms that lead to this behavior in the following sections.

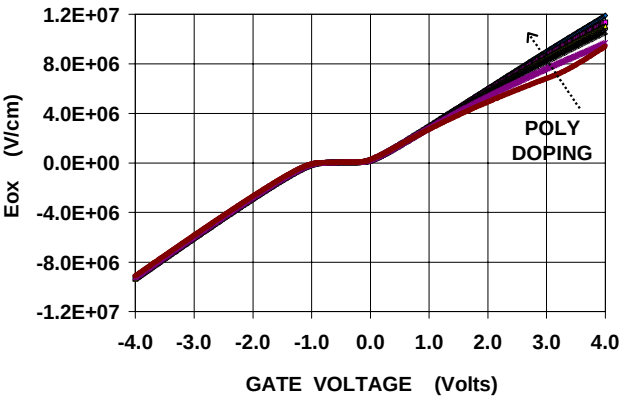

Figure 6. Oxide electric field vs. gate voltage as a function of poly doping. Due to poly depletion, the oxide field can be modulated by 2.5 MV/cm at a fixed $+V_G$.

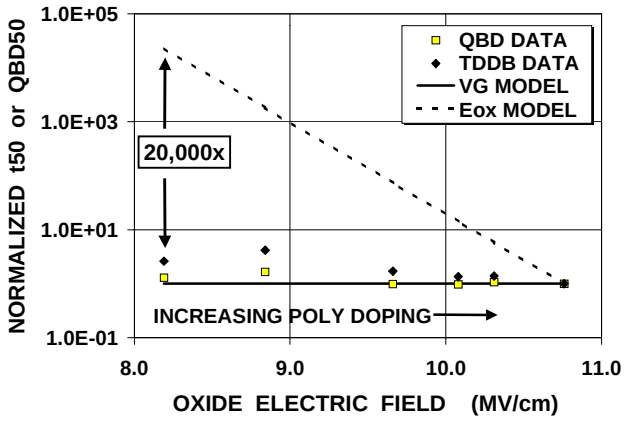

Figure 7. E-field and voltage models for 2.6 nm nMOS oxides stressed at +3.6 V. Breakdown is NOT field driven at this oxide thickness.

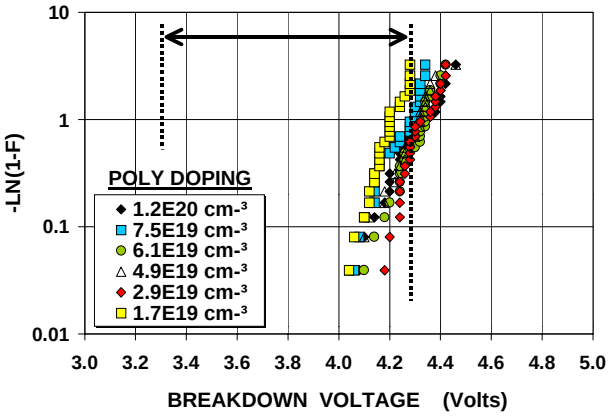

Figure 8. Effect of poly doping on 2.6 nm nMOS oxide breakdown voltage. The arrow demarcates the variation in mean breakdown voltage predicted by the E-field model.

Stress-Induced-Leakage-Current

We will use SILC measurements to analyze the evolution of bulk and interface traps generated during stress. Since the trap states that cause SILC also result in dielectric breakdown [8], the information contained in SILC measurements is of considerable interest.

We begin by reviewing the method for separating the effects of interface and bulk traps. The SILC increase resulting from trap assisted tunneling through bulk traps is independent of sense voltage [7], while the SILC increase resulting from tunneling via interface states (LV-SILC) is strongly dependent on sense voltage. LV-SILC is detected only at sense voltages within +/-1 V of VFB [12], because tunneling via interface states is only energetically possible when trap states in the anode and cathode are at similar electrostatic potentials. Accordingly, the interface and bulk trap SILC components can be resolved by sensing in the off-state near VFB and in the on-state, respectively [12].

It has been shown that interface traps are the dominant SILC mechanism below 5 V stress [12]. To further illustrate this point, the generation rates for bulk and interface traps,

extracted from SILC and LV-SILC measurements respectively, are shown for 2.8 nm nMOS devices in Figure 9. The generation rate P_{gen} is obtained using $P_{gen} = N_{bd}/Qbd$ [10], where N_{bd} is the critical density of traps at breakdown determined from the normalized SILC increase (dJ/J_o). The threshold energy for trap generation is about 0.5 V lower for interface states. At a given stress voltage, the interface state generation rate is more than 100X greater than the bulk trap generation rate. It can be seen that interface traps are much more readily generated than bulk traps below 5 V stress.

Figure 10 shows that the critical density of bulk traps at breakdown, extracted from SILC measurements, is the same for 2.7 nm nMOS and pMOS oxides. Similarly, the critical density of interface traps at breakdown, extracted from LV-SILC measurements, is also the same for nMOS and pMOS. Although interface trap generation rates are higher, it is not clear as to whether voltage driven breakdown is controlled by bulk or interface traps. We will resolve this issue with anode hole injection studies.

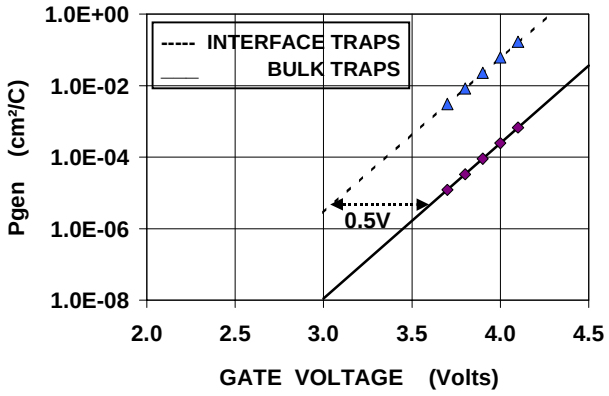

Figure 9. SILC (bulk trap) and LV-SILC (interface trap) generation rates in 2.8 nm nMOS oxides. Generation rates are higher for interface traps.

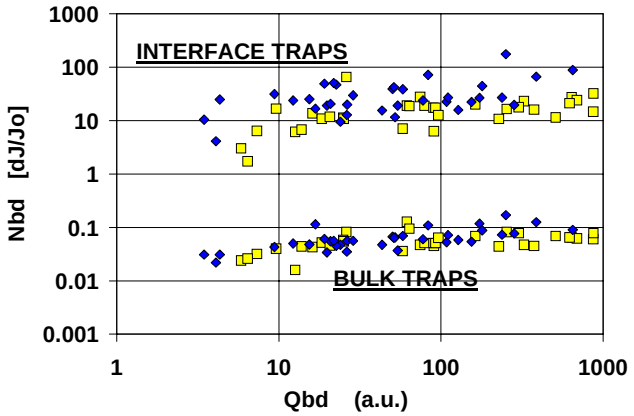

Figure 10. Critical density of interface traps and bulk traps at breakdown in 2.7 nm nMOS (light fill) and pMOS (dark fill) oxides.

Anode Hole Injection Mechanisms

In this section, we will demonstrate a measurable hole current during direct tunneling stress. The "conventional" anode hole injection mechanism [14,15] is illustrated for a 2.6 nm nMOS oxide at a gate voltage of 4 V in Figure 11. In this process, electrons with energy V_{OX} arrive at the anode and create a hole through impact ionization. The hole energy is $qV_{OX} - 1.1$ eV, where the energy to create an electron-hole pair through impact ionization is 1.1 eV. Under the specified conditions, the hole kinetic energy will only be about 1.3 eV, which is small compared to the 4.7 eV hole barrier at the poly-SiO_2 interface. Therefore, probability of injecting this hole into the oxide is small, making this process unfeasible for AHI studies. As this process is not dependent on the anode Fermi level, it does not account for the polarity gap [15], and therefore is not a mechanism for voltage driven breakdown.

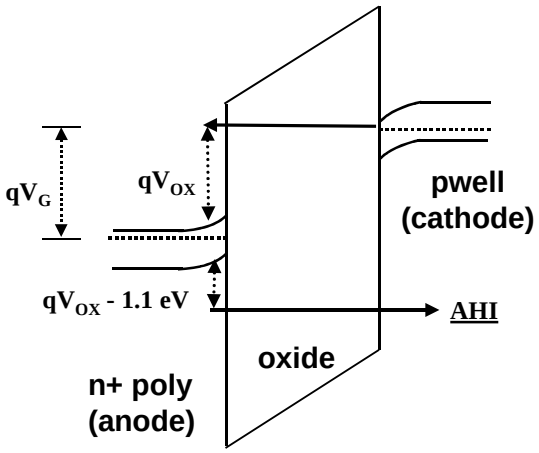

Figure 11. Conventional anode hole injection process in nMOS device with 2.6 nm oxide thickness. The hole energy with respect to the valence band edge is $qV_{OX} - 1.1$ eV. From Bude et al [15].

We will now expand our experimental space to include nMOS devices with poly doping sufficiently low enough to invert under stress conditions. Since the poly is degenerately doped, the surface potential required to invert the poly is approximately equal to the bandgap. Accordingly, inversion layer holes can be sourced by both band-to-band tunneling and thermal generation. Using the principles presented in [15], where electrons transfer their energy directly to an free hole in the anode valence band, we will use these devices to obtain a readily measurable hole current by increasing the supply of both hot and thermal holes in the poly anode.

Three-terminal gate controlled diodes are used to perform carrier separation measurements during a gate voltage sweep. Using quantum C-V simulations [20], the band bending in the substrate and poly are known as a function of gate voltage. Substrate current vs. poly band bending for 2.6 nm nMOS oxides is shown in Figure 12. For the lighter doped poly splits, the current in the **substrate** sharply increases when the band bending in the **poly** exceeds the bandgap and the poly inverts. This indicates that the origin of the substrate current may be hole injection from the poly anode. The oxide voltage does not exceed 2.8 eV for any of the devices shown in

Figure 12. The increase in substrate current shown in Figure 12 is not due to the "conventional" anode hole injection process illustrated in Figure 11, as the measured current is several orders of magnitude too large.

Valence band electron tunneling, generation/recombination (G-R) processes, and trap assisted tunneling are well-known mechanisms for substrate current [17]. The substrate current in our highest doped poly devices is indeed dominated by valence band electron tunneling. G-R can be ruled out as the primary origin of the additional substrate current component in the lightly doped poly devices, as its appearance coincides with inversion of the poly. It has also been proposed that photogeneration of an electron-hole pair in the substrate by a photon originating in the poly anode after absorbing a hot electron is a significant source of substrate current [17,21]. Although this effect, along with the other mechanisms discussed above may occur in our devices, we will subsequently show that anode hole injection must also be present to explain our results.

We will consider anode hole injection processes that are dependent on the Fermi level position in the poly anode. We will include mechanisms that require only a single electron-hole interaction, since processes requiring multiple scattering events are less probable. The four anode hole injection mechanisms that are possible in the presence of free holes at the poly-SiO_2 interface that meet these constraints are shown in Figures 13 and 14 for V_G = 4 V. In the processes illustrated in Figure 13, an electron injected from the cathode transfers energy (a) qV_{OX} or (b) qV_G to a *thermal hole* in the poly inversion layer, which subsequently tunnels through the barrier. For this process, the maximum hole energy with respect to the valence band is (a) $qV_{OX} + |E_F - E_V|$, or: (b) $qV_G + |E_F - E_V|$. In Figure 14, a thermally generated hole injected from the poly bulk towards the interface acquires a maximum energy of $|E_F - E_V| + 1.1$ eV. An electron injected from the cathode transfers energy (a) qV_{OX} or (b) qV_G to this *hot hole*. The hot hole can have sufficient energy to be injected over the barrier. For the processes illustrated in Figure 14, the maximum hole energy with respect to the valence band is: (a) $qV_{OX} + 2|E_F - E_V| + 1.1$ eV, or: (b) $qV_G + 2|E_F - E_V| + 1.1$ eV. In the next section, we will perform anode hole injection studies to gain insight into oxide breakdown mechanisms.

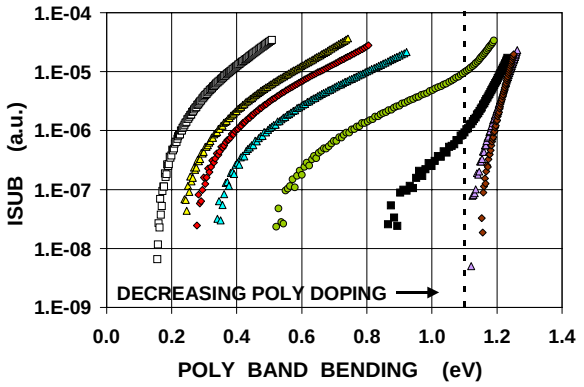

Figure 12. Substrate current vs. poly band-bending. The substrate current sharply increases after the poly inverts.

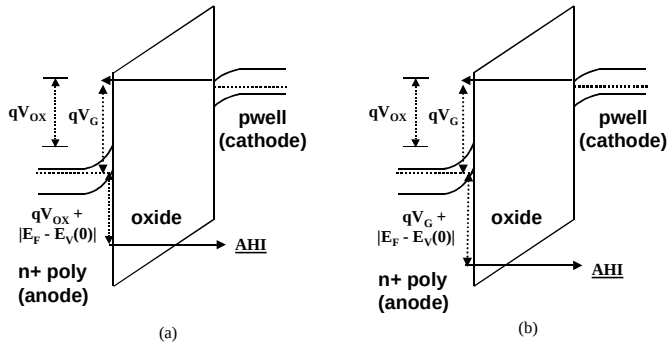

Figure 13. Band diagram for possible anode hole emission mechanisms. An electron injected from the cathode transfers energy (a) qV_{OX} or (b) qV_G to a *thermal hole* in the anode, which subsequently tunnels through the barrier. From Bude et al [15].

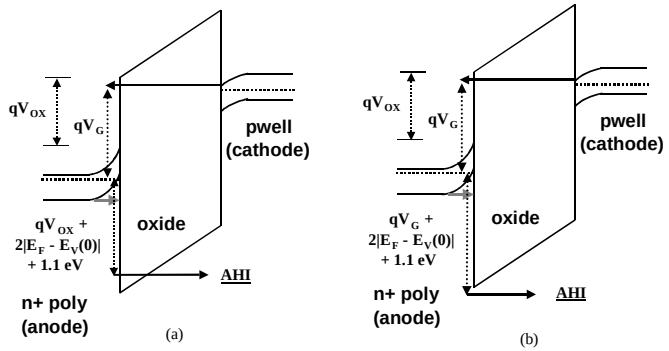

Figure 14. Band diagram for possible anode hole emission mechanisms. An electron injected from the cathode transfers energy (a) qV_{OX} or (b) qV_G to a *hot hole* in the anode, which subsequently tunnels through (or is emitted over) the barrier. From Bude et al [15].

Breakdown Mechanisms

In thick oxides, interface traps are created when holes are injected. One mechanism is the formation of "slow" states due to trapped holes [22]. However, this effect is unimportant in our devices, as C-V measurements showed no increase in positive charge trapping when AHI is significant. Another mechanism for interface trap generation is the energy release resulting from the recombination of an electron-hole pair in the oxide [23]. Although it was also proposed that bulk neutral traps could be generated through this process, it has been shown that only holes are required to create neutral traps [24]. In the voltage range utilized in our experiment, electron transport is through direct tunneling only. Therefore, interface trap generation from electron-hole recombination is also expected to be insignificant during anode hole injection since there are no electrons in the oxide conduction band. Since neutral trap generation only requires holes, anode hole injection can be used to preferentially generate bulk traps in ultrathin oxides. We will superimpose a hole current on the "nominal" trap evolution process, where both bulk and interface traps are generated. This experiment will reveal whether it is bulk or interface traps that control voltage driven

breakdown under direct tunneling stress. Also, it will allow us to examine whether the anode hole injection model is a plausible explanation for breakdown in ultrathin gate oxides.

Using the devices with poly doping splits, QBD vs. poly band bending is shown for +3.6V stress in Figure 15. The charge to breakdown drops sharply after the poly inverts and anode hole injection becomes a significant mechanism. The SILC increase due to bulk traps and the LV-SILC increase due to interface traps are shown vs. poly band bending in Figure 16. It can be seen that the bulk trap generation rate increases under AHI, while the interface trap generation rate is unchanged. Similar results were also obtained from high-frequency C-V stretchout (not shown). Therefore, we have verified that only holes are required to generate bulk traps, and as predicted, anode hole injection does not affect interface trap generation rates during direct tunneling stress.

Other workers have observed that dielectric breakdown occurs after a critical density of defects have been created [10]. However, it has not been shown unambiguously whether the defects controlling breakdown are bulk or interface traps. The effective number of bulk and interface traps at breakdown, determined from the normalized SILC increase, are shown in Figure 17. Breakdown occurs once a critical density of bulk traps is attained, independent of interface trap density. Although interface traps are the dominant SILC mechanism below 5 V stress, Figures 15-17 show unequivocally that breakdown is controlled by bulk traps.

The AHI model is indeed a possible explanation for voltage driven breakdown. However, since hole injection does not generate interface traps, another mechanism such as AHR must also be operative to account for all of the degradation observed during stress.

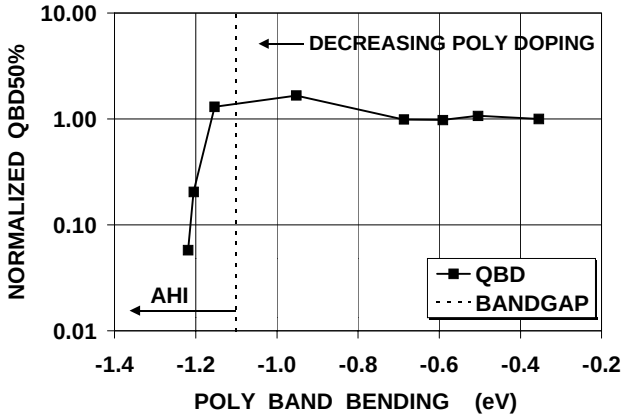

Figure 15. Q_{BD} vs. poly band bending for +3.6V stress. Q_{BD} decreases sharply after the poly inverts and AHI becomes significant.

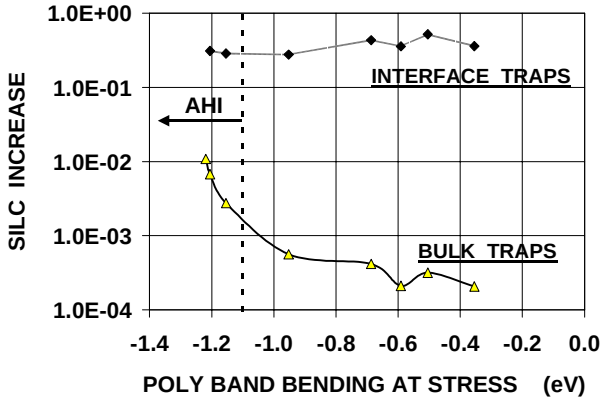

Figure 16. SILC increase after 1 C/cm^2 fluence at +3.6V stress. AHI increases the bulk trap generation rate.

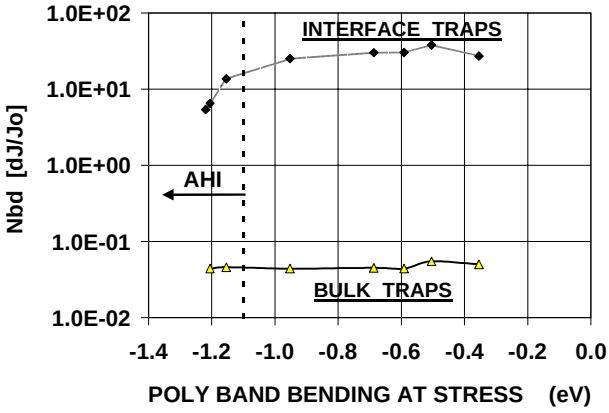

Figure 17. Effective number of defects at breakdown determined from normalized SILC increase. Breakdown occurs when a critical bulk trap density is reached.

DISCUSSION

When calculating maximum safe operating conditions, E-field and voltage models yield comparable results [16]. However, we have shown that the E-field model is a physically incorrect description of ultrathin oxide breakdown. Reliability projections should be performed with the voltage model. Breakdown models are often differentiated as voltage/fluence vs. field/time. We have shown that the primary distinction is the choice of voltage over field. In the voltage model, similar trends are observed for both fluence and time in the direct tunneling regime.

The voltage model provides the framework for understanding breakdown mechanisms under direct tunneling stress. When the voltage is sufficiently low so that the average electron energy dissipated in the anode is insufficient to generate traps, breakdown becomes voltage driven. In this regime, the electrons that dissipate the maximum energy at the anode, which is qVG for thermal carriers, control trap generation.

Interface traps are the dominant SILC mechanism below 5 V stress because the interface traps have a higher generation rate than bulk traps. To determine whether bulk or interface

traps control breakdown, we used anode hole injection to preferentially generate bulk traps over interface states during direct tunneling stress. This showed that breakdown is controlled by bulk traps over the thickness and voltage range investigated in this study. It is possible that the relative importance of interface and bulk traps in the breakdown process could change as oxide thickness is scaled.

Photogeneration of an electron-hole pair in the substrate by a photon originating in the poly anode may be a significant source of substrate current [21]. However, if photogeneration were the sole source of the substrate current, then it would not have been possible to separately generate bulk traps. The increased bulk trap generation rate would have been due to the injection of the photogenerated electron back to the anode, which would have also resulted in an increased interface trap generation rate, but was not observed in our experiment.

Valence band tunneling occurs when an electron in the pwell valence band tunnels into the poly conduction band, leaving behind a free hole in the pwell that results in substrate current. This process may also be trap assisted, as shown in Figure 18 for an inelastic tunneling event [25,26]. When the poly inverts and the poly valence band edge moves above the poly Fermi level, an additional transport path is created. In this event, tunneling from the pwell valence band to poly valence band via trap assisted tunneling through bulk oxide traps can result in an additional substrate current component. However, this process only occurs if the electron emitted from the bulk trap is at an electrostatic potential within the poly band gap when it arrives at the anode. Therefore, since this process can only deliver a maximum energy of 1.1 eV to the anode, this mechanism does not explain the increase in trap generation rates that are observed when the poly inverts.

Having ruled out other mechanisms, we have demonstrated that holes injected from the anode do indeed cause breakdown in ultrathin oxides. The AHI model provides a credible explanation for voltage-driven breakdown. However, hole injection does not generate interface traps during direct tunneling stress, so another mechanism such as anode hydrogen release must also be operative.

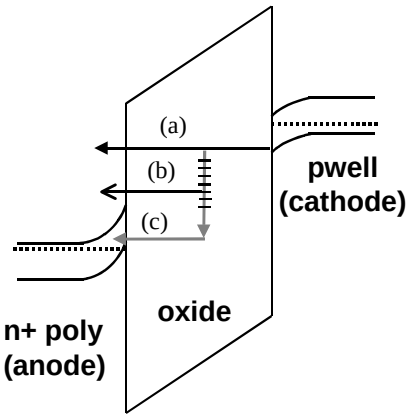

Figure 18. Band diagram for (a) tunneling from pwell valence band to poly conduction band. (b) Tunneling from pwell valence band to poly conduction band via inelastic trap assisted tunneling through bulk traps. (c) Tunneling from pwell valence band to poly valence band via inelastic trap assisted tunneling through bulk traps after the poly inverts.

CONCLUSIONS

The E-field model is a physically incorrect description of breakdown in ultrathin gate oxides. Breakdown is determined by the maximum rather than average electron energy dissipated at the anode, and is therefore voltage driven. Although interface traps are the dominant SILC defect produced below 5 V stress, breakdown remains controlled by bulk trap generation. The anode hole injection model is indeed a possible explanation for voltage driven breakdown. However, another mechanism such as anode hydrogen release must also be operative to account for interface trap generation under direct tunneling stress conditions.

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