Design and Evaluation of Efficient Power and Speed for Full Adder

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***Abstract*—**Arithmetic and Logic Unit (ALU) is an important component of the CPU. In ALU, adders not only perform addition, but also performs many other basic arithmetic operations like subtraction, multiplication, etc. Thus, for the better performance of an ALU and the processor, an efficient adder is required. Research started in late 1950s on designing efficient adder algorithms and their hardware implementation. Many designs based on serial and parallel structures have been proposed to optimize different parameters from time to time.

The first contribution of this thesis is the development of an efficient adder architecture that addresses the problems for higher bit operand lengths like fan-out, wiring complexity, etc. To improve the quality factors of the application specific adder architecture design, an efficient adder design is demonstrated in this paper. These parameters are propagation delay and power dissipation problem. Adder being one of the basic unit of processing system implies various adders to form a single adder structure for specific system architecture. Ripple Carry adder being one of them, utilizes the adder units to form n-unit adder system. Though, ripple carry adder is an older technique but still its improvement is necessary because of it area of application.

Finally, novel version of adder design is presented and implemented on ripple carry adder, which shows the improved and longitivity efficiency of the system design. Designs of the previous work are improved and implemented on CADENCE Virtuoso schematic circuit simulator.

Keywords*—*Arithmetic and Logic Unit, Adder, Ripple carry adder, Propagation Delay, Power dissipation.

I. Introduction

In various fields of engineering there are inescapably arrangement to be made and to equalize the performance against power consumption is one of the primary tradeoffs that designers are facing today. Through various factors such as voltage levels, micro architecture, logic style, or gate sizing the balance between the two can be made by the designer in order to fulfill his goals. The designers choice basically depends upon the information based on the after – effects of their decisions, and to expect the after – effect of their choices circuit designers uses models of changing accuracy and speed. A precise comprehension of the causes and seriousness of the power consumption inside a chip may impact the designer to make certain arrangements between speed and power, however a less exact understanding may lead to tradeoffs that are more awful for overall performance. Obviously, a precise portrayal of how a microchip consumes power is instrumental to great design. Circuit movement is the deciding factors in energy dissipation. In this particular thesis I will be taking a gander at adders particularly and will be deciding activity factors exploratory. From that point, I will be inspecting how these deviate from standard models and how this difference influences design decisions [6]-[9].

The most widely recognized methods for deciding the power consumption of a circuit is to expect some steady deviating action factor for each of the gates in circuit, and after that utilization that to decide the overall power utilization of that segment of the circuit.

The following equation is generally utilized.

$$P_{total} = p_t(C_L.V.V_{dd}.f_{clk}) + I_{sc}.V_{dd} + I_{leakage}.V_{dd} \quad (1)$$

Here the main term expresses the power dissipated by exchanging movement and the second term express the short circuit power loss and the third speaks to the power lost because of spillage. In the primary term p_t speaks to the activity factor, C_L speaks to the loading capacitance, V represents swing voltage, V_{dd} represents supply voltage, and f_{clk} is the clock recurrence. Inside the second term I_{sc} speaks to the short circuit current that happens once the adder is in an intermediary state and the third spillage speaks to the spillage current. The value of p_t is determined by utilizing rules of thumb, for example, accepting a 15% activity factor for gates in static adders and 50% action factor for gates in dynamic adders, while alternate factors can be resolved decisively.

A more complex way to deal with power estimation includes reproducing the circuit block being referred to for some arrangement of data sources. It is normally very tedious to run enough input vectors to make sure that the outcomes are adequately precise, however there are numerous approaches to accelerate or estimated the procedure that can be utilized if the

experimenter accept that the contributions to the adder are measurably autonomous of each other, and progressively that can be utilized if the extra presumption that the information sources are Bernoulli forms is additionally utilized. These presumptions and approximations are generally utilized, and with adders it is for the most part accepted by designers that each information is a Bernoulli Procedure with each information having an equivalent shot of being either a one or a zero autonomous of its neighbors or of past specimens. Once the activity variables of the different gates have been resolved, an indistinguishable condition from in the steady action factor technique can be utilized to evaluate power utilization [1]-[4].

A. Basics of Adder Design

Arithmetic and Logic Unit ALU is a basic component in CPU. In, Arithmetic and Logic Unit adders assume a noteworthy part for additions well as in performing numerous other fundamental arithmetic operations like subtraction, duplication, increment/decrement and so forth. Consequently, understanding a proficient adder is required for higher performance of a processor regularly and Arithmetic and Logic Unit (ALU particularly. Research into the design of efficient adder algorithms for hardware implementation of Very Large Scale Integrated VLSI arithmetic circuits started in late 1950's. Several designs based on serial and parallel structures were proposed to optimize different parameters from time to time. Binary addition consists of four potential elementary operations, which are shown in the following table 1.

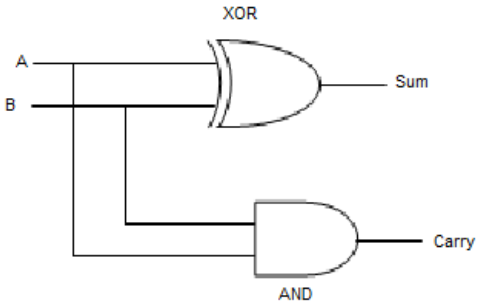
Table 1 Truth table logic of Half Adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The initial 3 operations produce just a "Sum" whose length is 1 digit, however once both augend and addend bits are equivalent to 1, the binary sum comprises of 2 digits. The higher critical bit of this outcome is known as 'Carry'. A combinational circuit that plays out the addition of two bits is known as a half-adder while the one that plays out the addition of three bits is known as a full-adder.

B. Half Adder

Half adder includes two input bits A, B and creates a carry (C)and sum (S), which are the two results of a half adder. In the event that A and B are the input bits, at that point sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is unmistakably clear that half adder circuit can be effortlessly designed utilizing one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit, yet it has a noteworthy disadvantage. The half adder just includes two input bits (A and B) and it has nothing to do with the carry if there is any in the input. Along these lines if the contribution to a half adder has a carry, at that point it will be overlooked and adds just the A and B bits. That implies the binary addition process isn't finished and that is the reason it's alluded to as a half adder.



"*Fig. 1, Logic Design of Half Adder*"

Truth table and equations got out of Half Adder configuration utilizing fundamental logic gates.

Table 2 Truth table logic of Half Adder

INPUT A	INPUT B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Equations obtained from Half Adder design are shown below and also is shown their XOR implementation.

$$SUM = A'.B + A.B' \quad (2.2)$$

Or it can also be written as

$$SUM = A \oplus B \quad (2.3)$$

$$CARRY = A.B \quad (2.4)$$

C. Full Adder

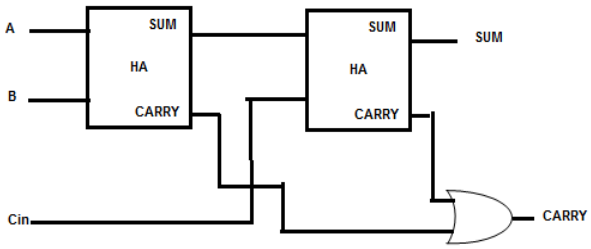
The real distinction between Full Adder and Half Adder is that a full adder includes two input bits (A, B) in addition to a carry bit (Cin) got from past stage and yields one outcome bit (S) and one carry yield (Cout) as appeared in underneath diagram.

The full adder is a legitimate circuit that plays out an addition operation on 3 binary digits and it likewise produces a carry out. Carry - in is a conceivable carry from a less noteworthy digit, while a Carry - out signifies carry to be more critical digit.

We can state that full adder can be worked with two half adders, where the carry of main half adder is passed to the second half adder.

Table 3 Truth Table implementation of Full Adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



"*Fig. 2, Full Adder Implementation using two Half Adder*

The Boolean expression for Full adder is shown below in equation

$$SUM = A'.B'.C + A'.B.C' + A.B'.C' + A.B.C \quad (3.1)$$

Or this can be written in precise as

$$SUM = (A \oplus B) \oplus C \quad (3.2)$$

$$CARRY = A'.B.C + A.B'.C + A.B.C' + A.B.C \quad (3.3)$$

Or we can write,

$$CARRY = A.B + C(A \oplus B) \quad (3.4)$$

D. Ripple Carry Adder

As appeared above single one – bit binary adders can be developed from fundamental logic gates. In any case, with a specific end goal to add 2n – bit numbers, n quantities of 1 – bit full adders should be connected or "cascaded" together to produce what is known as a Ripple CarryAdder. Different full adder circuits can be added in parallel to add an N-bit number. There must be N number of full adder circuits, for N – bit parallel adder. A ripple carry adder is basically a logic circuit in which the carry out of first full adder is the carry in for the prevailing next full adder. Since each carry bit gets rippled into the following stage along these lines it is called ripple carry adder. Until the carry in of a specific stage happens, the Cout and sum bit of that specific half adder stage won't be legitimate. The explanation behind this is essentially the propagation delay inside this logic circuitry. Propagation delay is essentially the time distinction between the utilization of an input and occurrence of corresponding output. For instance, in case of NOT gate when the input is 1, yield will be 0 and the other way around. The time taken by the NOT gates yield to end up 1 after the utilization of input 0 to the NOT gate input is the propagation delay. So also, the time that slipped between the use of the carry in signal and the occurrence of the carry out (Cout) signal is known as the carry propagation delay.

Same as the primary binary adder, the 2nd binary adder in the chain likewise creates a summed yield (the second bit) and another carry - out bit comparably to add vast numbers we can continue adding full adders to the blend, connecting the carry bit yield from the main full adder to the following full adder etc.

One of the primary weaknesses of "cascading" together one-bit binary adders to add vast binary numbers is that the yield is known after the carry that has been created by the past stage is delivered. Along these lines, the sum of the most significant bit is just accessible after the carry signal has undulated through the adder from the minimum critical stage to the most significant stage. Therefore, the sum bit and carry bit will be substantial after a considerable delay.

The summing velocity of this adder is not essential if the measure of the bits to be included is not very large for e.g. 4 or 8 bits. Henceforth this delay may not be vital. While if there should arise an occurrence of bigger bit size for e.g. 32 or 64 utilized as a part of multi-bit adders, addition is required at a high clock speed, and this delay wind up plainly conspicuous if the addition procedure is not finished effectively inside one clock cycle.

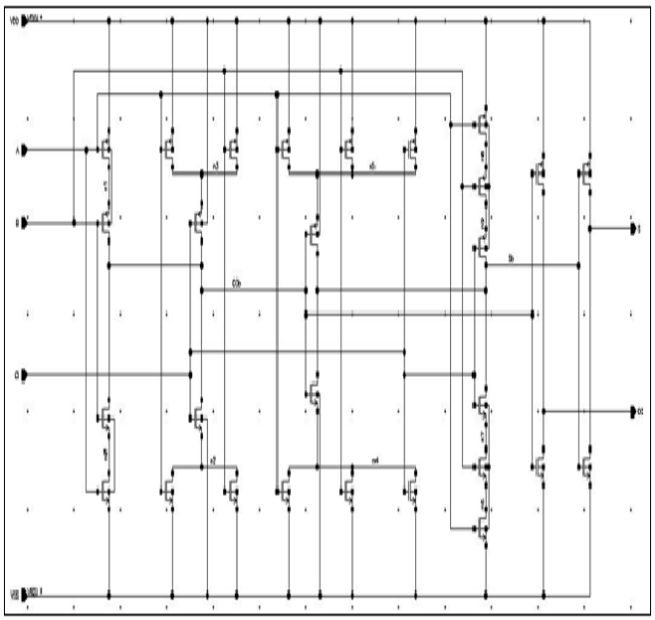
II. CMOS Implementation

A. Full Adder

A conventional full adder design consumes more power, produces more delay and occupies larger area. This gave rise to the problems of inefficient processing systems. Thus, the need rose for designing efficient adder units to improve the functionality of processing systems. The factor deciding the efficiency of any processing system architecture are power, propagation delay, area, etc. the CMOS implementation of a design gives the details and briefs about that design and that can be analyzed. The regular full adder configuration utilizes 28 transistors while in this thesis work another adder is intended to give preferred performance over the current designs.

The one-bit full adder cell consists of 28 transistors. Distinctive logic design can be explored from various perspectives. Clearly, they tend to support one performance perspective to the detriment of others. As such, it is entirely different design imperatives enforced by the application that every logic style includes its place inside the cell library development. Indeed,

even a chosen style that is proper for a specific function have chances that it may not be suitable for another.



"Fig. 3, Conventional full adder design"

For instance, static approach that presents sturdiness against noise impacts, so naturally gives a reliable operation. The trouble of simplicity of design is not generally accomplished effortlessly. The CMOS configuration style is not area economical for complex gates with expansive fan-ins. In this manner, ample care must be taken when a static logic style is selected to realize a logical function. Pseudo NMOS approach is simple, in any case it bargains noise margin and experiences static power dissipation. The Pass transistor logic style is believed to be a favored strategy for actualizing some particular circuits, for example, multiplexers and XOR-based circuits, similar to adders. Then again, dynamic logic encourages the realization of fast, small and complex doors. In any case, this favorable condition is gained at the detriment of parasitic impacts like load sharing, which makes this design procedure risky. Charge spillage requires constant refreshing, decreasing the operational frequency of the circuit. As a rule, none of the said styles can contend with CMOS style in strength and solidness.

B. Ripple Carry Adder

Since the carry bit "ripples" from one phase to the next consequently this setup is named as ripple carry adder. The delay through the circuit relies on the amount of logic stages that must be traversed and is an element of applied input signals. Fig2.5: Four-bit Ripple Carry Adder the corresponding adder design, using CMOS is shown in above fig-2.6 needs 28 transistors. This circuit is slow because; This configuration is termed as ripple carry adder. Long chains of PMOS transistors are present in both CARRY and SUM generation circuits.

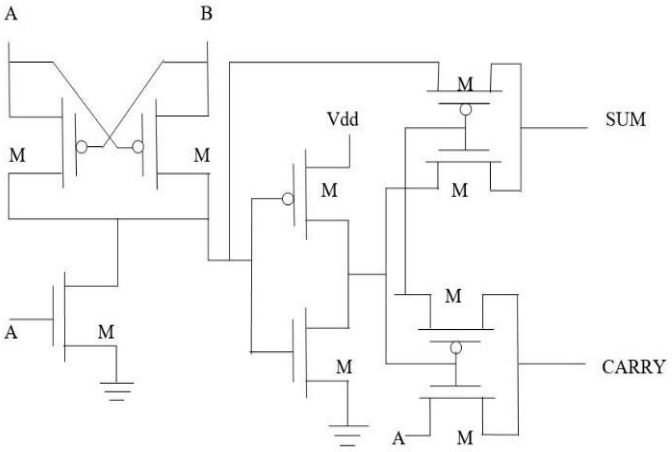
III. Proposed Work & Methodology

The goal of the research is to beat the issue of power consumption and propagation delay in a current design of Full Adder so as to accomplish:

1. High speed
2. Lower power consumption

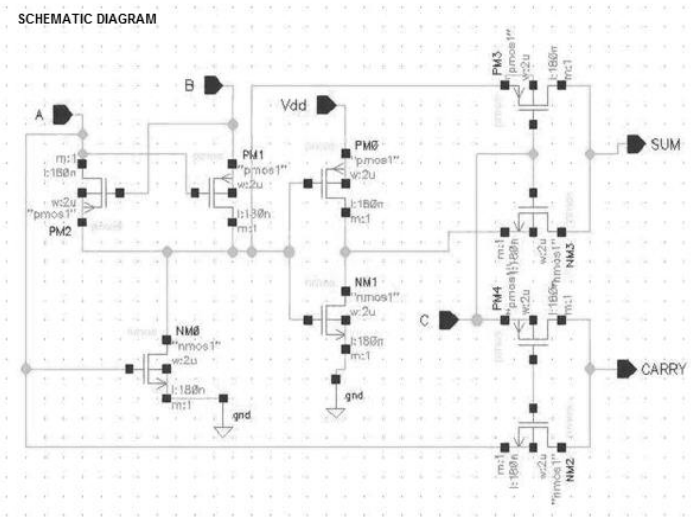
A. Proposed Methodology

In the current work the design application of Full adder is finished utilizing XOR-XNOR (3T) based Full adder topology. The design is as appeared underneath in Fig. 4.1. This design is implemented by varying the channel length and configuration to achieve an optimized adder design which is then further implemented on 3- bit Ripple carry adder. The obtained figures are as shown below.



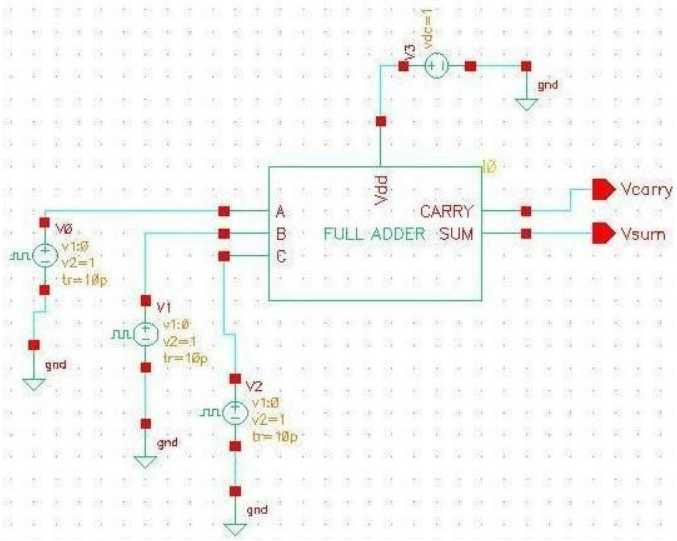
"Fig. 4, Proposed design"

This is the fundamental unit for the application of Ripple carry adder. The proposed design is appeared in the schematic usage beneath in fig 4.



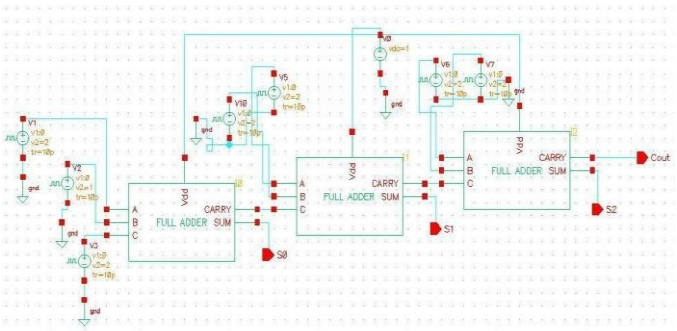
"Fig. 5, Schematic diagram for Full Adder design"

The block diagram of XOR-XNOR (3T) based full adder design is demonstrated in fig. 6



"Fig. 6, Block implementation of Full Adder design"

This full adder design is then implemented on the 3- bit Ripple Carry adder. This is demonstrated in the fig.7



"Fig. 7, Design implementation of Full adder utilizing Ripple Carry adder"

IV. Result & Discussion

A. Simulation Results

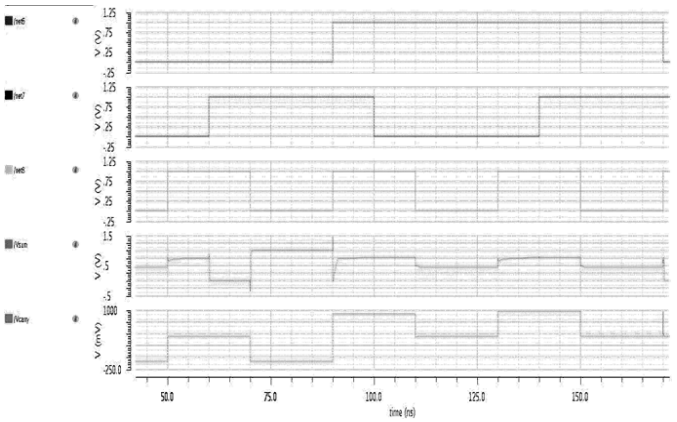
All the schematics were designed and simulated in schematic environment of CADENCE virtuoso schematic simulator. The designed CMOS based configurations were analyzed on 0.18µm CMOS technology. The executed designs were evaluated on the basis of power and delay of the adder hardware. The proficiency of any ALU system relies upon the essential adder unit of the system. The more efficient is the basic composition unit design of any system, the more efficient will be the processing system. This helps the processing system to provide on time results for any analysis done. The fundamental adder unit is implemented using Ripple Carry Adder. And then all the designs are analyzed for power and speed optimization for this process.

The essential application of adder configuration is XOR-XNOR based Full Adder. This design depends on XOR-XNOR setup and utilizes 9 transistors for Full Adder design usage. Also, the design implemented is based on varied aspect ratio. The width by length ratio of each transistor has been modified to 4µm/180nm. This results in reduced leakage current and improved power consumption. The improved circuitry was then implemented to design Ripple Carry Adder and it was found that the power consumed in the Full adder design based 3-bit Ripple Carry Adder circuitry is 140.7e-9W and the delay in achieving the output is 19.38e-6. The waveform got from the above investigation is appeared underneath in the accompanying figures and table.

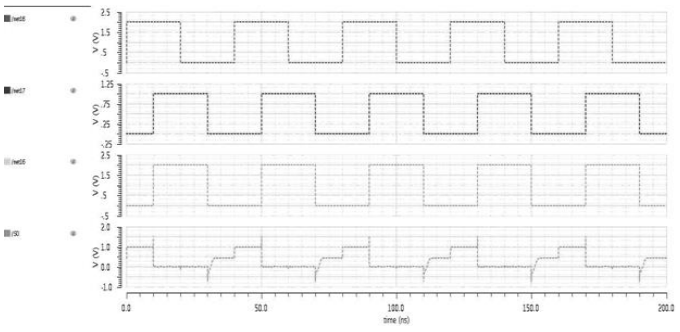
Table 4 Simulation results of Ripple Carry Adder Design

Ripple Carry Adder Parameters	Simulated Output
Power	140.7e-9
Delay	19.38e-6

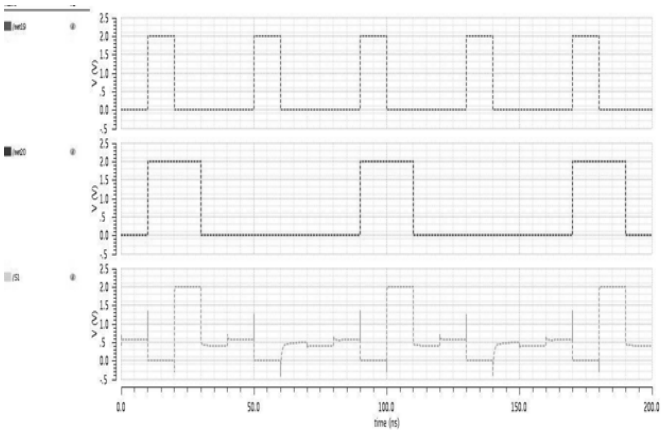
The simulation waveform is also shown below in the following figures.



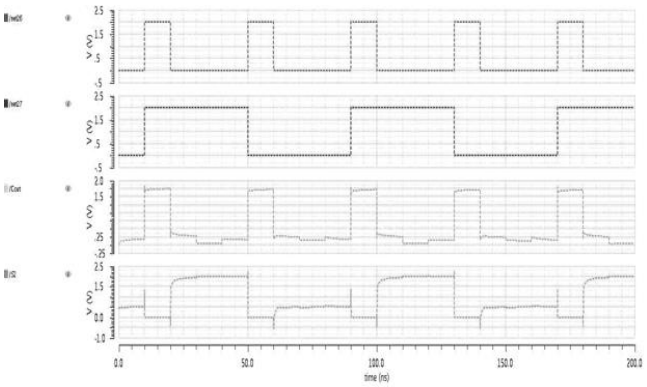
"Fig. 8, Waveform of XOR-XNOR based Full Adder Design"



"Fig. 9, S_0 output waveform of Ripple Carry Adder in view of proposed Full Adder."



"Fig. 10, S_1 output waveform of Ripple Carry Adder in view of proposed Full Adder."



"Fig. 10, S2 and Carry output waveform of Ripple Carry Adder in view of proposed Full Adder"

B. Comparison & Validation of Results

Table 5 Comparative analysis of the proposed design with existing work

Parameter	Proposed work	Existing work
Power	19.38e-6	20.35e-6
Delay	140.7e-9	151.3e-9

v. conclusion

In this paper the proposed technique for planning a efficient Full Adder unit utilizing XOR-XNOR based design was seriously studied. The aspect proportion was diminished with a specific end goal to accomplish low power and increased speed necessity. It is likewise proposed to confirm its design productivity in greater logic circuitry. For this reason, a 3-bit Ripple Carry Adder circuitry is utilized to confirm the application of the proposed Full Adder Design. The proposed strategy is first checked in CADENCE circuit simulator and afterward actualized for 3-bit Ripple Carry Adder. The ripple carry adder implemented in these conditions produces tasteful outcomes.

This work focuses on implementation of Full Adder unit for satisfactory performance and also the results of this work shows the performance as an optimized designed system, which could be confirmed from the table shown in result section of this thesis work.

References

[1] X. J. Zhang, P. D. Liu, D. R. Wang, "The design and implementation of smart battery management system balance technology", JCIT: Journal of Convergence Information Technology, vol. 6, no. 5, pp. 108-116, 2011. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[2] D. Markovic, C. C. Wang, L. P. Alarcon, T. Te Liu, J. M. Rabaey, "Ultralow-power design in near-threshold region", Proceedings of the IEEE, vol. 98, no. 2, pp. 237-252, 2010.

[3] [3] W. Q. Zhang, L. Su, Y. Zhang, L. F. Li, and J. P. Hu, "Low-leakage flip-flops based on dual-threshold and multiple leakage reduction techniques", JCSC, vol. 20, no. 1, pp. 147-162, 2011.

[4] [4] N. K. Singh and P. K. Sharma, "A Novel 4T XOR based 1 Bit Full Adder Design", International Conference for Convergence of Technology, 2014 IEEE.

[5] [5] D. Radhakrishnan, "Low-Voltage Low-Power CMOS Full Adder", IEEE Proceedings on Circuits Devices and Systems, Vol. 148, No. 1, pp. 19-24 February 2001.

[6] [6] Vojin G. Oklobdzija, Bart R. Zeydel, Hoang Q. Dao Sanu Mathew, and Ram Krishnamurthy. "Comparison of high-performance vlsi adders in the energy delay space," IEE Transaction on Very Large-Scale Integration (VLSI) Systems, Vol. 13, Issue 6, June 2005, pp. 754-758.

[7] A. M. Shams, T. K. Darwish, M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells", IEEE Transactions on VLSI Systems, vol. 10, no.1, pp. 20-29, 2002.

[8] [8] Rashmi D S, Sadiya, Rukhsar R, Shilpa H R, Vidyashree C R, Kunjan D. Shinde and Nithin H V, "Modeling of Adders using CMOS and GDI Logic for Multiplier Applications," IEEE Conference on Circuit, Power and Computing Technologies [ICCPCT], March 2016, pp. 34-39.

[9] [9] Subodh Wairya, Rajendra Kumar Naaria and Sudarshan Tiwari, "Comparative Performance Analysis of XORXNOR Function Based High-Speed CMOS Full Adder Circuits for Low Voltage VLSI Design," International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, April 2012, pp. 222-242.

[10] [10] Mohammad JavadZavarei, Mohammad Reza Baghbanmanesh, EhsanKargaran, HoomanNabovati, Abbas Golmakani, "Design of New Full Adder Cell Using Hybrid-CMOS Logic Style", IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp.-451-454, Nov 2011.

[11] DivakarTamang, Vinay Pandey and Neeraj Kumar Singh, "A Sub-Threshold Operation of XOR based Energy Efficient Full Adder," IEEE Conference on Communication and Signal Processing, April 6-8, 2016, pp. 1066-1069.

[12] Mr. Kunjan D. Shinde, Mrs. Jayashree C. N. "Comparative Analysis of 8-bit Adders for Embedded Applications", Proceedings of the IJERT in National Conference on "Real Time System (NCRTS-14)" at City Engineering College Bangalore, Karnataka, India. 9th and 10th May 2014, ISSN-2278-0181 pp. 682 to 687, NCRTS'14 Conference Proceedings, IJERT publication

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