Study of the Propagation Delays and Rise, Fall time of Gate based and Static CMOS based Circuit Designs

Harshel Jain[1], Ashish Verma[2]
[1]*B.Tech, Department of Electronics and Comm. Engineering, MNIT Jaipur*
[2]*Associate Professor, Department of Physics, Dr. Harisingh Gaur Central University, Sagar*

Abstract - The performance of the digital circuits is graded on the basis of their speeds and power consumption. Speed can be defined as the number of times the voltage switches from one state (H/L) to other (L/H). Therefore for a higher speed the output will come out in less time. So the speed of a circuit is greatly affected by the time it takes to go from high voltage to low voltage (also known as fall time) and low voltage to high voltage (also known as rise time). There is a third parameter known as propagation delay which also affects the speed of the digital circuits. Propagation delays (t_{PHL} & t_{PLH}) are directly proportional to the time taken by the circuit to process the data and give the output. Hence higher the propagation delay more time will be taken to receive the output. In today's electronic circuits in which millions of transistors are employed, the summation of the propagation delays and also the rise and fall times can affect the speed and hence performance of the systems at an unimaginable intensity. So improving upon these parameters is very important to achieve high speed systems and devices.

Keywords **-** Combinational Logic, Sequential Logic, CMOS Design Logic, Gates, VLSI Design, Propagation Delay, Rise Time, Fall Time

I. INTRODUCTION

Today CMOS gates are widely used in the electronic manufacturing industry [1]. These gates simplified the designing and implementation of logic operations and functions. Their usage includes designing of combinational circuits like Adders [2-4], Encoders [3,4], Decoders [3,4], MUXs [3,4] and sequential circuits like SR flip-flops [3-5], JK flip-flops [3-5], D flip-flops [3-5], Registers [3,4] etc. These are also used in designing ASICs [6] like sensors, controller ICs and signal processors to name a few. The performance of the digital circuits is graded on the basis of their speeds and power consumption. Speed is defined as the number of times the voltage switches from one state (H/L) to other (L/H). Therefore for a high speed circuit, output takes less time compared to a low speed circuit. This is the time that is required by the output signal to go from high voltage to low voltage (also known as fall time) or low voltage to high voltage (also known as rise time) in the circuit [7,9]. In addition to above mentioned parameters, another parameter that also affects the speed of the digital circuits is propagation delay. The time taken by the circuit to process the data and give the output is directly proportional to the propagation delay (t_{PHL} & t_{PLH}) [8,9]. Hence for high values of propagation delay, the time required will be more in receiving the output from that circuit. Today's digital circuits comprise of numerous combinational as well as sequential logic components. All these components determine the performance of that circuit. So the summation of the propagation delays and rise and fall times of all these components affect the speed and hence performance of the systems at an unimaginable intensity. Therefore in order to achieve high speed systems and devices, it is required to reduce the propagation delay and the rise and the fall times in order to get optimum performance. The two important design logics for digital circuits are "CMOS gates based logics" and the "Static CMOS logics" [9]. The gate based logic has widely been used and is better than the BJT transistor based logic. But when it is compared to the static CMOS logic, the transistor count [4,9] of these gates exceeds the transistor count of the static CMOS logic in many cases [9]. This increase in the transistor count may result in an increase of the chip area. However, the more prevalent problem is the increase in the propagation delays (t_{PHL} & t_{PLH}) and the rise (t_{rise}) and fall (t_{fall}) times of the CMOS gates. As these parameters are responsible for performance slumps and slowed data transfer rates, improvements are required that boost the speed of the binary operations and the entire processing task significantly [12]. In this paper, different combinational circuits like Priority Encoder, Decoder, Multiplexer and Adder and also some sequential circuits like SR, JK and D flip-flops have been designed and compared on the basis of various parameters like propagation delay, rise time, fall time and transistor count. The results are discussed.

II. EXPERIMENTAL METHODOLOGY

The circuit simulation software LT SPICE IV has been employed to design different circuits reported in this paper using both 'Gate based logic' and 'Static CMOS transistor based logic'[13]. The combinational circuits like Priority Encoder, Decoder, Multiplexer and Adder and also some sequential circuits like SR, JK and D flip-flops circuits are compared.

III. RESULTS AND OBSERVATIONS

The observations for different systems are summarized in the following tables:

- 2X1 MULTIPLEXER

Table 1: Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) for 2X1 MULTIPLEXER

Properties	GATE BASED 2X1 MULTIPLEXER	STATIC CMOS 2X1 MULTIPLEXER
$^{out}t_{PLH}$	-27.56 ps	835.03 fs
	-27.47 ps	3.738 ps
$^{out}t_{PHL}$	24.32 ps	-2.8 ps
	24.56 ps	419.39 fs
	24.32 ps	846.71 fs
$^{out}t_{rise}$	60.30 ps	33.75 ps
	60.04 ps	33.63 ps
$^{out}t_{fall}$	70.05 ps	29.23 ps
	71.98 ps	29.34 ps
	70.05 ps	29.76 ps

Transistor count for 2X1 MULTIPLEXER -

- Gate based: 20
- Static CMOS based: 12
- 2X4 DECODER

Table – 3: Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) for 2X4 DECODER

Properties	GATE BASED 2X4 DECODER	STATIC CMOS 2X4 DECODER
$^{out}t_{PLH}$	247.5 fs	5.71 fs
	-276.07 fs	12.78 fs
$^{out}t_{PHL}$	-276.25 fs	-18.72 fs
	246.31 fs	-24.60 fs
	-425.26 fs	-25.43 fs
$^{out}t_{rise}$	700.74 fs	85.55 fs
	701.90 fs	35.57 fs
$^{out}t_{fall}$	600 fs	74.28 fs
	600.79 fs	412.06 fs
	702.39 fs	32.24 fs

Transistor count for 2X4 DECODER -

- Gate based: 28
- Static CMOS based: 28
- 4X2 PRIORITY ENCODER

Table – 5: Rise and Fall time Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) for 2X1 PRIORITY ENCODER

Properties	GATE BASED 2X1 PRIORITY ENCODER			STATIC CMOS 2X1 PRIORITY ENCODER		
	S1	S0	V	S1	S0	V
$^{out}t_{PLH}$	-425 fs	222.89 fs	-267.34 fs	-170.60 fs	0.1289 fs	-307.10 fs
	-265.78 fs	-266.48 fs	-267.34 fs	-170.60 fs	10.67 fs	-286.57 fs
		-266.44 fs			169.42 fs	
$^{out}t_{PHL}$	221.44 fs	1.22 ps	289.95 fs	24.87 fs	1.02 ps	199.73 fs
	221.44 fs	222.17 fs		24.87 fs	11.85 fs	200 fs
		201.31 fs			11.85 fs	
RISE	700.59 fs	700.74 fs	700.74 fs	252.44 fs	378.41 fs	335.80 fs
	699.94 fs	700.15 fs	700.15 fs	252.81 fs	377.82 fs	335.17 fs
FALL	760.68 fs	760.52 fs	700.39 fs	501.11 fs	530 fs	495.51 fs
	760 10 fs	761.82 fs	700.26 fs	503.43 fs	506.93 fs	493.93 fs

Transistor count for 2X1 PRIORITY ENCODER

- Gate based: 30
- Static CMOS based: 26
- 1-BIT FULL ADDER

Table – 7: Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) 1-BIT FULL ADDER

Properties	GATE BASED 1-BIT FULL ADDER		STATIC CMOS 1-BIT FULL ADDER	
	SUM	CARRY	SUM	CARRY
$^{out}t_{PLH}$	289.9 fs	-425.06 fs	-18.87 fs	6.29 fs
	291.34 fs	-266.18 fs	0.331 fs	13.84 fs
		-266.18 fs	0.111 fs	6.54 fs
$^{out}t_{PHL}$	289.9 fs	290.17 fs	2.13 fs	1.18 fs
	290.43 fs	290.56 fs	1.42 fs	44.07 fs
		290.17 fs	35.88 fs	-169.31 fs
RISE	700.39 fs	700.39 fs	138.20 fs	343.65 fs
	700.15 fs	700.527 fs	148.43 fs	343.16 fs
	702.10 fs	699.538 fs	230.13 fs	343.12 fs
FALL	700.25 fs	700.59 fs	173.82 fs	459.76 fs
	700.52 fs	699.68 fs	390.98 fs	223.64 fs
	699.68 fs	700.26 fs	174.13 fs	459.12 fs

Transistor count for 1-BIT FULL ADDER

- Gate based: 36
- Static CMOS based: 28
- SR FLIP-FLOP

Table – 9: Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) for SR FLIP-FLOP

Properties	GATE BASED SR FLIP-FLOP	STATIC CMOS SR FLIP-FLOP
	Q_{n+1}	Q_{n+1}
$^{out}t_{PLH}$	0.985 fs	-34.74 fs
	0.793 fs	-34.45 fs
	0 fs	-34.74 fs
$^{out}t_{PHL}$	0.70 fs	-35.25 fs
	0.71 fs	-11.10 fs
	0.71 fs	-35.25 fs
RISE	4.02 ps	78.58 fs
	3.998 ps	117.77 fs
	4.04 ps	116.77 fs
FALL	4.01 ps	366.9 fs
	4 ps	367.13 fs
	3.99 ps	364.28 fs

- Transistor count for SR FLIP-FLOP
  - Gate based: 20
  - Static CMOS based: 12
  - JK FLIP-FLOP

Table – 11: Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) JK FLIP-FLOP

Properties	GATE BASED JK FLIP-FLOP	STATIC CMOS JK FLIP-FLOP
	Q_{n+1}	Q_{n+1}
$^{out}t_{PLH}$	-268.46 fs	109.76 fs
	-268.13 fs	109.81 fs
	-267.018 fs	109.76 fs
$^{out}t_{PHL}$	290.62 fs	108.21 fs
	289.96 fs	107.93 fs
	289.36 fs	108.21 fs
Low → High	700.52 fs	161.95 fs
	699.47 fs	162.38 fs
	702.37 fs	161.95 fs
High → Low	700.92 fs	500.01 fs
	700.26 fs	502.33 fs
	700.84 fs	502.01 fs

Transistor count JK FLIP-FLOP -

- Gate based: 24
- Static CMOS based: 16
- D FLIP-FLOP

Table – 13: Propagation Delay ($^{out}t_{PLH}$ and $^{out}t_{PHL}$) for D FLIP-FLOP

Properties	GATE BASED D FLIP-FLOP	STATIC CMOS D FLIP-FLOP
	Q_{n+1}	Q_{n+1}
$^{out}t_{PLH}$	-268.46 fs	115.5 fs
	-268.13 fs	115.71 fs
	-267.018 fs	115.50 fs
$^{out}t_{PHL}$	290.62 fs	-3.75 fs
	289.96 fs	-3.84 fs
	289.36 fs	-3.80 fs
Low → High	700.52 fs	168 fs
	699.47 fs	169 fs
	702.37 fs	168 fs
High → Low	700.92 fs	182.36 fs
	700.26 fs	183.88 fs
	700.84 fs	182.17 fs

Transistor count D FLIP-FLOP

- Gate based: 26
- Static CMOS based: 18

IV. DISCUSSIONS

From the above observation tables we notice and conclude the following

- In the 2X1 Multiplexer, 4X2 Priority Encoder, JK flip-flop and D flip-flop the t_{PLH} of Gate level designs is faster while the static CMOS based designs are faster for the t_{PHL}.(Tables 1, 5, 11, 13)
- In the 2X4 Decoder, the gate level design is faster than the static CMOS based design for both t_{PLH} and t_{PHL}.(Table 3) d
- In the 1-bit Full Adder, the propagation delays (t_{PLH} and t_{PHL}) for the static CMOS transistor SUM bit has a lower value compared to the gate level design. The t_{PLH} of gate level CARRY bit is faster than the static CMOS based design while it is opposite for the t_{PHL}.(Table 7)
- In the SR flip-flop, the static CMOS based design is faster than the gate level design for both t_{PLH} and t_{PHL}.(Table 9)

From the rise and fall time data, it can be seen that the static CMOS based design is much faster than the gate level design for all the circuits used. From the transistor count data, we see that the transistor count of Multiplexer, Decoder, Encoder, Adder, SR flip-flop, JK flip-flop and D flip-flop for static CMOS based designs is 12, 28, 26, 28, 12, 16 and 18 respectively. While for gate level designs the transistor count is 20, 28, 30, 36, 20, 24 and 26 respectively.

From the observation tables, it can be seen that some propagation delay values are negative. This negation is signifying that the output is reaching its desired value i.e. 50% of its maximum value before the input reaches 50% of its maximum value. This anomaly is taking place due to the use of generic NMOS and PMOS transistors.

The interpretation of the negative value is as follows:

- Circuits with values farther below zero are considered faster than the circuits with values closer below zero as less time is taken to reach the desired output value.
- Circuits with negative values are considered faster than the circuits with positive values as less time is taken to reach the desired output value.

V. CONCLUSIONS

This paper compares the gate based and the static CMOS based design of various combinational and sequential circuits. It can be seen from the simulation results that most of the circuits (except the decoder) that have been used in this paper perform better (faster) when designed using the static CMOS based design logic rather than using the gate based design logic. This work will help to design faster combinational as well as sequential circuits.

Acknowledgement

One of the authors (HJ) is indebted to various people, who directly or indirectly contributed in the development of this work and who influenced his thinking, behavior, and acts during the course of study. He is grateful to **Prof. R. A. Singh**, Professor & Head, Dr. H.S. Gour University, Sagar for providing the facilities in the department to do the work. He is thankful to **Prof. K. K. Sharma**, Head, Department of Electronics and Communication Engineering, MNIT Jaipur for his support, guidance, and motivation. He is also grateful to **Prof. I. K. Bhat**, Director, MNIT Jaipur for providing him an opportunity to undergo summer training at Dr. Hari Singh Gour University, Sagar.

VI. REFERENCES

[1]. Some Common Applications of Logic Gates [http://www.electrical4u.com/some-common-applications-of-logic-gates/]
[2]. Area, Delay and Power Comparison of Adder Topologies[http://airccse.org/journal/vlsi/papers/3112vlsics13.pdf]
[3]. Digital Circuits And Design, 3rd Edition by S. Salivahanan, Vikas Publishing House Pvt. Ltd
[4]. Digital Design, 4th Edition by M. Morris Mano, Prentice Hall
[5]. Comparative Analysis of Timing Yield Improvement under Process Variations of Flip-Flops Circuits by Mostafa, H. ; Dept. of Electr. & Comput. Eng., Univ. of Waterloo; Anis, M. ; Elmasry, M. [http://ieeexplore.ieee.org/xpl/abstractKeywords.jsp?arnumber=5076396&queryText=flip+flops&newsearch=true&searchField=Search_All]
[6]. Application-Specific Integrated Circuit (ASIC) [http://www.techopedia.com/definition/2357/application-specific-integrated-circuit-asic]
[7]. Signal transition time effect on CMOS delay evaluation by Auvergne, D. ; Lab. d"Inf. de Robotique et de Microelectron. de Montpellier, CNRS, France ; Daga, J.M. ; Rezzoug, M. [http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=883331&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F81%2F19111%2F00883331]
[8]. Propagation Delay Calculation of CMOS Inverter [http://www.nptel.ac.in/courses/117101058/downloads/Lec-16.pdf]
[9]. Digital Integrated Circuits: A Design Perspective, 2nd Edition by Jan M. Rabaey, PHI Learning Private Limited.
[10]. Reducing the Number of Transistors in Digital Circuits Using Gate-Level Evolutionary Design by Zbysek Gajda and Lukas Sekanina [http://www.fit.vutbr.cz/~sekanina/publ/gecco07/gajda-sekanina.pdf]
[11]. CMOS VLSI Design : A Circuits and Systems Perspective (English) 3rd Edition by Neil H.E. We Weste, Pearson India
[12]. Propagation delay by Margaret Rouse [http://searchnetworking.techtarget.com/definition/propagation-delay]
[13]. LT SPICE - Getting Started [http://www.linear.com/docs/39806]