DESIGN OF HIGH PERFORMANCE ALU USING VEDIC MATHEMATICS

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Abstract— *This paper presents Multiply and Accumulate unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit ALU architecture along with 32-bit version and results are presented in comparison with conventional architectures. The efficiency in terms of area and speed of proposed ALU unit architecture is observed through reduced area, low critical delay and low hardware complexity. Comparison is made with the delay of ALU with different FPGA technology in Xilinx. The Simulation is performed using ISE and power analysis is done using the Xilinx tool for synthesis. The implemented architecture shows the improvement in delay and the low area is obtained based on the performance.*

Keywords— *Vedic Mathematics, urdhva triyakbhyam sutra, vedic multiplier*

I. INTRODUCTION

The general ALU design comprises of a traditional multiplier, adder and an aggregator. Where the yield is added to the past ALU yield result by a collect adder. The Multiply-Accumulate (ALU) unit is broadly utilized as a part of chip and computerized flag processors for data intensive applications, for example, separating, convolution, and inward items. Most computerized flag preparing strategies utilize nonlinear capacities, for example, discrete cosine change (DCT) or discrete wavelet change (DWT) or FFT/IFFT calculations that can be productively quickened by devoted ALU units. Since they are fundamentally proficient by monotonous utilization of duplication and expansion, the speed of the increase and expansion decides the execution speed and execution of the whole calculation. As the multiplier displays characteristically long deferral among the fundamental operational squares in computerized framework, the multiplier decides the basic way. Duplicate and Accumulate (ALU) unit configuration utilizing Vedic Multiplier, which depends on Urdhva Tiryagbhyam Sutra. The paper stresses a proficient 32-bit ALU design alongside 16-bit form and results are displayed in examination with ordinary structures. The productivity as far as zone and speed of proposed ALU unit engineering is seen through lessened zone, low basic deferral and low equipment unpredictability. The proposed ALU unit lessens the region by utilizing MUX in multiplier which utilizes two multipliers Instead of four multipliers and from decreasing the quantity of multipliers and Units Increase in the speed of task is accomplished by the various leveled nature of the Vedic multiplier unit. The proposed ALU unit is actualized on a field programmable entryway cluster (FPGA) gadget, 3S100ETQ144-5 (Spartan 3). The execution advancement

II. LITERATURE REVIEW

The proposed calculation is outline of Multiplier utilizing vedic multiplier technique and its utilization of Digital Signal processing.[1] NxN multiplier configuration utilizing four N/2 bit multiplier, two N-bit full adder ,one half adder and N/2 bit full adder to include the entirety and convey of half adder.[2] 16×16 exhibit of cluster Multiplier utilizing vedic multiplier this structure is various leveled plan calculation is urdhva triyagbhyam sutra on vedic mathematics.[4] The deferral of proposed ALU unit is 43.899 ns and Conventional ALU is 55.662 ns. The traditional and proposed ALU unit is coded on verilog-HDL and XILINX ISE simulator.[5] The recreation on Spartan-3e family utilizing XILINX ISE device and coding on verilog. The aftereffect of deferral is proposed multiplier is 41.562 ns and parallel multiplier is 94.087.[6]

Vedic arithmetic is the name given to the antiquated arrangement of science which was rediscovered from the vedas. It gives clarification of a few scientific terms including math, geometry, trigonometry and even analytics. it was developed by Shri Bharati krsna theertaji (1884-1960), after his eight long periods of research on Vedas. He built 16 primary sutras and 16 sub sutras. One strategy for increase is Urdhva Tiryakbhyam (Vertical and Crosswise) .The multiplier depends on a calculation Urdhva Tiryakbhyam (Vertical and Crosswise) of old Indian Vedic arithmetic. Urdhva Tiryakbhyam sutra is general increase recipe material to all instance of duplication. A. vedic Multiplier The primary motivation behind Vedic Mathematics is to have the capacity to settle complex computations by basic methods. The equation being short makes them for all intents and purposes basic in usage. Urdhva-tiryagbhyam (Vertically and transversely) sutra is general equation appropriate to augmentation task. The methodology connected for building up a 64 x 64-bit Vedic multiplier is to plan a 2 x 2-bit Vedic multiplier as an essential building module for the framework. In the following phase of advancement a 4 x 4-bit multiplier is outlined utilizing 2 x 2-bit Vedic multiplier. Assist in same way 8 x 8, 16 x 16 and32 x 32-bit Vedic multiplier is outlined. For the halfway item expansion for all phases of advancement a quick adders is utilized .Multiplier assumes an imperative part in the present computerized circuits. The multiplier depends on a calculation Urdhva Tiryagbhyam (Vertical and

transversely).This sutras demonstrates to deal with duplication of bigger number (N X N bits) by breaking it into littler sizes.

Advantages:

• Vedic multiplier is speedier than alternate multipliers.

• The zone required for vedic multiplier is little when contrasted with other multiplier design.

• ALU is utilized as a part of present day advanced flag handling. ALU dependably lie in the basic way that decides the speed of the general equipment frameworks.

• It is use in parallel and decimal number duplication and furthermore utilize unsigned and marked number increase.

Disadvantages:For complex duplications , even the framework winds up complex.

III. PROPOSED METHOD

The 32x32bit Vedic multiplier module as shown in the block diagram in Fig.7 it is easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section. It is analyze four block of 16x16bit multiplications, say a= a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0 and b= b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5b4 b3 b2 b1b0.So total two 32 bit input give to 16x16bit multiplications. The output line for the multiplication result will be of 64 bits as –S63 to S0.

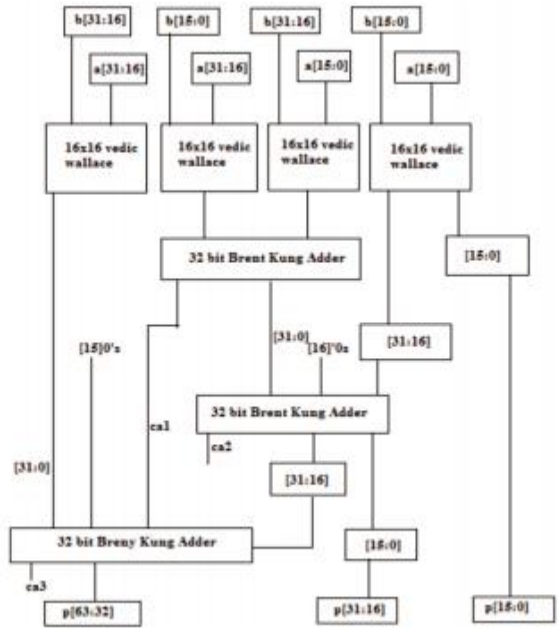

Figure 1. Schematic Diagram of 32x32 bit Vedic Wallace based Multiplier

The equipment engineering of 2x2, 4x4, 8x8, 16x16, 32x32 piece Vedic Wallace multiplier (VW) modules are shown in beneath segments. Here, "Urdhva-Tiryakbhyam" (Vertically and transversely) sutra is utilized to propose such an engineering for the increase of two parallel numbers. The excellence of Vedic Wallace multiplier is that, here halfway item age and increments are done simultaneously. Consequently, it is a very much adjusted parallel preparing. The highlights make it more appealing for double increases. This decreases deferral and this is the essential inspiration driving this work.

Design of Arithmetic Logic Unit

ALU was intended to play out the math and intelligent activities for the controller. Number-crunching activities performed are the 32-bit expansion, subtraction, and duplication. Intelligent activities performed are AND, OR, XOR, NAND, NOR, XNOR, NOT and Data Buffer. For planning the ALU, the creators had taken after an adaptable outline that comprises of littler, yet more sensible hinders, some of which can be re-utilized [2]. Outlining of half-adder, 2-bit multiplier, 4-bit Brent-Kung, 4-bit multiplier, 8-bit Brent-Kung adder, 8-bit multiplier, 8-bit full adder, 8-bit subtractor, 32-bit Brent-Kung adder, 32-bit multiplier, 32-bit full adder, 32-bit subtractor, 32-bit number juggling unit, legitimate unit and 32-bit ALU has been done .

S. No	Multiplexer Selection Lines and Operation						Operation Selected
	S(5)	S(4)	S(3)	S(2)	S(1)	S(0)	
1	0	X	X	X	0	0	Addition
2	0	X	X	X	0	1	Subtraction
3	0	X	X	X	1	0	Multiplication
4	0	X	X	X	1	0	Other
5	1	0	0	0	X	X	AND
6	1	0	0	1	X	X	OR
7	1	0	1	0	X	X	NAND
8	1	0	1	1	X	X	NOR
9	1	1	0	0	X	X	XOR
10	1	1	0	1	X	X	XNOR
11	1	1	1	0	X	X	NOT
12	1	1	1	1	X	X	DATA BUFFER

Table 1. Control Word for ALU Operations

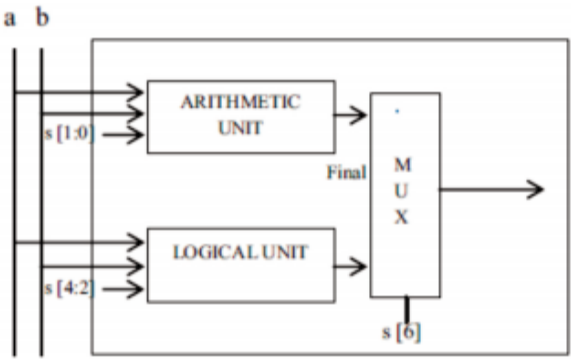

Figure 2. Schematic Block Diagram of Arithmetic Logic Unit

Arithmetic Unit An Arithmetic unit does the accompanying undertaking: Addition with convey, augmentation, and subtraction. A half adder is utilized to make the 4-bit Brent-Kung adder and afterward a 4-bit multiplier. •4-bit Brent-Kung adder is utilized to make the 8 bit BrentKung adder. The 8-bit multiplier is made by utilizing the 4-bit multiplier and 8-bit Brent-Kung adder. 8-bit subtractor. The 32-bit multiplier is made by utilizing the 16-bit multiplier and the 16-bit Brent-Kung adder. 32-bit subtractor. Number juggling unit utilizing multiplexer is outlined.

Logical Unit: For outlining of the legitimate unit, the execution of rationale circuits has been dissected by utilizing the ordinarily utilized rationale doors and a multiplexer. A Logic unit does the different tasks, for example, Logical AND, OR, XOR, NOT, NAND, NOR, XNOR, and information cushion. Notwithstanding this number juggling unit and consistent unit, they have been consolidated into the math rationale units. The schematic square graph of a math rationale unit is appeared in Figure 9 that is clear as crystal in itself. The yield of the ALU and Logical Unit is 64 bits. Table 1 demonstrates the control word for ALU activities

IV. SIMULATION RESULTS

2. Summary
2.1. On-Chip Power Summary

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	0.00	0	---	---
Logic	0.00	4242	11776	36
Signals	0.00	4350	---	---
IOs	0.00	135	372	36
Quiescent	31.52			
Total	31.52			

Figure 3. POWER report

LUT4:I2->O	1	0.648	0.563	VV11/Kk3/K1/GC16/G8 (VV11/Kk3/K1/GC16/G8)
LUT3:I0->O	1	0.648	0.423	VV11/Kk3/K1/GC16/G27_SW1 (N1277)
LUT4:I3->O	6	0.648	0.812	VV11/Kk3/K1/GC16/G27 (VV11/Kk3/cout1)
LUT3:I0->O	3	0.648	0.563	VV11/Kk3/K2/GC1/G1 (VV11/Kk3/K2/q<1>)
LUT3:I2->O	2	0.648	0.590	VV11/Kk3/K2/GC5/G1 (VV11/Kk3/K2/s<5>)
LUT4:I0->O	1	0.648	0.423	VV11/Kk3/K2/GC13/G_and0000_SW0 (N613)
LUT4:I3->O	1	0.648	0.452	VV11/Kk3/K2/GC13/G_and0000 (VV11/Kk3/K2/GC1
LUT4:I2->O	1	0.648	0.420	out<62> (out_62_OBUF)
OBUF:I->O		4.520		out_62_OBUF (out<62>)
Total		70.646ns (40.539ns logic, 30.107ns route) (57.4% logic, 42.6% route)		

Figure 4. DELAY REPORT

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2403	5888	40%
Number of 4 input LUTs	4242	11776	36%
Number of bonded IOBs	135	372	36%

Figure 5. DESIGN SUMMARY

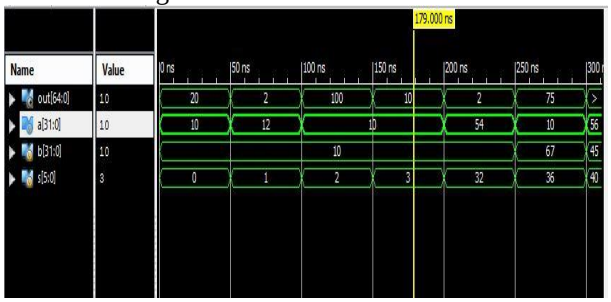

Figure 6. ALU OUTPUT

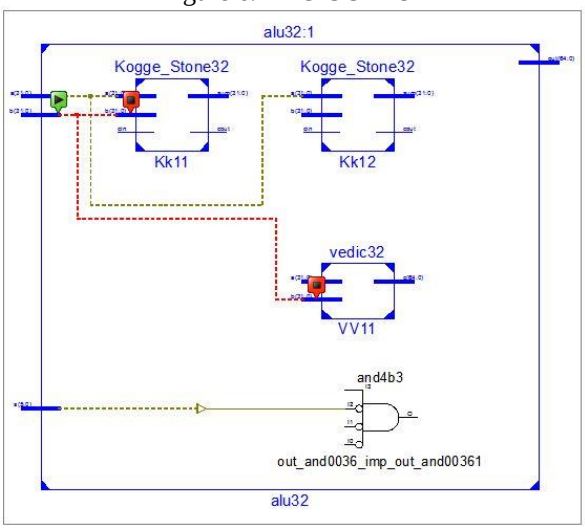

Figure 7. RTL SCHEMATIC

V. CONCLUSION

Through this paper, the authors have presented an extremely effective method of multiplication, i.e. UrdhvaTiryakbhyam Sutra based on Vedic mathematics. With this method, the multiplier of any number of bits can be designed, and show the computational benefits given by Vedic methods. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. Since the objective was to reduce the delay, the computational path delay for the proposed 32x32 bit Vedic Wallace multiplier is found to be 54.004ns. The Vedic Wallace multiplier is much more efficient than Vedic multiplier and Array multiplier in terms of execution time (speed) and Area Delay Product. So we can say Vedic mathematics can be included in the education systems and help students learn mathematics fast and perform better in less time. In future, all the research centers are to promote research works in Vedic mathematics.

VI. REFERENCES

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