A PASSIVE 2ND-ORDER SIGMA-DELTA MODULATOR FOR LOW-POWER ANALOG-TO-DIGITAL CONVERSION

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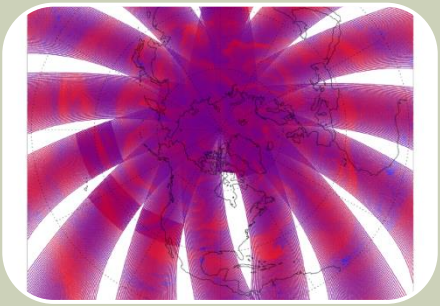
A BRIEF ROADMAP

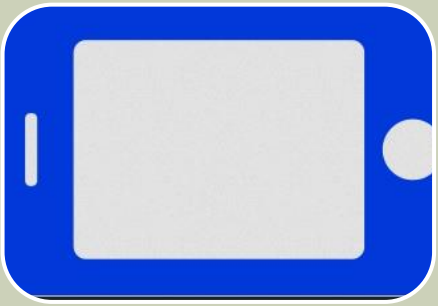
- Need for Low Power ∑-Δ ADCs
- Review of Basic ∑-Δ Modulator Topologies
- Proposed ∑-Δ Modulator Topology
- Circuit Design and Layout
- Test Results

MARKET NEED FOR LOW POWER ∑-Δ ADCS



Remote Sensing

Internet of Things



Mobile Devices

All these future devices and trends require low cost, low power ADCs.
High resolution and precision are not prioritized.
Passive ∑-Δ ADCs can meet this need.

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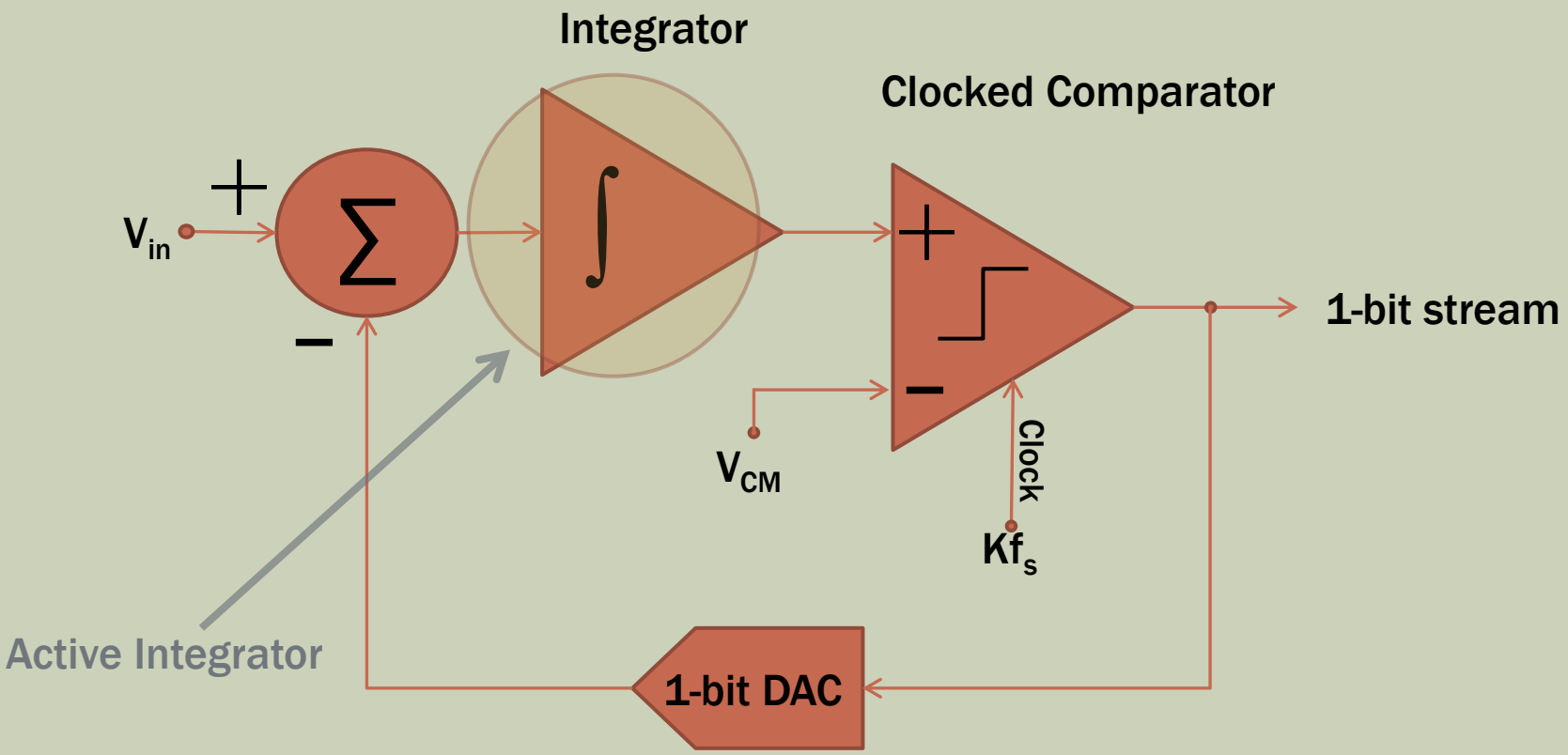
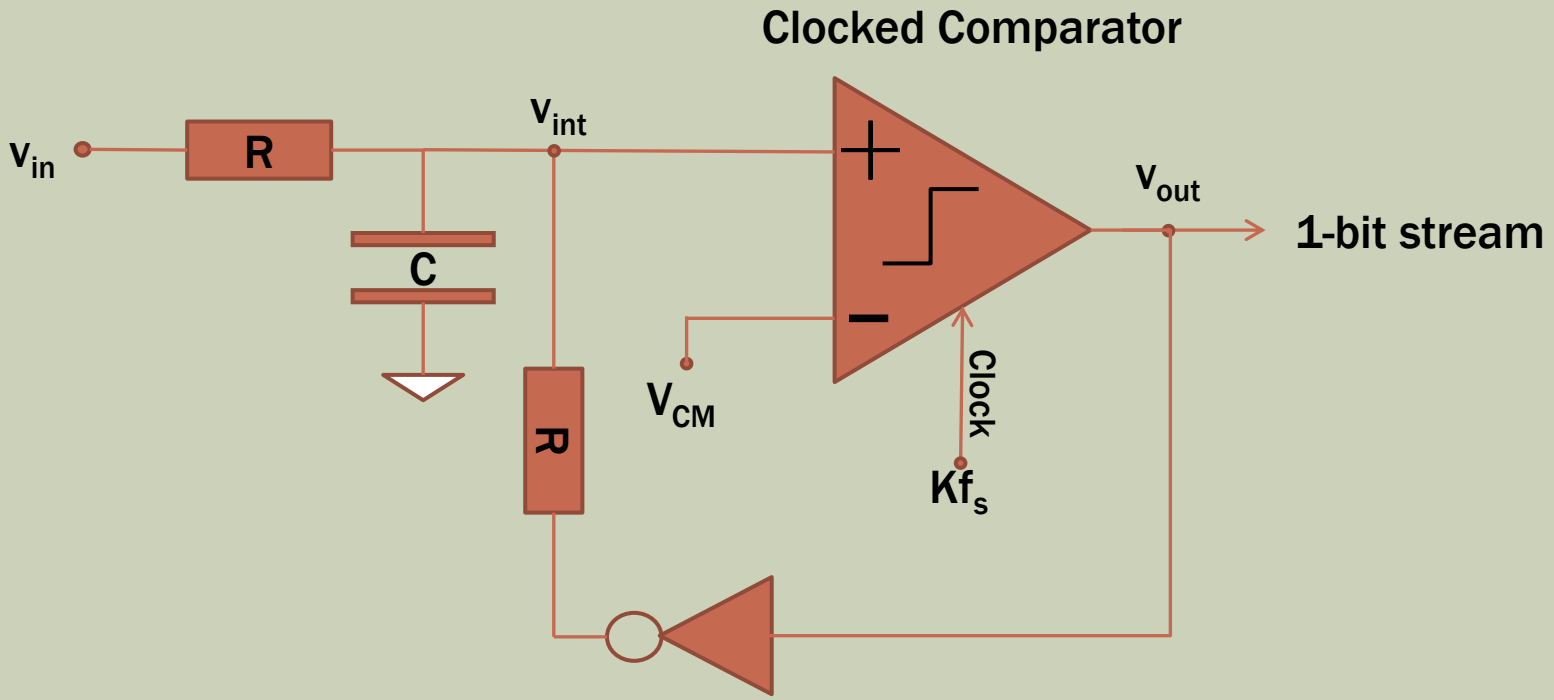
REVIEW OF BASIC 1ST ORDER ∑-Δ MODULATORS



Generally, ∑-Δ modulators use an active integrator to keep the voltage swing on the integrator's input to a minimum (ideally zero).

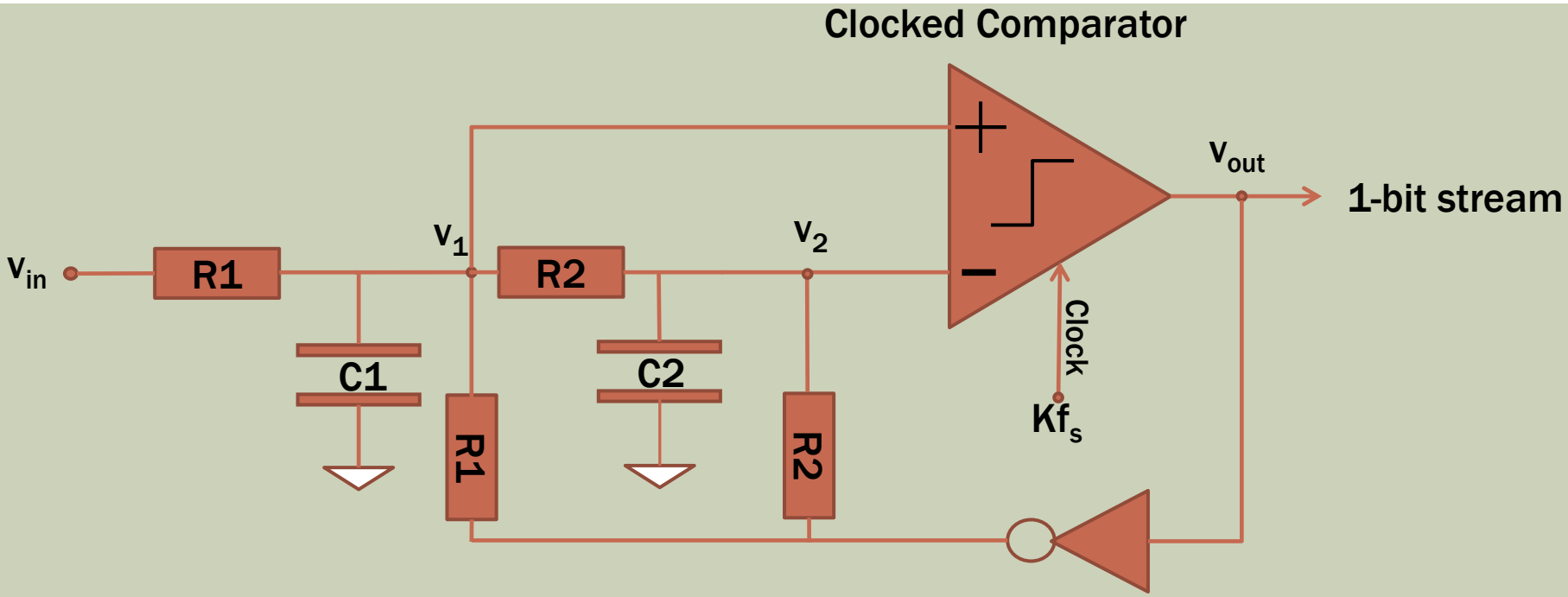
1ST ORDER PASSIVE ∑-Δ MODULATOR



STF NTF DT (distortion term)

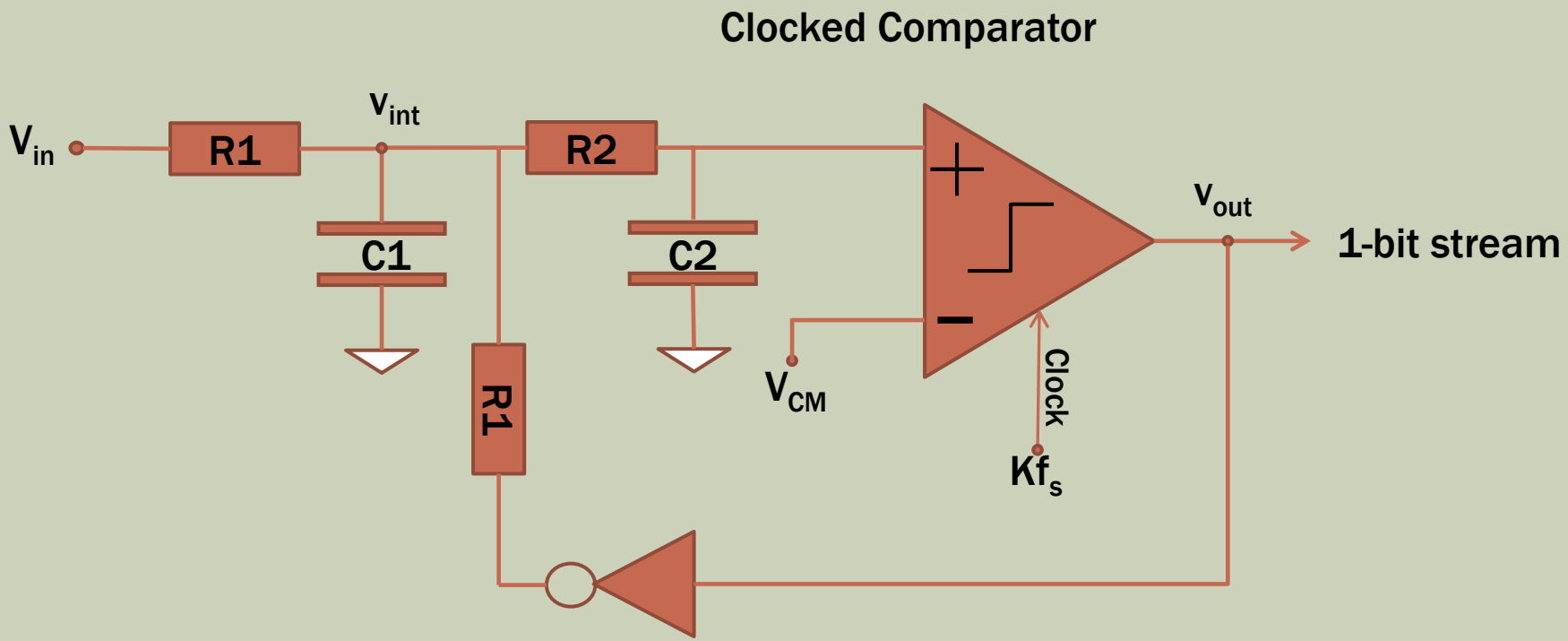
$$v_{out} = \overbrace{\frac{1}{1+sRC}}^{\text{STF}} \cdot v_{in} + \overbrace{\frac{sRC}{1+sRC}}^{\text{NTF}} \cdot V_{Qe} + \overbrace{\frac{-2}{1+sRC}}^{\text{DT}} \cdot v_{int}$$

CONVENTIONAL 2ND ORDER PASSIVE ∑-Δ MODULATOR



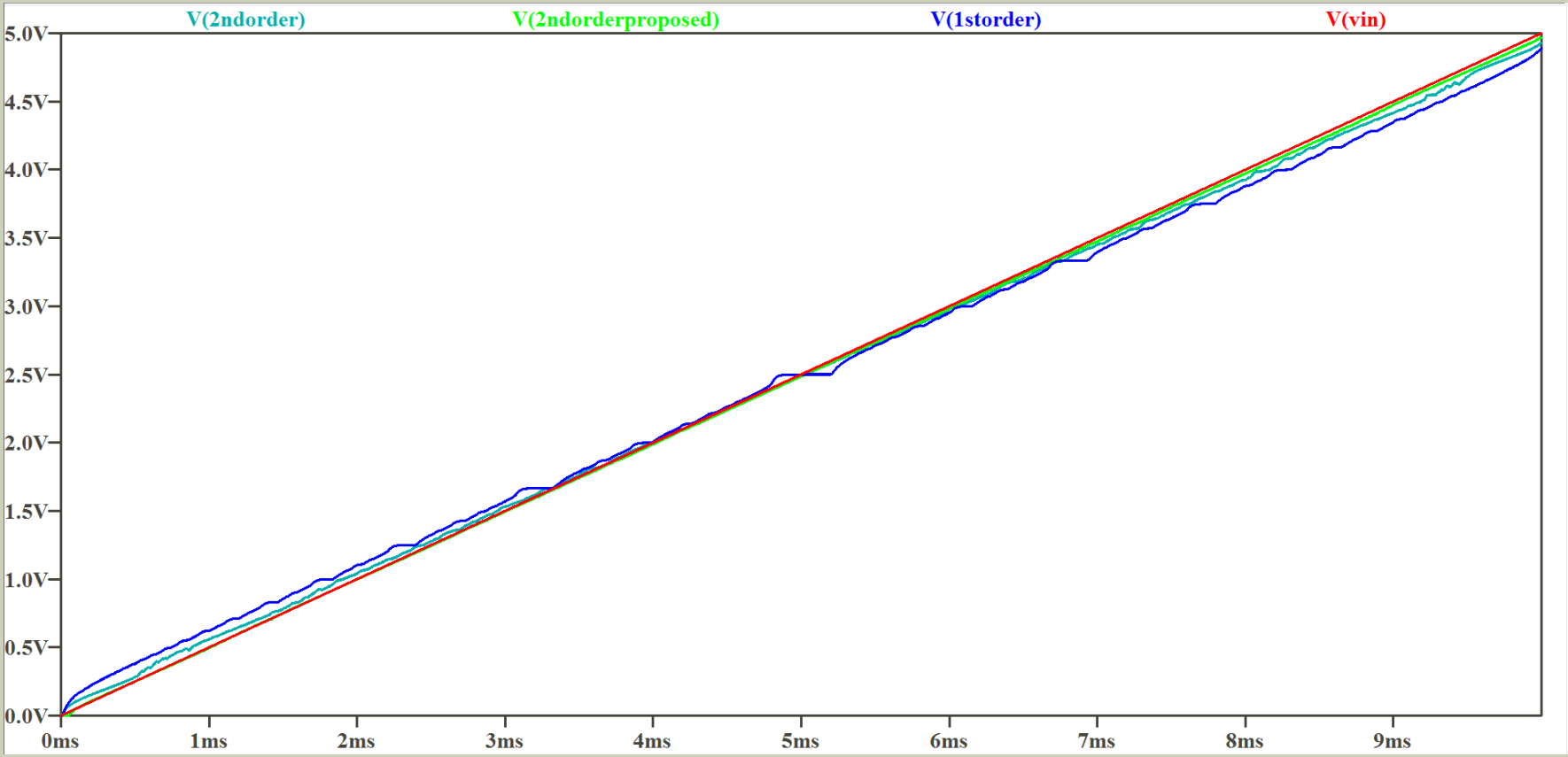
$$v_{out}{}^2 = \overbrace{\frac{1}{1+(\omega RC)^2}}^{\text{STF}} \cdot v_{in}{}^2 + \overbrace{\frac{(\omega RC)^2}{1+(\omega RC)^2}}^{\text{NTF}} \cdot \frac{V_{Qe}{}^2}{2} + \overbrace{\frac{2v_1 + v_2}{1+(\omega RC)^2}}^{\text{DT (distortion term)}}$$

PROPOSED 2ND ORDER MODULATOR



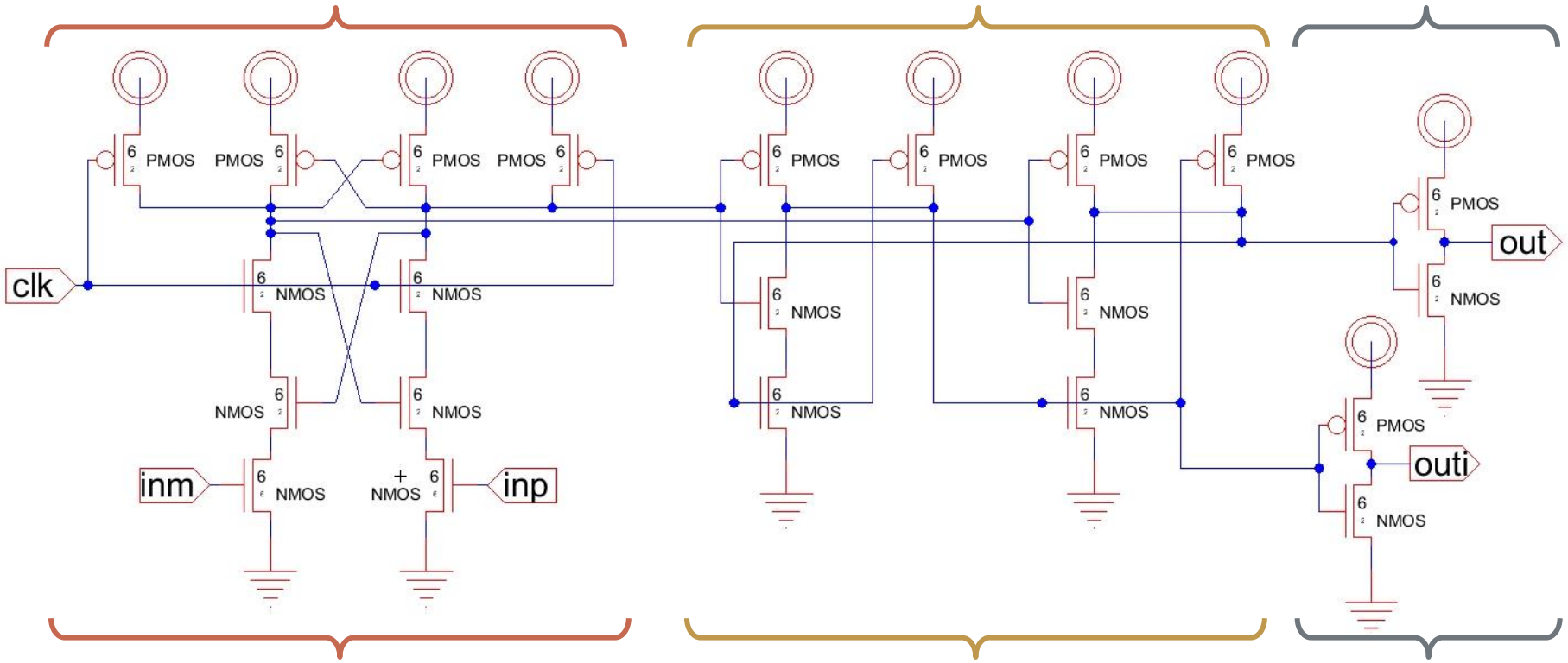
$$v_{out} = \overbrace{\frac{1 + sR_2C_2}{1 + sR_2C_2 + sR_1C_1}}^{\text{STF}} \cdot v_{in} + \overbrace{\frac{s(sR_1C_1R_2C_2 + R_1C_1)}{1 + sR_1C_1 + s^2R_1C_1R_2C_2}}^{\text{NTF}} \cdot V_{Qe} + \overbrace{\frac{1}{1 + sR_1C_1 + (1 + sR_2C_2)}}^{\text{DT (distortion term)}} \cdot v_{int}$$

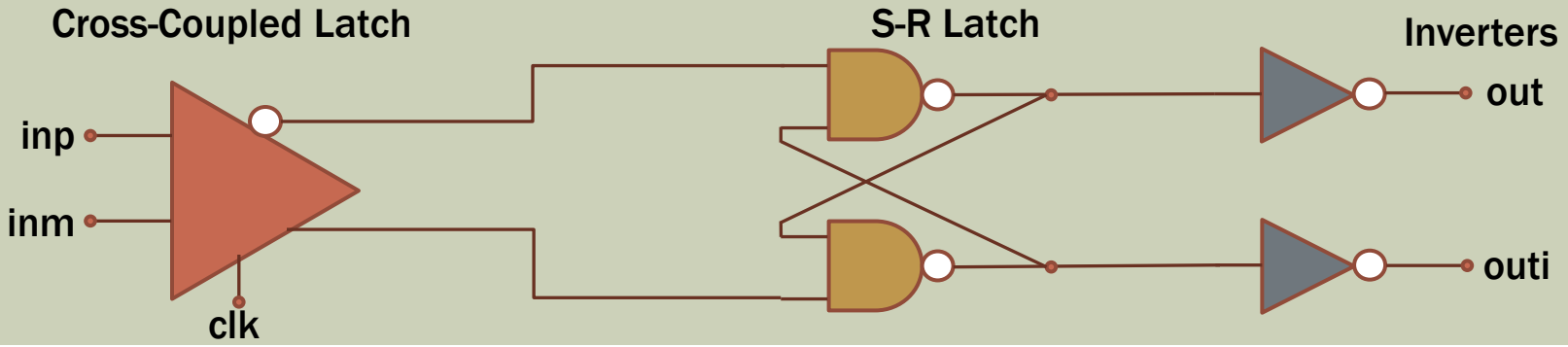
SPICE SIMULATION WITH IDEAL COMPONENTS



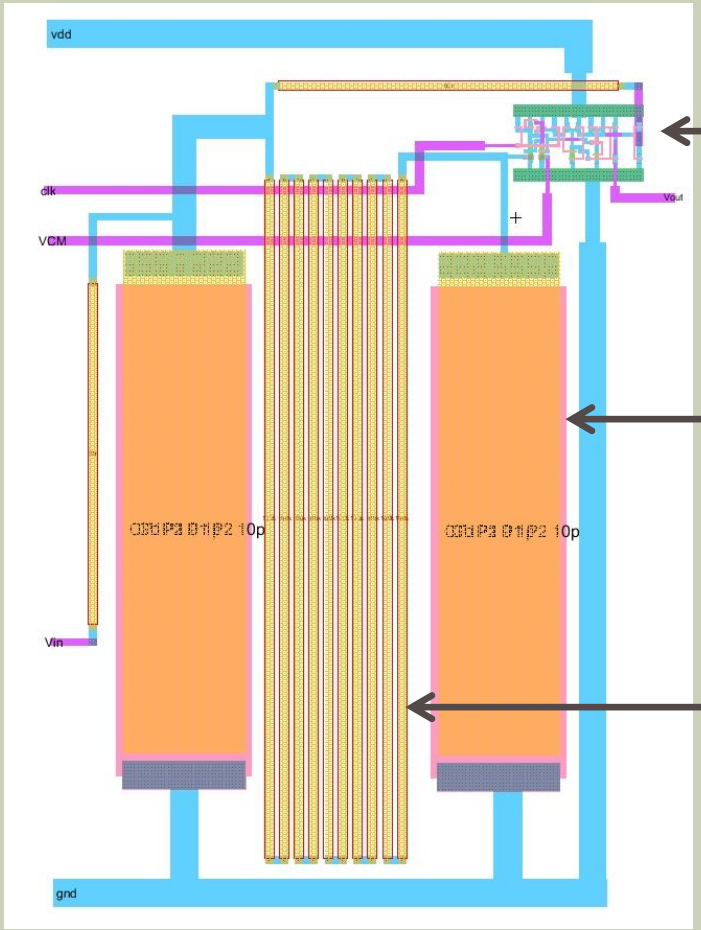
Linearity Comparison of ∑-Δ Modulator Topologies with a 10mS 0-5V Ramp Input

LOW POWER COMPARATOR DESIGN





CHIP LAYOUT



400 µm

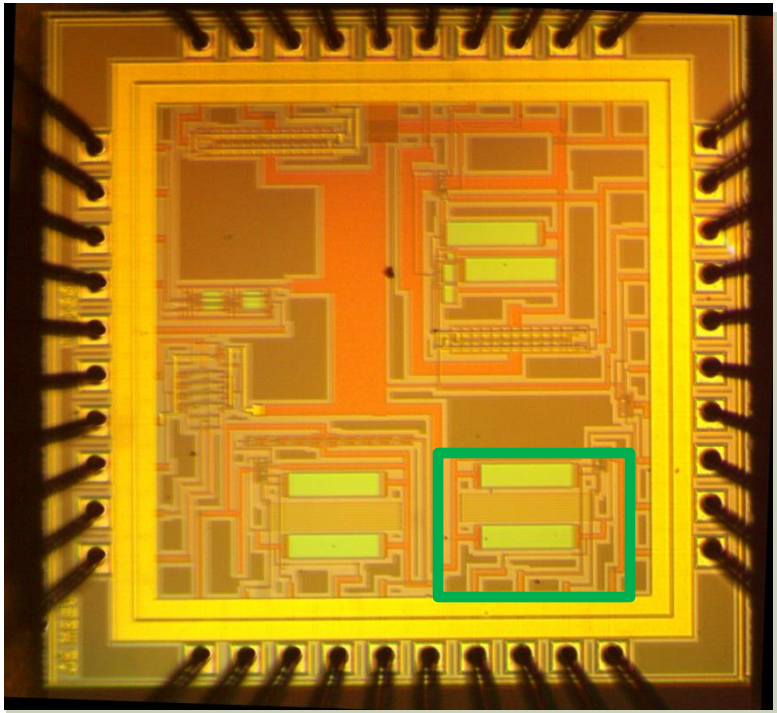
270 µm

Low Power Comparator With Minimum Size Devices

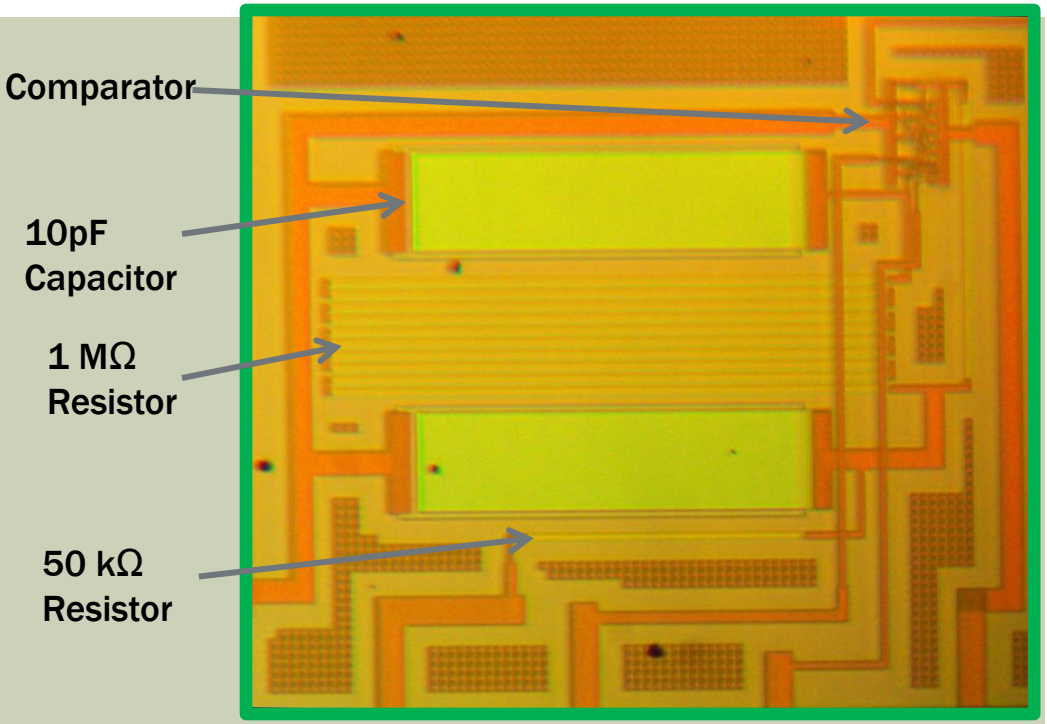
Poly1-Poly2 Capacitor

High Resistivity Poly2 Resistor

CHIP MICROGRAPHS

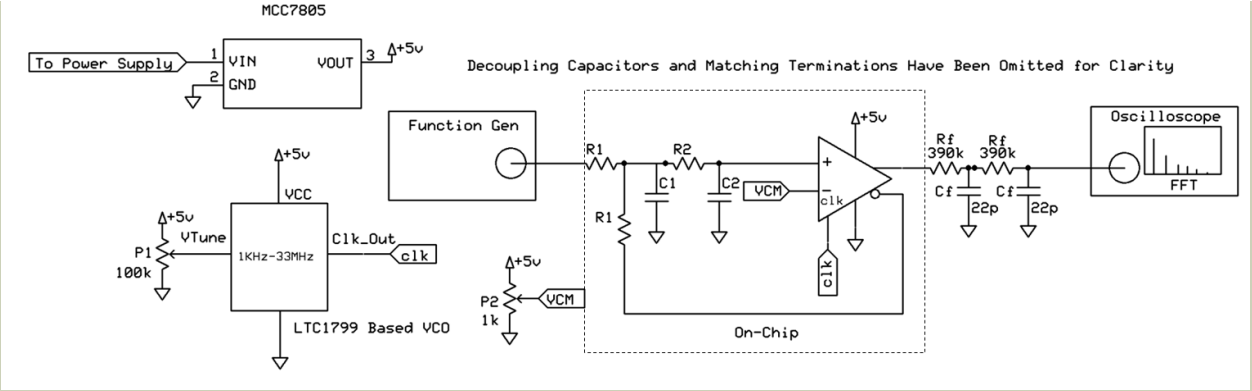


Micrograph of Entire Chip
Area = 1.5 mm^2
Proposed Modulator in Green

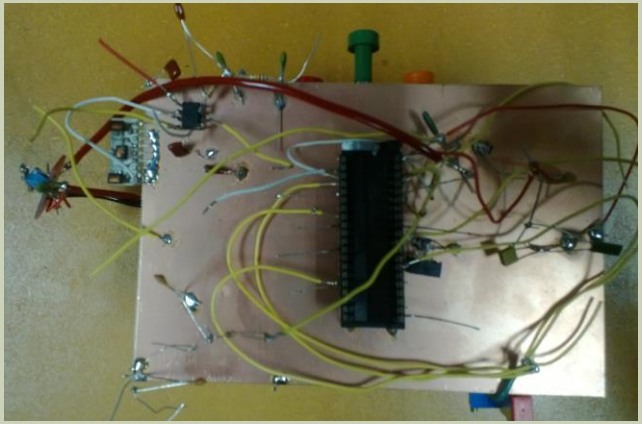


Micrograph of Proposed Modulator
Area in View ≈ 400 μm^2

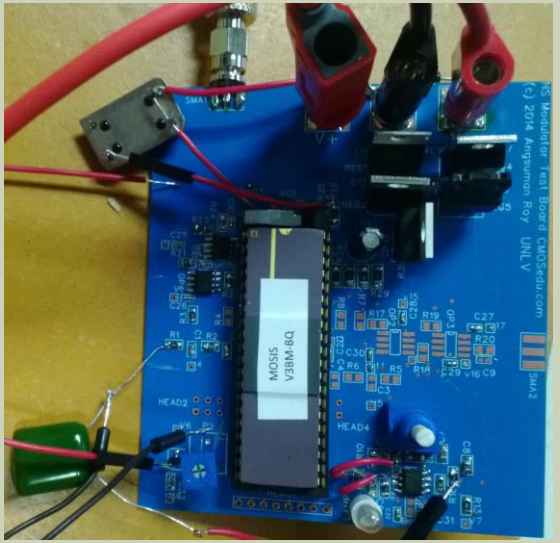
TEST CIRCUIT



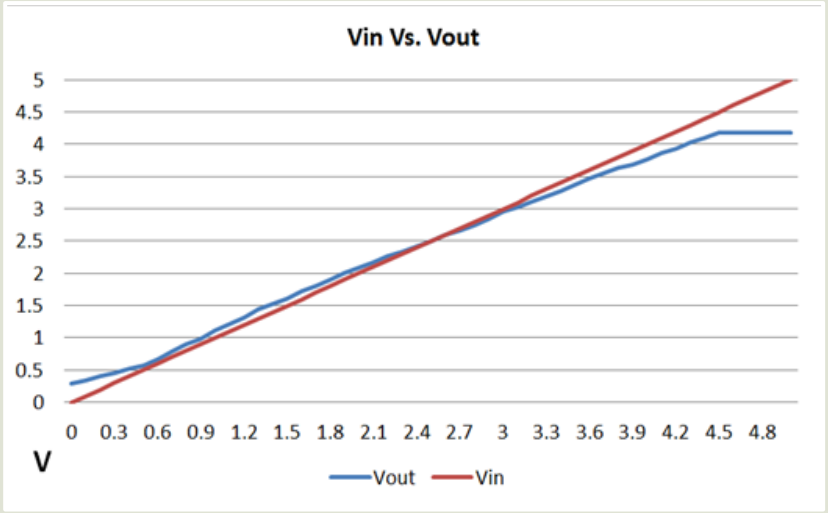
"Dead-bug" Test Set-up



PCB Test Set-up

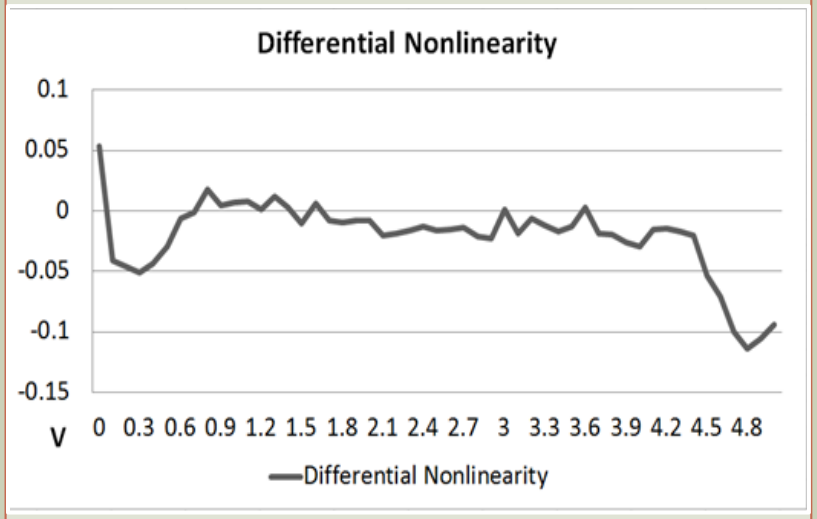


MEASURED DC TEST RESULTS



DC Transfer

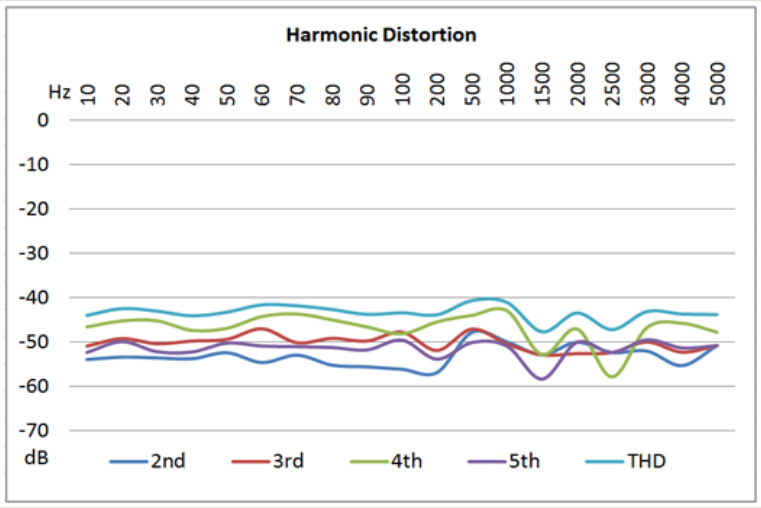
Input and output voltages were compared using a 6.5 digit multimeter.



% Differential Nonlinearity

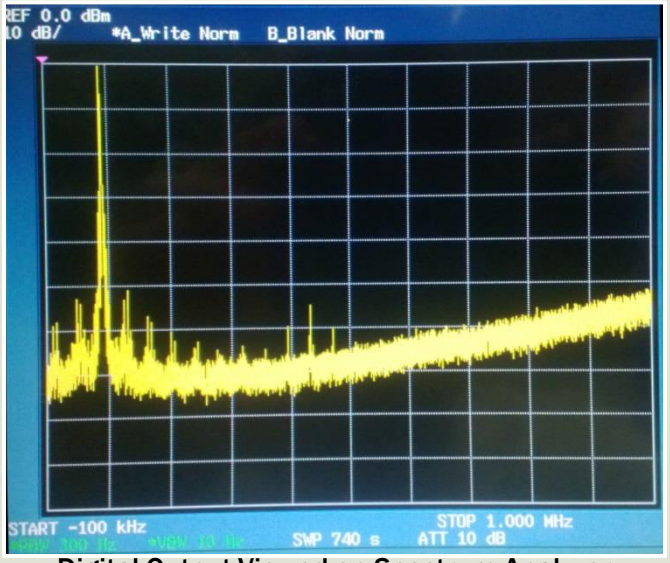
Significant filtering was used to make the output nearly static. DNL was calculated by dividing the measured incremental change by the ideal incremental change between data points.

MEASURED AC TEST RESULTS



Harmonic Distortion (dB Below Fundamental)

Result measured using 8-bit oscilloscope FFT function. This limits SNR to around 50 dB.



Digital Output Viewed on Spectrum Analyzer

Unfiltered digital output with 1kHz sine input. The spuriae free dynamic range is 50dB.

The noise shaping is clearly visible.

COMPARISONS TO OTHER WORKS

Parameter	2nd Order Passive ∑-Δ Modulator in This Work (Measured)	2nd Order Active ∑-Δ Modulator in [5] (Simulated)	2nd Order Passive∑-Δ Modulator in [2] (Simulated)
Process	500 nm	350 nm	350 nm
Resolution (ENOB)	8-bit	12-bit	10-bit
Power Consumption	100µW (typical) @5V VCC	120 µW @2V VCC	50 µW @3.3V VCC
Signal Bandwidth	5 kHz	1 kHz	4 kHz
Clock Frequency	10 MHz	320 kHz	1 MHz

[2] Guessab, S., P. Benabes, and R. Kielbasa. "Passive Delta-Sigma Modulator for Low-Power Applications," *MWSCAS '04*. (2004): 295-298.

[5] Gundel, Adnan, and Carr, William N. "A Micro Power Sigma-Delta A/D Converter in 0.35µm CMOS for Low Frequency Applications," *LISAT 2007*. (2007): 1-7.

CONCLUSIONS

Measurement Quality Limited by Test Equipment

Promising Topology for Low Power Applications

Proposed Topology Should Scale Well Down to nm CMOS

Future Work Will Include More Detailed Comparisons Between Passive Topologies

Future Work Will Attempt to Optimize Components to Increase ENOB