Intend and Analysis of Configurable Multipliers using Dual Quality 4:2 Compressors

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Abstract- Multiplier plays a vital role in many applications such as digital image processing, digital signal processing etc…so it is important to design the multiplier with low power consumption and reduced delay. In order to reduce this factor we design the multiplier using four 4:2 compressor and these compressors has a dual quality property and this property is used to switch between the exact and approximate modes. When it operates at approximate mode it reduces the power consumption and area at the cost of low accuracy. During approximate and exact mode each of these compressors has different power consumption and delays but only at approximate mode these compressors has its own level of accuracy. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors in a 32-bit Dadda multiplier are evaluated in a 45-nm standard CMOS technology by comparing their parameters with those of the state-of-the-art approximate multipliers. The results of comparison indicate, on average, 46% and 68% lower delay and power consumption in the approximate mode. Also, the effectiveness of these compressors is assessed in some image processing applications. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Keywords- 4:2 compressors, dada multiplier, CMOS, Error, Logic size, speed & power.

I. INTRODUCTION

The most commonly used techniques for the generation of approximate arithmetic circuits are truncation, voltage over scaling (VOS) and simplification of logic .Extensive research has been conducted on approximate address providing significant gains in terms of area and power while exposing small error. Approximate hardware circuits, contrary to software approximations, offer transistors reduction, lower dynamic and leakage power, lower circuit delay, and opportunity for downsizing. Motivated by the limited research on approximate multipliers, compared with the extensive research on approximate adders, and explicitly the lack of approximate techniques targeting the partial product generation, we introduce the partial product perforation method for creating approximate multipliers. We omit the generation of some partial products, thus reducing the number of partial products that have to be accumulated; we decrease the area, power, and depth of the accumulation tree. By reducing the quality (accuracy), the delay and/or power consumption of the unit may be reduced. In addition, some digital systems, such as general purpose processors, may be utilized for both approximate and exact computation modes [4]. An approach for achieving this feature is to use an approximate unit along with a corresponding correction unit. The correction unit, however, increases the delay, power, and area overhead of the circuit. Also, the error correction procedure may require more than one clock cycle, which could, in turn, slow down the processing further. Parallel multipliers are utilized in superior applications wherever their large power consumptions could produce hot-spot locations on the die [3]. Since the power consumption and speed are crucial parameters within the style of digital circuits, the optimizations of these parameters for multipliers become critically vital. Very often, the improvement of one parameter is performed considering a constraint for the opposite parameter. Specifically, achieving the specified performance (speed) considering the limited power budget of transportable systems is difficult task. In addition, having a given level of reliability may be another obstacle in reaching the system target performance. An approach for achieving this feature is to use an approximate unit alongside a corresponding correction unit. The correction unit, however, will increase the delay, power, and space overhead of the circuit. Also, the error correction procedure could need more than one clock cycle (see [9]), that might, in turn, slow down the process additional. In this paper, we have a tendency to propose four dual-quality reconfigurable approximate 4:2 compressors, which give the flexibility of switching between the precise (Exact) and approximate operative modes during the runtime. The compressors are also utilized within the architectures of dynamic quality configurable parallel multipliers. The fundamental structures of the projected compressors consist of 2 components of approximate and supplementary. In the approximate mode, solely the approximate half is active whereas in the actual operative mode, the supplementary half alongside some parts of the approximate half is invoked.

II. RELATED STUDY

While there are several works in coming up with approximate multipliers, the analysis efforts on accuracy configurable approximate multipliers are restricted. During this section, we review some of these works. In [1], a static section methodology (SSM) is given, that performs the multiplication operation on an mbit section ranging from the leading one little bit of the input operands wherever m is adequate to or bigger than n/2.Hence, an m × m multiplier consumes a lot of less energy than other multiplier. Also, a dynamic vary un

biased multiplier (DRUM) multiplier, that selects an mbit section, starting from the leading one little bit of the input operands, and sets the least important little bit of the truncated values to "1," has been proposed. During this structure, the truncated values are multiplied and shifted to the left to come up with the ultimate output. Although, by exploiting smaller values for m, the structure of [1] provides higher accuracy styles than those of [1], its approach needs utilizing additional complicated electronic equipment.

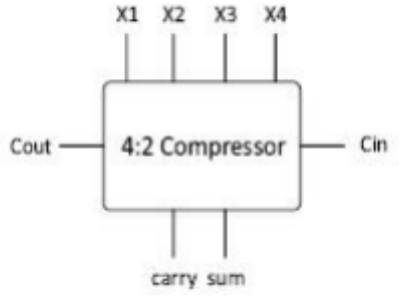

Fig.1: Design of 4:2 compressor.

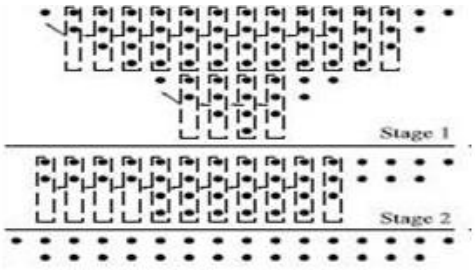

Fig.2: Dot diagram for an multiplier using exact 4:2 compressor.

A bio inspired approximate multiplier, called broken array multiplier, has been proposed. In this structure, some carry save adder cells, in both vertical and horizontal directions during the summation of the partial products, have been omitted to save the power and area and reduce the delay. Two approximate 4:2 compressors have been proposed and utilized in Dadda multiplier. The proposed compressors only operated in the approximate mode. By modifying the Karnaugh map of a 2×2 multiplier (omitting one term in the Karnaugh map), an approximate 2×2 multiplier with a simpler structure has been proposed. This block may be used for constructing larger multipliers. Also, in this paper, an error detection and correction (EDC) circuit has been proposed. An inaccurate multiplier design strategy based on redesigning the multiplier into two multiplication and non-multiplication parts was introduced. The multiplication part was constructed based on the conventional multipliers while then on-multiplication part was implemented in an approximate structure with a specified value of error. It should be noted that both of the approaches presented suffer from high relative errors.

III. AN OVERVIEW OF PROPOSED SYSTEM

We present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked. The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown in Fig. 3. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from Fig. 3, in the exact operating mode, tri-state buffers are utilized to disconnect the outputs of the approximate part from the primary outputs.

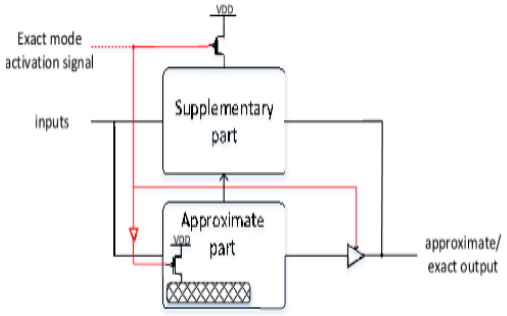

Fig.3: proposed system model.

Structure 1 (DQ4:2C1):For the approximate part of the first proposed DQ4:2C structure, as shown in Fig. 4(a), the approximate output carry (i.e., carry') is directly connected to the input x4(carry'=x4), and also, in a similar approach, the approximate output sum (i.e., sum') is directly connected toinputx1 (sum'=x1). In the approximate part of this structure, the output Cout is ignored. While the approximate part of this structure is considerably fast and low power, its error rate is large (62.5%).

The supplementary part of this structure is an exact4:2 compressor. The overall structure of the proposed structure is shown in Fig. 4(b). In the exact operating mode, thedelay of this structure is about the same as that of the exact4:2 compressor. 2) Structure 2 (DQ4:2C2): In the first structure, while ignoring Cout simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C1, the output

Cout is generated by connecting it directly to the input x3 in the approximate part. Fig. 5 shows the internal structure of the approximate part and the overall structure of DQ4:2C2. While the error rate of this structure is the same as that of DQ4:2C1,namely, 62.5%, its relative error is lower.

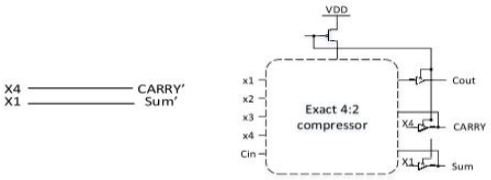

Fig.4: Carry and sum indication.

The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Fig. In this structure, the accuracy of output sum' is increased. Similar to DQ4:2C1, the approximate part of this structure does not support output Cout. The error rate of this structure, however, is reduced to 50%.

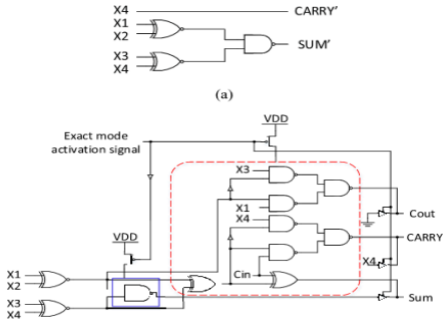

Fig.5: Approximate part of DQ4:2C3 and (b) overall structure of DQ4:2C3.

When multiplying A × B, the imposed error is proportional to the multiplicand A and the term xB and thus decreasing one of these operands decreases the error delivered to the output. As a result, comparing A and B or xA and xB before the multiplication and swapping accordingly, A and B can reduce the error.

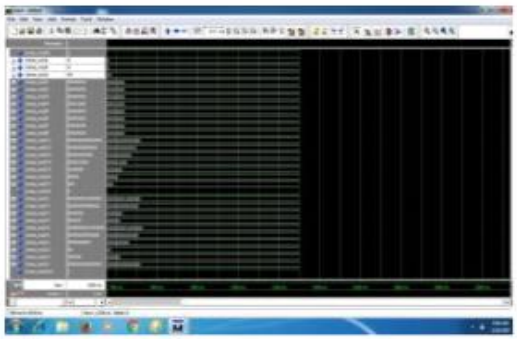

Fig.7: approximate multiplier using dual quality for 4:2 compressor.

IV. CONCLUSION

In this paper we presented four DQ4:2Cs, which had the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these compressors provided higher speeds and lower power consumption at the cost of lower accuracy .each of these compressors had its own level of accuracy in the approximate mode as well as different delays and power in the approximate and exact modes. These compressors were employed in the structure of 32 bit Dadda multiplier to provide a configurable multiplier whose accuracy (as well as its power and speed) could be changed dynamically during the runtime.

V. REFERENCES

[1]. Omid Akbari, Mehid Kamal, Ali Afzail-Kusha, and Massoud Pedram,"dual quality 4:2 compressors for utilizing in dynamic accuracy configurable multipliers",IEEE Trans. Very large scale integr. (VLSI) Syst., vol:pp,issue99,jan 2017.

[2]. P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in Proc. 24th Int. Conf. VLSI Design, Jan. 2011, pp. 346–351.

[3]. D. Baran, M. Aktan, and V. G. Oklobdzija, "Multiplier structures for low power applications in deep-CMOS," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2011, pp. 1061–1064.

[4]. S. Ghosh, D. Mohapatra, G. Karakonstantis, and K. Roy, "Voltage scalable high-speed robust hybrid arithmetic units using adaptive clocking," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 9, pp. 1301–1309, Sep. 2010

[5]. Pedram, "RAP-CLA: A reconfigurable approximate carry look-ahead adder," IEEE Trans. Circuits Syst. II, Express Briefs, doi: 10.1109/TCSII.2016.2633307.

[6]. A.Raha, H. Jayakumar, and V. Raghunathan, "Inputbased dynamic reconfiguration of approximate arithmetic units for video encoding," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 3, pp. 846–857, May 2015.

[7]. J. Joven et al., "QoS-driven reconfigurable parallel computing for NoC-based clustered MPSoCs," IEEE Trans. Ind. Informat., vol. 9, no. 3, pp. 1613–1624, Aug. 2013.

[8]. M. Shafique, W. Ahmad, R. Hafiz, and J. Henkel, "A low latency generic accuracy configurable adder," in Proc. 52nd ACM/EDAC/IEEE Design Autom. Conf. (DAC), Jun. 2015, pp. 1–6.

[9]. Narayanamoorthy, H. A. Moghaddam, Z. Liu, T. Park, and N. S. Kim, "Energy-efficient approximate multiplication for digital signal processing and classification applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1180–1184, Jun. 2015.

[10]. S. Hashemi, R. I. Bahar, and S. Reda, "DRUM: A dynamic range unbiased multiplier for approximate applications," in Proc. IEEE/ACM Int. Conf. Comput.- Aided Design (ICCAD), Austin, TX, USA, Nov. 2015, pp. 418–425.

[11]. K. Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low-power high-speed multiplier for error-tolerant application," in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC), Dec. 2010, pp. 1–4.