High Speed and Low Power SRAM Circuit based on Adiabatic and Transmission Gate Logic

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Abstract **-** In this paper, we propose a high speed, low power dissipation, low average power consumption and low PDP (Power Delay Product) based SRAM cell. SRAM cell play an important role in storage devices and hence it is necessary to produce a better design for the optimal use in the portable devices. The MOSFET based conventional 6 T SRAM has high power and delay product with high short channel effects in 32nm technology. Hence, a solution is provided by the use of adiabatic logic and transmission gate logic. In this technique, we use a transistor between Vdd and Virtual Vdd to improve the characteristics, it shows that Average power is decreased by 94.75%, delay is improved by 87.15%, power dissipation is improved by 88.78% and energy is decreased by 99.19% in adiabatic proposed circuit when compared to adiabatic FinFET based circuit and similarly the improvements in transmission gate based proposed circuit from simple transmission gate FinFET SRAM is improved by 55.24%, 50.28%, 68.63% and 75% on basis of Average Power, Delay, Power Dissipation and Energy. The proposed circuits are of 8 Transistors.

Keywords **-** SRAM, adiabatic, FinFET, Transmission gat

I. INTRODUCTION

Memory cells assume a critical job regarding force, speed and execution in computerized circuits, for example, the System-on-Chips (So Cs), microchips and microcontrollers. These memory clusters possess impressive piece of the chip region. Consequently, these memories. Cells as a general rule contribute for a higher division of the chip control.[1][2] A few literary works have exhibited different designs for the SRAM cell, with their principle centre around decrease of the cell territory, diminished gadget include and decrease in the spillage control. The preference to optimize the layout metrics of overall performance, strength, area, fee, and time to market (opportunity cost) has now not changed for the reason that progress of the IC enterprise. In truth, Moore's law is all about optimizing those parameters.[3] however, as scaling of producing nodes progressed in the direction of 20-nm, some of the tool parameters couldn't be scaled any in addition, specifically the strength deliver voltage, the dominant component in figuring out dynamic electricity. This research is to lessen the power consumption and off currents at the FINFET based SRAM cell. The backend device Synopsys HSPICE is selected for the analysis of power dissipation and delay of SRAM. In this paper, four- enter SRAM is designed and simulated in 32 nm era the usage of FINFET technology. Simulation end result imply that the proposed technique offer improvement in term of strength consumption and delay over MOSFET. As nanometer technique technologies have advanced, chip density and running frequency have extended, making energy consumption in battery-operated portable gadgets a first-rate concern. Even for no portable devices, electricity consumption is critical because of the improved packaging and cooling expenses in addition to ability reliability issues. [4][5]Therefore, the principle design purpose for VLSI (very-large-scale integration) designers is to meet overall performance necessities within a power budget. Scaling of gate MOSFET in nm face exceptional assignment due to the extreme short channel effect that reason an exponential growth in the sub-threshold and gate –oxide leakage and DIBL.[7]-[11]

II. SIMULATION RESULTS

In this section, we propose the circuits for adiabatic and transmission gate logic based 9T SRAM cells. The circuit consists of one p type FinFET at VDD part of the base circuit. The circuit is controlled by the signal given in this circuit. The circuit is simulated in HSPICE Synopsys and the technology used 32nm.

Proposed Adiabatic based FINFET Circuit:

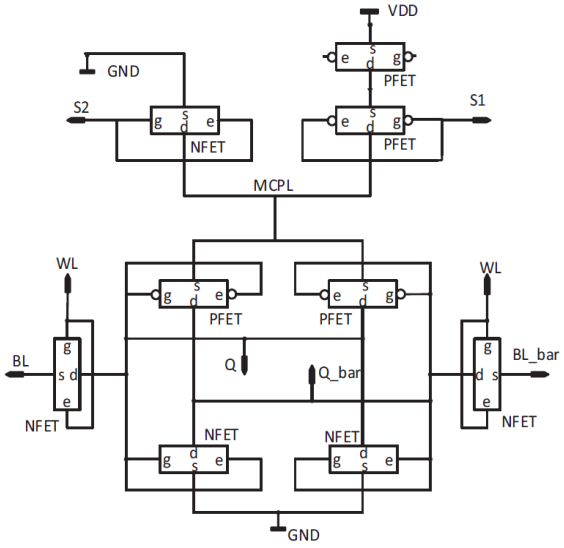

Figure 1: Proposed Adiabatic based SRAM cell FinFET

In the figure 1, the adiabatic logic is created by the use of MCPL logic, and also at Vdd an extra control transistor is added which decides when the circuit is on or off. The makes it in sleep or active mode.

Proposed Transmission Logic based FINFET Circuit:

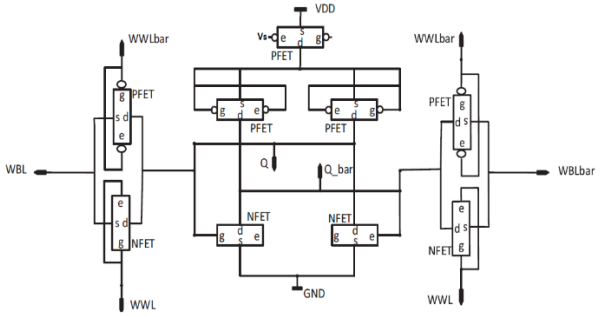

Figure 2: Transmission Gate Logic Proposed Circuit for SRAM

In the figure 2, the transmission gate logic is created by the use of two transistors at WBL and ABL bar, and also at Vdd an extra control transistor is added which decides when the circuit is on or off. The makes it in sleep or active mode.
The results of the performance parameters are shown in table 1 which clearly shows the enhancements in proposed circuits.

Table 1: Simulation Results

	SRAM adiabatic mos	SRAM adiabatic mos proposed	SRAM adiabatic fin	SRAM adiabatic fin proposed
Average Power	1.25E-07	1.04E-07	4.63E-09	2.43E-10
Delay	1.41E-07	1.41E-07	7.27E-11	9.34E-12
Power Dissipation	1.79E-07	1.06E-07	1.23E-11	1.38E-12
Energy	1.75E-14	1.46E-14	3.37E-19	2.27E-21
	sram TGL mos	sram TGL mos proposed	sram TGL fin	sram TGL fin proposed
Average Power	3.07E-08	7.08E-09	5.23E-12	2.55E-12
Delay	5.17E-11	3.33E-12	5.10E-11	2.60E-11
Power Dissipation	9.87E-08	8.57E-08	5.26E-12	1.65E-12
Energy	1.59E-18	2.36E-20	2.66E-22	6.65E-23

In figure 3 and Figure 4 shows the Average Power in Various circuits for adiabatic and transmission logic gate based. The proposed circuits shows better performance in Average Power Consumption.

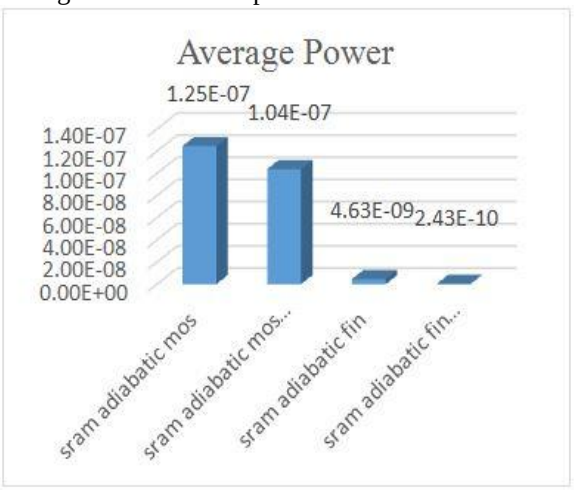

Figure 3: Average Power Consumption in Adiabatic SRAMs

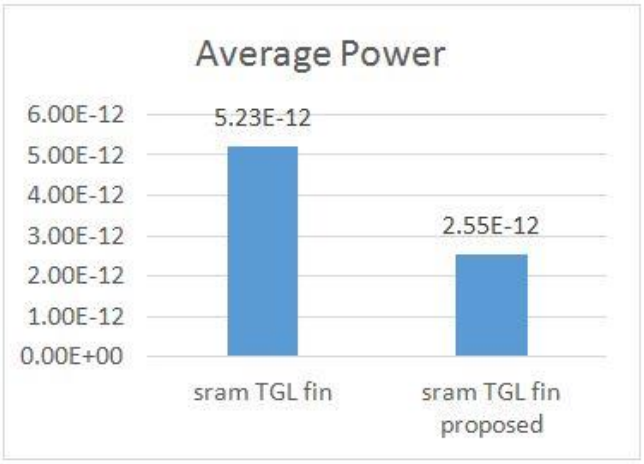

Figure 4: Average Power Consumption in TGL SRAMs

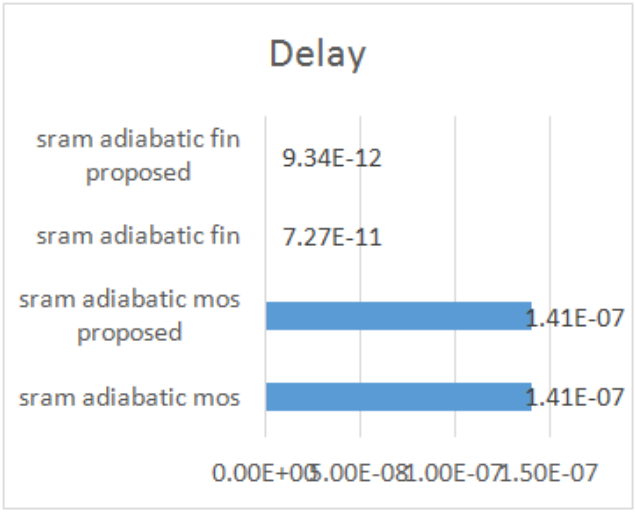

Figure 5: Delay in Adiabatic based Circuits

Figure 5 and Figure 6 shows the delay enhancements and Power dissipations enhancements in Adiabatic logic based circuits respectively.

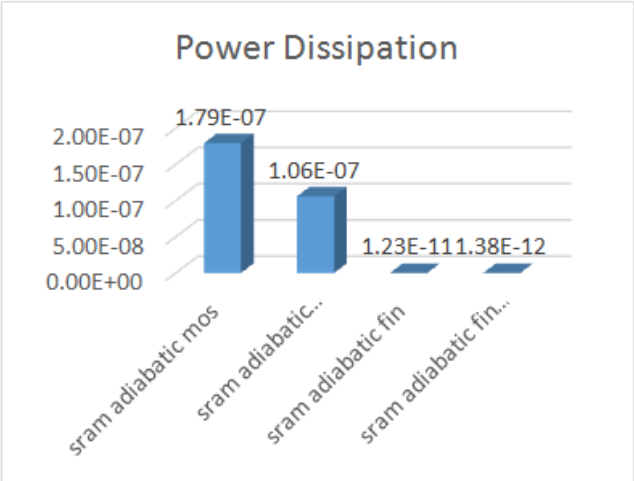

Figure 6: Power Dissipation in Adiabatic based Circuits

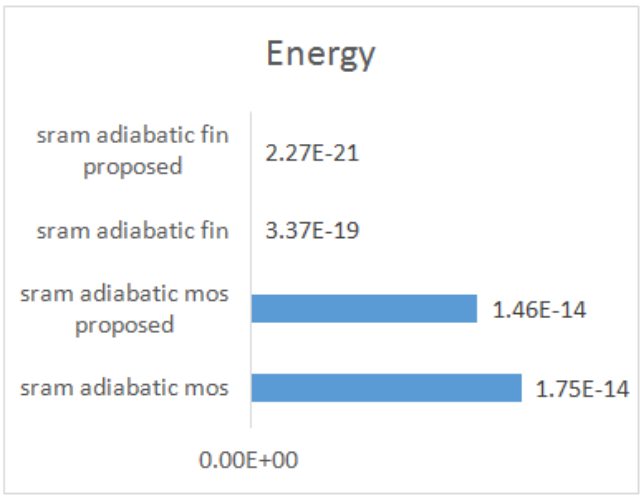

Figure 7: Energy in Adiabatic based Circuits

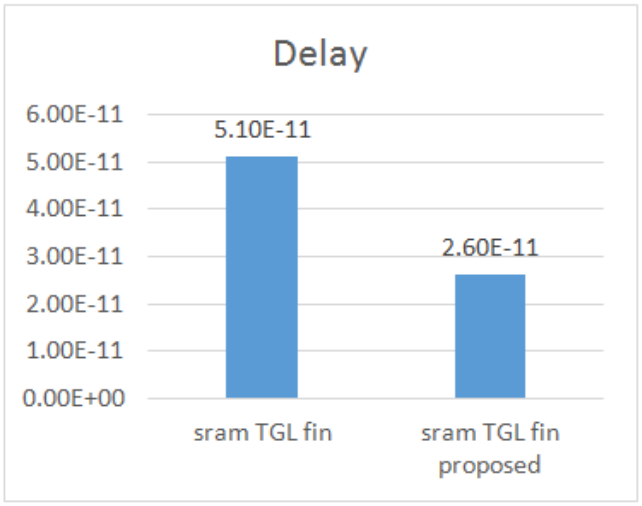

Figure 8: Delay in TGL based Circuits

Figure 7 and Figure 8 Energy in Adiabatic and Delay in transmission gate logic circuits in SRAM FinFET are represented.

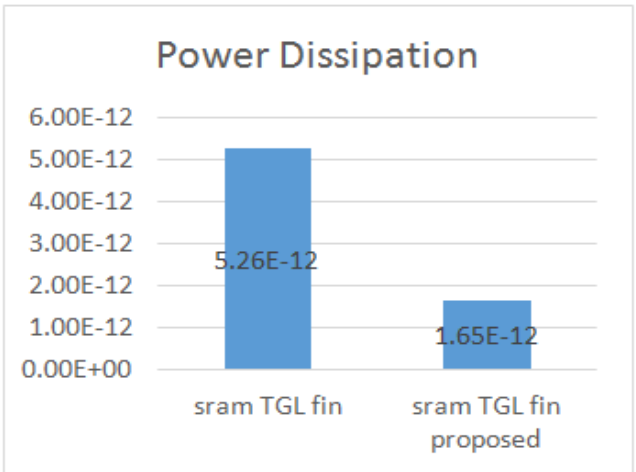

Figure 9: Power Dissipation in TGL based Circuits

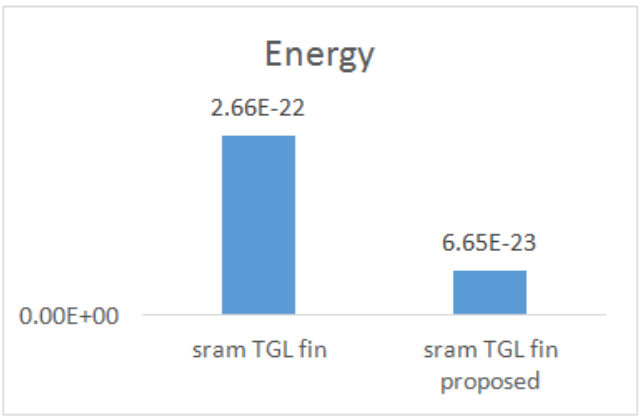

Figure 10: Energy in TGL based Circuits

Figure 9 and Figure 10 shows the Power Dissipation and Delay in TGL based circuits and shows that Proposed circuit is improved the performance.

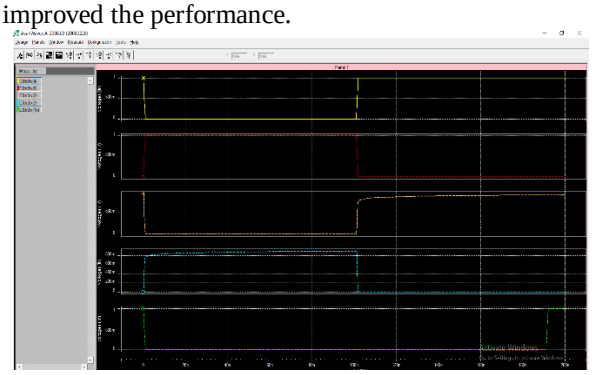

Figure 11: Waveform TGL

Figure 11 shows the waveforms for the TGL based circuits, the SRAM stores 0 and 1 efficiently.

Figure 12: Waveform Adiabatic based Circuits

Figure 12 shows the waveforms for the Adiabatic based circuits, the SRAM stores 0 and 1 efficiently.

III. CONCLUSION

Hence, we conclude that by use of transistor between VDD and the circuit virtual Vdd will improve the characteristics and performance of the circuit. The proposed circuit consists of 9T based FinFET. The improvement in the circuit are follows:

In adiabatic SRAM proposed circuit:

- Average power is decreased by 94.75%,
- delay is improved by 87.15%,
- power dissipation is improved by 88.78% and
- energy is decreased by 99.19%

In transmission gate based proposed circuit improvements are:

- 55.24% in Average Power
- 50.28% in Delay
- 68.63% in Power Dissipation
- 75% in Energy

IV. REFERENCES

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