A low power with high speed 8T SRAM cell design based on Transmission Gate

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Abstract— As per the latest technology, the size of transistor in modern VLSI system is shrinking day by day. And as it shrinks down; low supply voltage device with low power and high stability characteristic come into picture. Here we proposed a latest 8T SRAM cell at 90nm technology which consume very less power as compared to previous memory cells. This proposed design uses transmission gate to get low power leakage current. The simulation results of power dissipation, delay and power delay product of the proposed SRAM cell have been evaluated and it is compared with that of previous model of 8T SRAM cell. In the modified design, there is approx 76.42% reduction in power. The circuit is designed and simulated using a 90nm process with Tanner EDA tool.

Keywords— *SRAM, Low Voltage, High Speed, Low Power, Transmission Gate*

I. INTRODUCTION

In the era of latest technology, high speed and low power circuits are used in the portable device such as mobile, laptop, CPU etc. It requires high speed memory cell which can consume lesser power along with high speed and high signal to noise margin. In every VLSI based circuits, RAM memory is very important part for storage. But dynamic power dissipation and leakage current are the main concern for high speed SRAM cells because this suffers from unwanted power dissipation which reduces the battery backup life of portable devices. So the requirement of high speed and low power SRAM cell arises. In this paper, a low power with high speed 8T SRAM cell at 90 nm technology is proposed. A charge recycling technique is used to reduce the leakage currents and static power dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. The different performance parameters have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells. The paper is organized as follows: Section II discusses about other existing SRAM cells, Section III describes circuit design and working principle of the proposed 8T SRAM cell. Section IV describes the detailed analysis of the characteristics of the proposed cell and comparison with other SRAM cells and in the last, Section V conclusion is made and result is analyzed.

II. 8T SRAM CELL

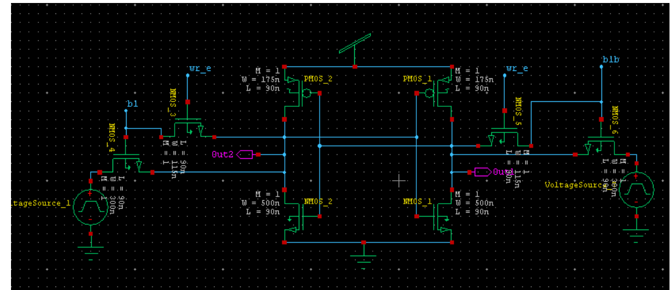

Fig.1 The 8T SRAM cell

In order to overcome the drawbacks associated with the conventional 6T SRAM, in this paper, we have modified the classical SRAM configuration. The proposed designed SRAM cell results in almost constant power dissipation even if the frequency increases. In the proposed design we are using two voltage sources VS1 and VS2 connected to the output of the bit and bit bar line. Two NMOS transistor VT1 and VT2 are connected with input of bit and bit bar line directly to switch ON and switch OFF the power source supply during write "0" and write "1" operations, respectively. The proposed design has been illustrated in Figure 1. These power supply sources reduce the voltage swing at the 'out' node when write operation is being performed.

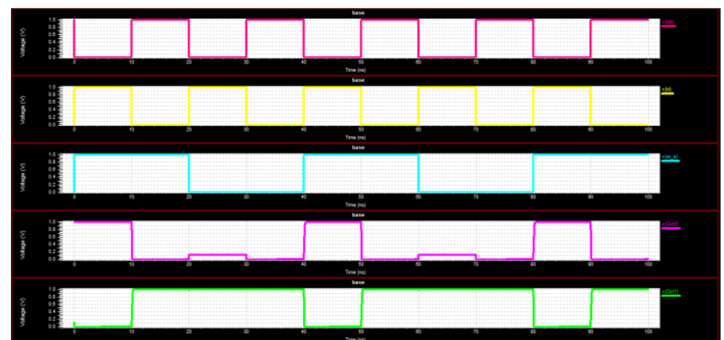

Fig.2 Simulation Diagram of the 8T SRAM cell.

III. Proposed 8T SRAM cell

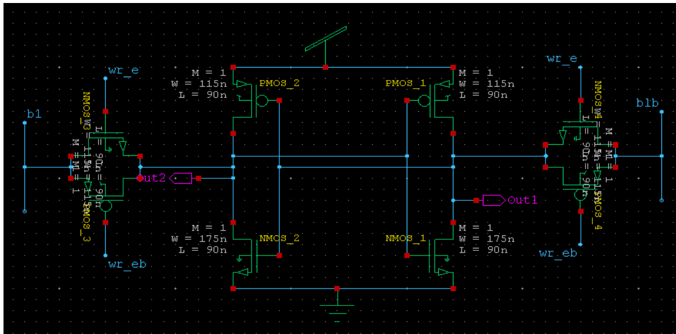

Fig.3 The proposed 8T SRAM cell.

The proposed 8T SRAM cell is illustrated in the figure 3 The conventional SRAM cells are associated with the problem of low static noise margin and high power dissipation. In order to overcome this problem associated with existing conventional SRAM cells, there proposes a transmission gate (TG) based 8T SRAM circuit to get low static and dynamic power dissipations for lower power dissipation, high speed and high stability. In the modified design there are two mosfets at the access transistor end connected as transmission gate configuration.

The transmission gate consists of one PMOS and one NMOS transistor connected end to end.It ensures the proper voltage level at a speedy rate.

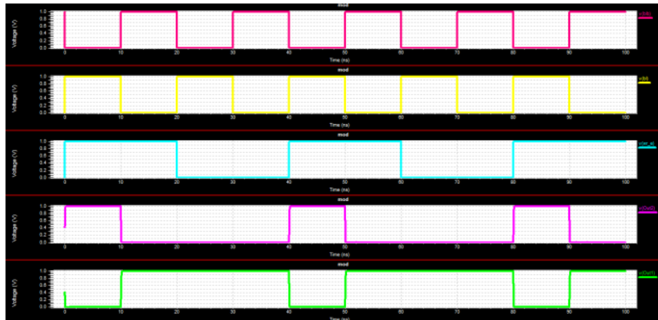

Fig.4 Simulation Diagram of the proposed 8T SRAM cell.

IV. RESULT AND CONCLUSION

A modified design is simulated using Tanner EDA Tool using 90nm technology at 1V supply. Here Fig.4 shows output waveform of proposed 8T SRAM cell. The result obtained of proposed circuit is compared with the previous circuit and is tabulated as shown below in Table 1and Table 2.

Table 1. Conventional 8T SRAM Cell Results

Frequency (in HZ)	Power (in µW)	Write_1		Write_0	
		Delay (ps)	PDP (in a)	Delay (ps)	PDP (in a)
500M	2.5731	74.940	192.828	45.319	116.610
1G	4.8162	73.133	352.223	45.552	219.387
2G	9.5662	73.084	699.136	45.542	435.663

Table 2. Proposed 8T SRAM Cell Results

Frequency (in HZ)	Power (in µW)	Write_1		Write_0	
		Delay (ps)	PDP (in a)	Delay (ps)	PDP (in a)
500M	0.6065	46.744	28.350	28.349	17.193
1G	1.1601	47.548	55.160	27.739	32.180
2G	6.7268	69.041	464.442	33.972	228.522

V. CONCLUSION

As, technology shrinks day by day power dissipation and speed main concern of any high VLSI device. The modified 8T SRAM cell is used for low power dissipation and high speed Memory Cell. The proposed 8T SRAM cell shows approx 76.42% reduction in power dissipation. This high speed and low power 8T SRAM cell finds application mainly in flash memory. Simulation is carried out using Tanner EDA Tool on CMOS 90nm technology.

VI. REFERENCES

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