# 400X, 400T Series
# Dual MOSFET Switch Mini Module
## SMT, High Speed, High Voltage, Opt Terminals

ACTUAL SIZE

XSYSTOR

PRODUCT FLYER
August 2015

## General Description

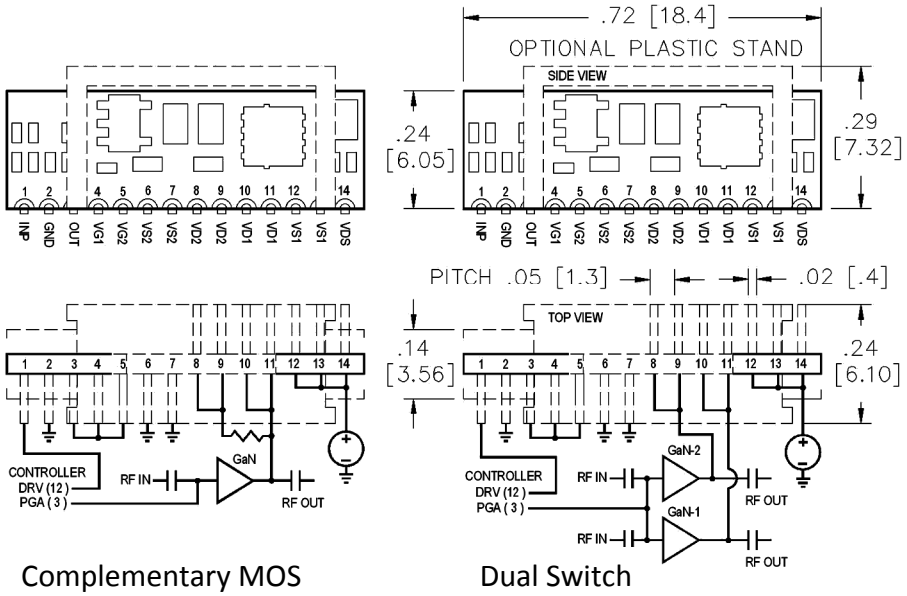
The 400 Series Dual MOSFET Mini Switch offers ease of integration to the GaN amplifier. With board space at a premium, its very tiny footprint allows direct placement to the RF chokes and supply lines of two or more devices. The current capacity of each switch is 10A average CW with good heat sinking, and safe with momentary peak surges of current reaching >3X the average. The SMT switch is ideally driven by the 100 or 200 Series Controllers with direct connection to its GATE input port. The 400 Series come in dual P-channel or complementary P & N-channel (Push-Pull).

## Features

- Rated for 100V
- Ultra-low Rds ON
- Operation up to 175°C, with derated voltage and current.
- CW and Pulsed versions available.
- Ideal for 2-stage amps, balanced amps, and for single GaN with critical rise and fall time requirements.
- Push-pull (totem pole) configuration assures faster shut-down to Vds=0.
- Total switching times of <500 nsec when used together with 100 or 200 Series GaN Controllers.
- Available in tape & reel.
- RoHS* Compliant

| | |
|---|---|
| INP | INPUT FROM CONTROLLER DRIVER |
| GND | GROUND |
| OUT | OUTPUT TO MOSFET GATES |
| VG1,VD1,VS1 | GATE, DRAIN, SOURCE OF MOS #1 |
| VG2,VD2,VS2 | GATE, DRAIN, SOURCE OF MOS #2 |
| VDS | POSITIVE VOLTAGE SUPPLY |

## Typical Connection Diagrams




Complementary MOS  Dual Switch

## Specification Snapshot

| Parameter | Min | Max |
|---|---|---|
| Source Voltage | +28 V | +80 V |
| Gate Voltage | 0 V | +20 V |
| Drain Voltage | +28 V | +80 V |
| Drain Current, CW | | 10 A |
| Rds ON, P-channel | | 0.18 Ω |
| Rds ON, N-channel | | 0.08 Ω |
| Turn-ON Propagation Delay | | 100 ns |
| Turn-ON Rise Time | | 70 ns |
| Turn-OFF Propagation Delay Complementary Pair Only | | 150 ns |
| Turn-OFF Fall Time | | 100 ns |
| Period for Pulsed Versions | | 5 ms |
| Soldering Temp (10 sec) | | +260°C |
| Operating Temperature | -40°C | +85°C |
| Storage Temperature | -65°C | +150°C |

Propagation Delay is measured from 90% of Drive Signal from Controller to 10% of Drain Voltage Output with load of 1KΩ. Faster speeds occur with decreased load resistance. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

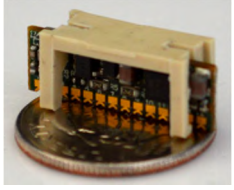
## Ordering Information

| | |
|---|---|
| 410X0000<br>410T0000 | 10 AMP AVG, DUAL P-CHAN MOSFET SWITCH, CW |
| 420X0000<br>420T0000 | 10 AMP AVG, DUAL P-CHAN MOSFET SWITCH, PULSED |
| 430X0000<br>430T0000 | 10 AMP AVG, COMPLEMENTARY P-N-MOS SWITCH PAIR, PULSED |

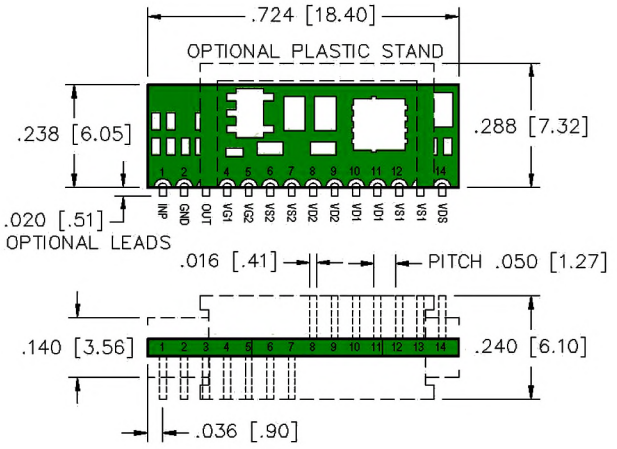
X = STANDARD CONFIGURATION

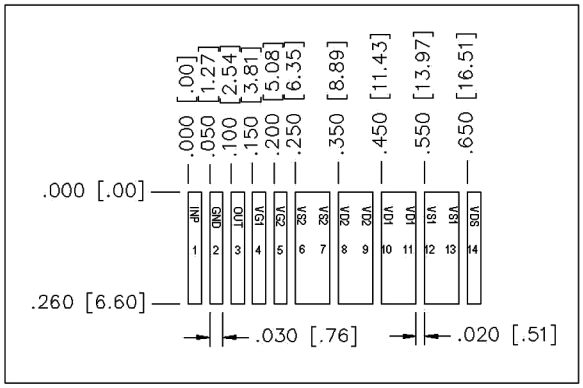
T = OPT PINS AT 0.05" [1.3mm] PITCH


**XSYSTOR INC.**
**18000 STUDEBAKER RD SUITE 700 MS 723**
**CERRITOS CA 90703**
**TEL: 888-968-7755 FAX: 888-968-7755**
**EMAIL: SALES@XSYSTOR.COM**

## Outline & Land Pattern

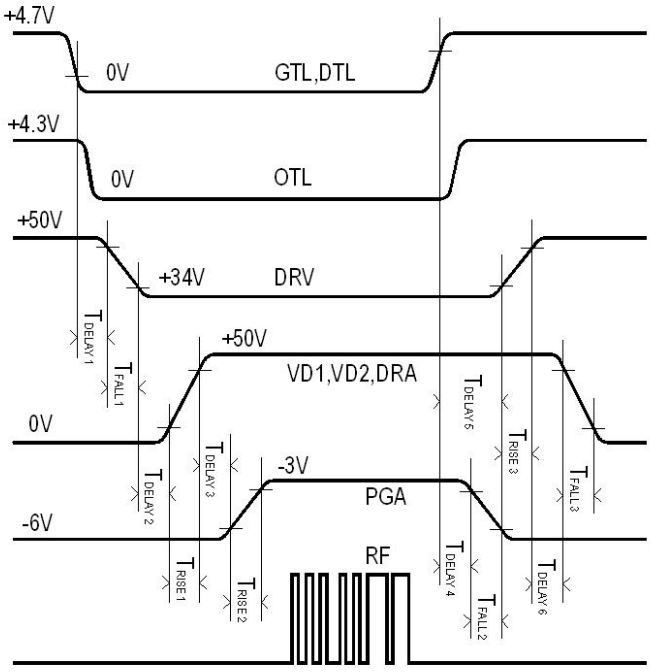



TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED

## Typical Timing Diagrams

Refer to Application Note XAN-2 for further details.




## Switch I/O Pin Descriptions

**INP** input connects directly to the Controller DRV output.
**OUT** is a low-side driver output which connects to MOSFET gates VG1 and VG2.
**VG1, VG2, GAT** are gate inputs that receive signals from DRV output of Controller. For a general purpose switch like the 410, the DRV pin can be tied to VG1 & VG2, while bypassing INP & OUT pins.
**VD1, VD2, DRA** are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.
**VS1, VS2, SOU** are source inputs that take up to +80V supply. Larger storage capacitance are attached here.

## Controller I/O Pin Descriptions

**WARNING**
—Do not connect Outputs together unless specified to do so.
—Do not ground unused Outputs. Leave open.
—Familiarize with the maximum rated voltages and currents.

**NTP** has –4.3V output from a voltage inverter. It is intended to be tapped if needed, by a >10KΩ potentiometer to establish the -Vgs input to the POT pin of the 100 series.
**VN6** input is connected to the system negative supply of less than –6V. Although the 30mA output of the voltage inverter may suffice in most instances, an external supply is helpful for gate current boost of large GaN in saturation.
**POT** input receives negative voltage for the 100 series or positive voltage for the 200 series. Then the value is either inverted or not to approximately the same level reaching the transistor gate.
**PGA** output produces a square waveform triggered by TTL signal to pin GTL. It provides gate bias to GaN HEMT at a level set from POT pin and down to V_pinchoff established from the voltage inverter (-4.3V) or from pin VN6.
**FGA** output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.
**PTP** has +4.3V output from a voltage regulator. It is also intended to be tapped if needed, by a >10KΩ potentiometer to set operating voltage for POT pin of the 200 series.
**GTL** input is an independent, active-low TTL signal ( <4.7V ) that controls gate switching of the device. It is tied together with DTL pin for sequential pulse-width modulation at both gate and drain of the GaN. This is not used for sub-models.
**DTL** input is the primary logic enabler that controls the drain switching end of the transistor. When tied with GTL pin, the active-low TTL ( <4.7V ) switches the drain voltage ON first and would remain there until the gate voltage signal undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during Vdd ramping up & down.
**VP4** input is connected to the system logic supply of ≤ 5V. If none is available, the internal voltage regulator kicks in unless the feature is not included in sub-models.
**OTL** output is an active-low TTL drive signal reserved for future switches with high/low-side drivers. Leave pin open.
**DFB** input monitors the presence of drain voltage when the MOS switch is ON. It is only used if gate switching is desired; otherwise, leave pin open for sub-models.
**DRV** output connects to the gate input of MOSFET switch module. The open drain port can handle up to 300mA, or be connected to multiple switching units.
**VDS** input receives up to +80V from the same supply that powers the GaN HEMT. This source generates negative and logic voltages internal to the 100 and 200 models.

## Model Number Color Code

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|