Design of Fault Tolerant Full Subtractor

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Abstract- Now days, the complexity of integrated circuits is increasing while reliability of the components is decreasing due to small gates and transistor. One of the impacts of technology scaling is more sensitivity to transient and permanent faults. It is very difficult to detect these faults offline. The fault tolerant subtractor can detect the faults and tolerate the detected faults. There are many fault tolerant full subtractor which can detect these faults online. So, an efficient fault tolerant full subtractor is proposed in this paper which can detect the faults with their exact location and also tolerate the faults. The proposed subtractor can detect the faults in single and multi net. The design has less area overhead and has less power requirements as compared to the previous techniques.

Keywords-*Full subtractor, Fault tolerance, DFT (design for testability), single fault, double fault*

I. INTRODUCTION

With technology advancement, the complexity of circuit increases which results to increase the occurrence of the faults. The presence of these faults can destroy the functionality of overall system. Modern integrated circuits with smaller sizes are more prone to transient faults. The reason of these faults are electromagnetic noises, crosstalk and power supply noises. So, Fault tolerant system plays important role in critical application where immediate human action is not possible. For reliable and efficient operation of a system, the detection of the transient fault is necessary [1-3]. These faults can be detected online by using the concept of self checking. Fault tolerant system performs two functions - detection and correction of the faults. The design can perform these functions with minimum hardware and area requirements [4-5]

Arithmetic operations are frequently used in VLSI circuits. Subtractor performs subtraction which is one of the arithmetic operations. Subtractor is also used in other parts of processor. Subtraction is carried out using adders in addition of some extra circuit like generating 2's complement of a number which is to be subtracted. The proposed design is an independent subtractor so that addition and subtraction can be carried out parallel which improves the performance of system. So, the design of faster and reliable subtractor is of great importance in such systems. There are many approaches to achieve the fault tolerance in full subtractor. The researchers have introduced the concept of redundancy to detect the fault in full subtractor. But in order to detect and tolerate the faults there is need of an efficient fault tolerant full subtractor.

A. Fault Tolerance

Fault tolerance is the ability of the system to continue performing its functions even one or more its components have faults or failures. This capability of performing makes the system more software component. Implementation of fault tolerance technique depends on faults, design, configuration and application of the system. The faults can be of any type-hardware or software. In hardware faults mostly permanent, transient, stuck-at faults occur in the system. It is necessary to detect and repair these faults online.

For detection and repairing the faults there is need of fault tolerant design which is reliable and have less area overhead and power requirements [6-7].

B. Redundancy

There are many approaches to design a fault tolerant system. The most common approach is redundancy. It is basically addition of resources beyond what is needed for normal system operation. In hardware redundancy, there is need of extra hardware to detect and tolerate the faults. The redundancy technique is N- modular redundancy [8]. For N = 2 there is DMR (double modular redundancy) in which one extra full subtractor is used along with the original full subtractor to detect the faults as shown in Fig.1. Outputs of both subtractors are compared by using x-nor gates and if

they are not equal then it shows there is fault in the circuit. It has 200% area overhead requirements.

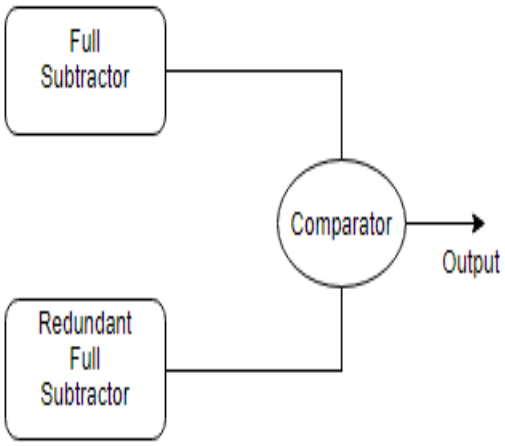

Fig.1. Double Modular Redundancy

Similarly for N = 3, TMR (triple modular redundancy) in which two redundant full subtractor is used along with the original full subtractor as shown in Fig.2. The output of three subtractors can be compared by using x-nor gates and if two generate the same output then the output of third subtractor also considered as faulty. A fault condition is there if output of any two modules is different from the third module. It also requires 300% area overhead. This technique can detect the faults but can't able to repair the faults [9]. So there is need of fault tolerant design which can detect and repair these faults.

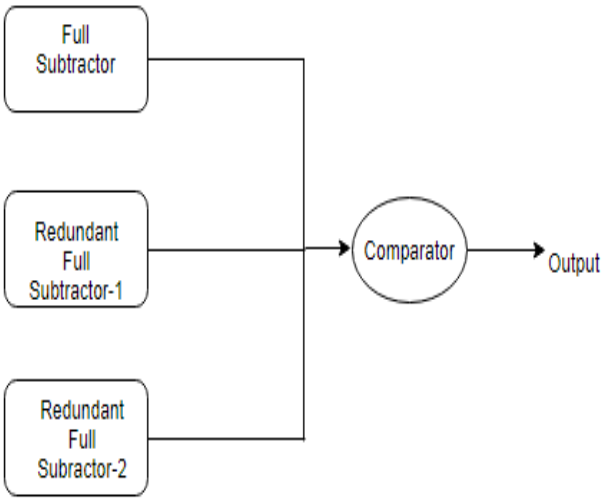

Fig.2. Triple Modular Redundancy

II. DESIGN OF FAULT TOLERANT FULL SUBTRACTOR

In digital circuits, subtractor is one of the most important components used in various applications. Subtractor is a combinational circuit which performs subtraction with A, B and B_{in}. Fault tolerant full subtractor has the ability to detect and correct the faults. Following are some design with can detect faults in subtractor.

A. Full Subtractor with DFT for single fault

The expressions for difference and borrow out are shown in equations 1 and 2. Here, we have to calculate the value of diff (difference) and bout (borrow out) from the inputs A, B and B_{in} (borrow-in).

$$diff = A \oplus B \oplus B_{in} \quad (1)$$

$$b_{out} = A'B + A'B_{in} + B\,B_{in} \quad (2)$$

The author in [10] designed a self checking full adder. Full subtractor can be tested for faults by using the functional unit F1 as shown in Fig. and we have to compute the logic for functional unit and the expression for this is shown in equation 3. By using this functional unit and two x-nor gates (X1 and X2) as shown in fig.3 we can find that the circuit works under fault free condition or not.

$$F1 = A\,B'\,B_{in}' + A'\,B\,Bin \quad (3)$$

TABLE I
TRUTH TABLE OF SUBTRACTOR WITH DFT FOR SINGLE FAULT

A	B	B_{in}	Diff	b_{out}	X1	F1	E_f
0	0	0	0	0	1	0	0
0	0	1	1	1	1	0	0
0	1	0	1	1	1	0	0
0	1	1	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	0	0	0	1	0	0
1	1	1	1	1	1	0	0

The gate X1 is used for x-nor operation of diff and b_{out}, gate X2 which gives final E_f is used to compare the value of X1 and F1 by the x-nor operation as given in equation 4 and 5.

$$X1 = (diff \oplus b_{out})' \quad (4)$$

$$E_f = (X1 \oplus F1)' \quad (5)$$

If the value of E_f is 0 then it shows there is no fault in the circuit. On the other hand if E_f is 1 then fault will be indicated. In this way, the design can detect the single fault in single net. The fault which is detected can be either in diff or bout output. The design also decreases the area overhead as compared to the previous approaches TMR and DMR.

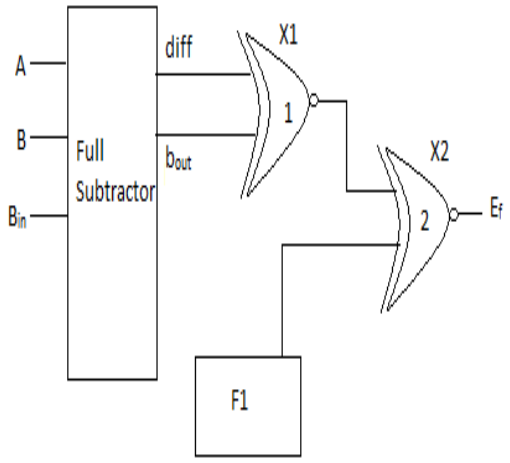

Fig.3. Full subtractor with DFT for single fault

B. Full Subtractor with DFT for double fault

The author in [11] proposed a self checking adder which can detect the faults. Now there is a proposed design of full subtractor is shown in Fig.4 which can detect single fault at a time and not able to detect the double fault occur at a time.

Now there is a design which can detect single and double fault occur at a time and also capable of identifying the location of the fault. The diff and bout output bits are verified individually to make the design more efficient and reliable. It also reduces the hardware cost as compared to various previous approaches.

TABLE II
TRUTH TABLE OF DFT FOR DOUBLE FAULT

A	B	Bin	diff	b_{out}	X1	X2	X3	F1	F_d	F_b
0	0	0	0	0	0	1	1	0	0	0
0	0	1	1	1	1	0	0	1	0	0
0	1	0	1	1	0	1	1	0	0	0
0	1	1	0	1	1	0	1	0	0	0
1	0	0	1	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0
1	1	0	0	0	1	0	0	1	0	0
1	1	1	1	1	0	1	1	0	0	0

In the design, by using one x-or gate, four x-nor gate and one functional unit we can find whether the circuit works under fault free condition or not. The gate X1, X2 are used to detect the fault in diff bit and the gate functional unit F1, gate X3 are used to detect the fault in bout bit. The gate X4 and X5 gives the final outputs F_d and F_b. The expressions for all gates and functional unit are shown in following equations:

$$X1 = A \oplus Bin \quad (6)$$

$$X2 = (diff \oplus B)' \quad (7)$$

$$X3 = (b_{out} \oplus B)' \quad (8)$$

$$F1 = A' B' Bin + A B B_{in}' \quad (9)$$

$$F_d = (X1 \oplus X2)' \quad (10)$$

$$F_b = (X3 \oplus F1)' \quad (11)$$

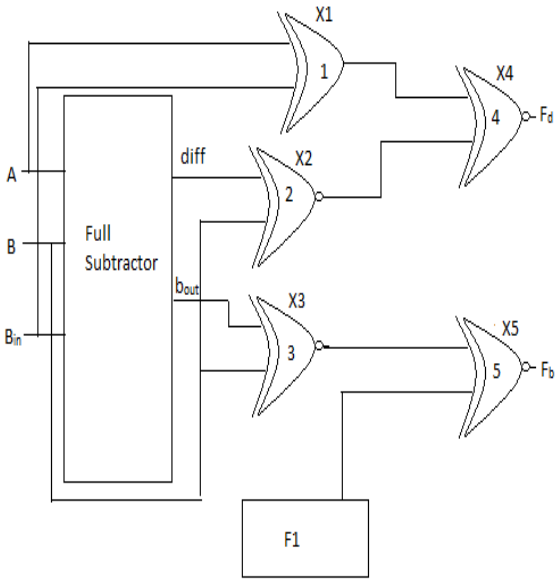

Fig.4. Full subtractor with DFT for double fault

The fault can be detected in diff and bout output bits in the form of F_d and F_b. If the value of F_d is 0 then there is no fault in difference bit and if it is 1 then it indicates the faulty condition. Similarly if value of F_b is 0 then borrow out bit is also fault free otherwise borrow out bit of full subtractor is faulty.

C. Fault tolerant full subtractor

The fault tolerant full subtractor is used for repairing the faults which is detected during testing process. The design can repair single and the double faults. The author in [11] designed a self

repairing circuit to repair the faults in adder. In fig.5 there is tolerant circuit in which value of diff output bit is selected by the multiplexer under the control of F_d and value of bout is also selected by the multiplexer according to F_b bit. If value of F_d is 0 then diff output bit is selected by the multiplexer and If F_d is 1 then multiplexer selects the inverted value of diff output. Similarly If value of F_b is 0 then bout output bit is selected by the multiplexer and If F_b is 1 then multiplexer selects the inverted value of bout output.

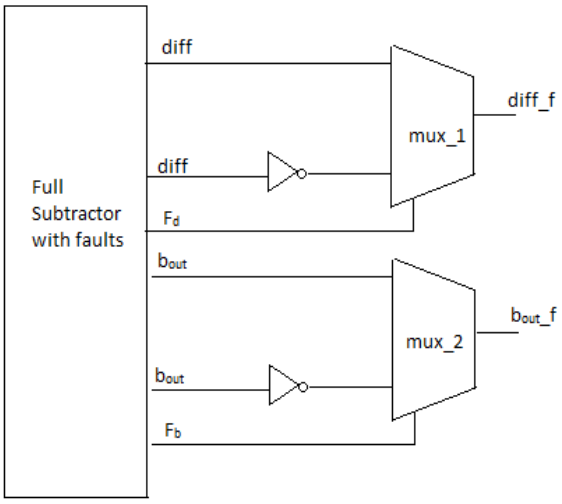

Fig.5. Fault tolerant full subtractor

II. SIMULATIONS RESULTS AND COMPARISON OF TECHNIQUES

A. Simulation Results

The fault tolerant full subtractor with DFT for single fault can detect only one fault. The fault in final output can be indicated in form of E_f.

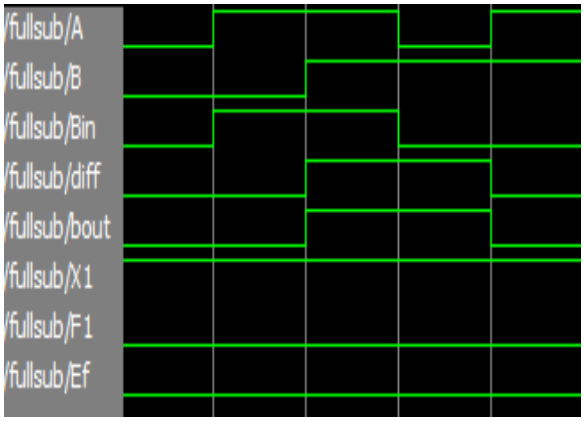

Fig.6. Output Waveform of fault free Full subtractor for single fault

If the value of E_f is high then the circuit is faulty. The output waveform fault free full subtractor and faulty full subtractor are shown in fig.7 and fig.8.

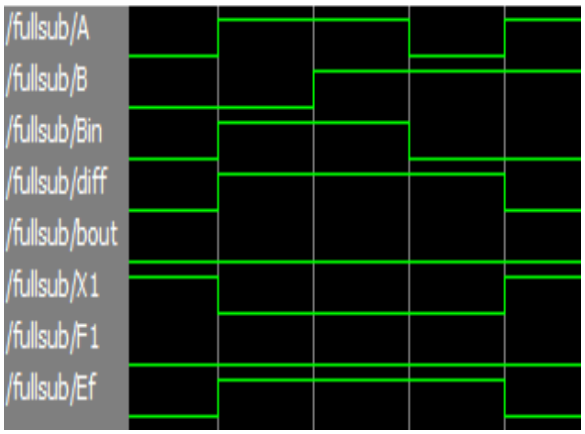

Fig.7. Output Waveform of faulty Full subtractor for single fault

The fault tolerant design with DFT for double fault can detect single and double faults in multiple nets. The final output are in terms of F_d and F_b .If both values are low then there is no fault and if any one of them or both are high then the circuit is faulty and the fault which is detected can be corrected by the repairing circuit. The output waveform are shown in fig.9 and fig.10

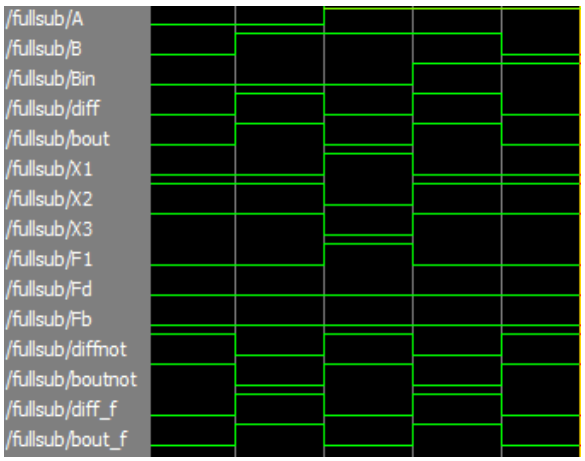

Fig.8. Output Waveform of fault free Full subtractor for double fault

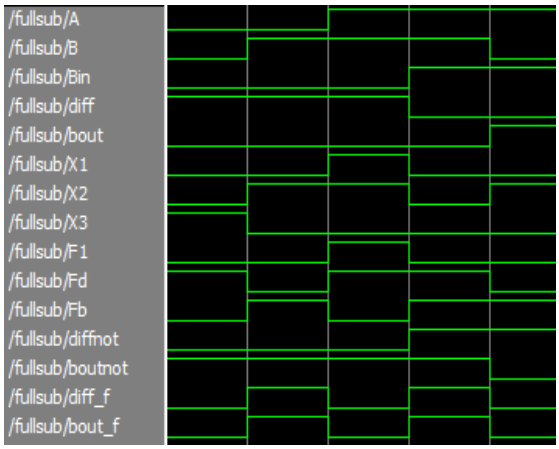

Fig.9. Output Waveform of faulty Full subtractor for double fault

B. Comparison of different techniques

There is comparison of proposed full subtractor with the existing approaches like DMR and TMR on the basis of fault detected, conditions and fault tolerated which is shown in table 3. According to the designs internal structure there is comparison of various approaches on the basis of cell used, input-output ports, nets and gates which is shown in table 4.

TABLE III.

COMPARISON ON THE BASIS OF FAULT DETECTION, TOLERANCE AND POWER

	DMR	**TMR**	**DFT with single fault**	**DFT with double fault**
Faults detected	Single fault	Single fault	Single fault	Single fault and Double fault
Conditions	Output = 0 -fault free Output = 1 - faulty	Output = 0 -fault free Output = 1 - faulty	E_f =0 - fault free E_f =1 - faulty	F_d = 0 and F_b =0 - fault free F_d = 1 and F_b =0 - fault in diff output F_d = 0 and F_b =1 - fault in b_{out} F_d = 1 and F_b =1 - fault in both output
Tolerance	Possible with double area overhead	Possible with triple area overhead	Possible with less area overhead	Possible with very less area overhead
Power	0.242 W	1.081 W	0.242 W	0.593 W

TABLE IV

COMPARISON ON THE BASIS OF INTERNAL STRUCTURES

	DMR	**TMR**	**DFT with single fault**	**DFT with double fault**
cells	8	11	6	11
I/O ports	5	5	4	5
Nets	13	17	10	15
gates	16	23	17	20

IV. CONCLUSION

In this paper, firstly a fault generated by a full subtractor is detected by a proposed design of full subtractor with DFT for single fault. But this design is not able to detect more than one faults. Then a full subtractor with DFT for double fault is designed with can detect single and double fault and capable of identifying the exact location of the fault. Then self repairing circuit is designed which can repair the detected faults. The design provides the higher error detection and correction capabilities. This design has less area overhead as compared to the existing designs and has less power requirements.

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