Two-trap model for low voltage stress-induced leakage current in ultrathin SiON dielectrics

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Stress-induced leakage current is a useful probe of the buildup of trap states created by the electrical stress of ultrathin dielectric films. The generation of both bulk and interface traps can affect the current-voltage characteristics. It has been shown that trap assisted tunneling through interface traps is the dominant transport mechanism below 3.5 nm thickness when the poststress leakage is sensed in the off state. However, there is some ambiguity in the literature regarding whether traps at one or both of the contact interfaces are involved in the tunneling process. In this work, we show that for *n*-channel metal-oxide-semiconductor (NMOS) devices, the off-state ($V_G < 0$ V) gate current of electrically stressed ultrathin SiON dielectrics senses a two-trap tunneling process that involves interface states at both anode and cathode interfaces. In aggregate, five peaks due to tunneling via interface traps are observed in the poststress *I-V* characteristics of ultrathin NMOS SiON dielectrics. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2969791]

I. INTRODUCTION

The *I-V* characteristics of dielectric films subjected to electrical stress has long been a topic of considerable interest. In oxides thicker than about 7 nm when the applied field is too low for Fowler–Nordheim tunneling to occur, only transient gate currents are observed after stress due to detrapping via tunnel emission of carriers trapped within a few tunneling lengths of the device electrodes.[1–5] When the oxide thickness is scaled below 7 nm, a steady-state poststress gate current is observed, primarily when it is measured in the direct tunneling regime.[1] This instability is known as stress-induced leakage current (SILC). It is due to trap assisted tunneling through neutral electron traps in the bulk of the dielectric,[1,6] and is an inelastic tunneling process with an energy loss of about 1.5 eV.[7,8] Empirically, the SILC increase due to the generation of bulk traps is weakly dependent on the poststress sense voltage.[6]

For oxide thickness less than about 3.5 nm, a sense voltage dependent steady-state leakage instability is observed when the gate current is measured in the off state.[9] This effect is called low voltage SILC (LV-SILC) since (i) the phenomenon is readily observable below the threshold voltage for bulk trap generation (approximately 5 V),[6] and (ii) in oxide films, the degradation is highest near flatband voltage (V_{FB}) and is detected only when the sense voltage is $V_{FB}+/-1$ V, as shown in Fig. 1.[9] It can be seen that LV-SILC is observed only when the energy states within the anode and cathode band gaps are within the same range of electrostatic potential, indicating that LV-SILC is due to tunneling via interface traps.[9] Unlike trap assisted tunneling through bulk traps, LV-SILC is either an elastic tunneling process or an inelastic tunneling process with a small relaxation energy because LV-SILC is still observed as V_G approaches 0 V, as shown in Fig. 1.[9]

The capability to resolve the effects of interface states (through LV-SILC) and bulk traps (through SILC) on the reliability of gate dielectrics has provided insight into the trap distributions and degradation mechanisms that lead to the breakdown of ultrathin SiO_2 and SiON films. Some of these results are that (i) the creation of bulk traps controls breakdown in sub-3 nm SiO_2 films,[10] (ii) the generation of interface states is the rate limiting step controlling breakdown in sub-1.5 nm SiON films below 2.7 V stress,[11] and (iii) trap generation results from the release of two hydrogen species from the anode interface during low voltage stress of ultrathin SiON dielectrics.[12]

While Ref. 9 identified trap assisted tunneling via interface states as a mechanism for SILC, tunneling via interface traps is a known effect. In the late 1960s, tunneling from metal gates into as-grown $Si-SiO_2$ interface traps was inferred by noting that wafer processing that led to higher *C-V* extracted interface trap densities also had higher conductance when the device was biased so that the metal Fermi level aligned opposite the substrate band gap.[13] This effect was observed only when heavily doped $p{+}{+}$ substrates were uti-

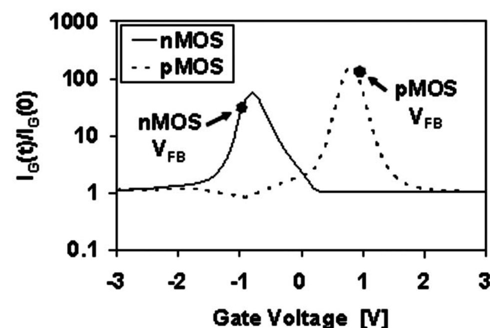

FIG. 1. Poststress increase in gate current vs sense voltage at 298 K for NMOS and PMOS devices with 2.7 nm SiO_2 dielectrics. For both devices, the degradation is highest when the sense voltage approaches V_{FB}. After Nicollian, Ref. 9. © 1999 IEEE.

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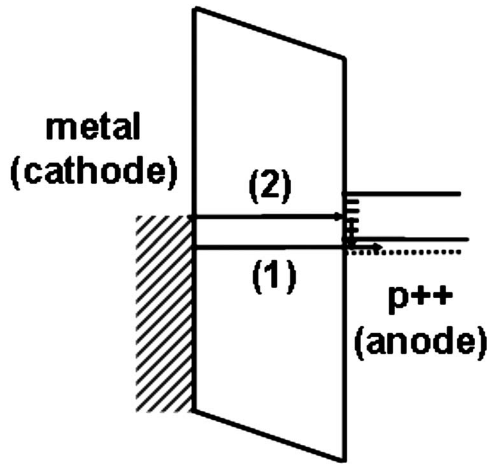

FIG. 2. Band diagram for tunneling in a metal-oxide-p++ structure with $-V_G$ applied. The possible transport paths are (1) tunneling of electrons from the metal gate into the p++ VB, (2) tunneling of electrons from the metal gate into as-grown interface traps at the oxide-p++ interface, followed by recombination with holes.

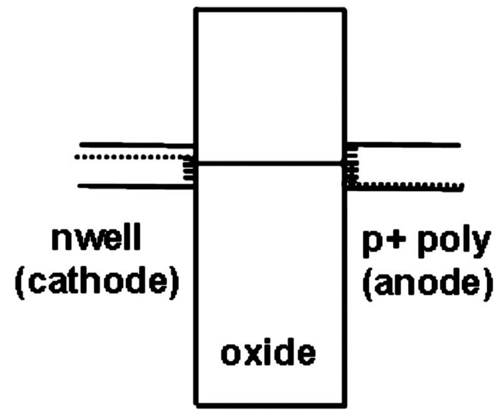

FIG. 3. Band diagram for PMOS at $V_G = V_{FB}$ illustrating a two-trap LV-SILC process. Electrons tunnel from interface traps below the n-well Fermi level into interface traps above the p+ polysilicon Fermi-level. A steady-state current arises when electrons captured in p+ polysilicon-SiO_2 interface traps recombine with majority holes in the p+ polysilicon.

lized. Under these conditions, the current through the dielectric could be due to either tunneling from the metal into unoccupied states in the silicon valence band (VB), or into interface traps, as shown in Fig. 2. For tunneling from the metal into the silicon VB, the substrate must be degenerately doped p++ so that the substrate Fermi level is at a lower energy than the VB edge. This provides empty states in the VB for electrons to tunnel into. For tunneling into interface traps to result in a steady-state current, the electrons that are captured by interface traps must recombine with majority carrier holes in the accumulated p++ substrate.[13]

In the more recent experiments reported in Ref. 9, the devices are fabricated with polygate electrodes and the substrates are not degenerately doped. Accordingly, electrons cannot tunnel from the gate into the VB as in Fig. 2 because the p-doped body of the NMOS device (p-well) Fermi level is above the p-well VB edge. Also, the LV-SILC peaks in Ref. 9 occur near V_{FB}, where the field across the oxide is zero. Under these conditions, the driving force for conduction is the separation between the cathode and anode Fermi levels. In this operating mode, the current through the dielectric can only be due to tunneling into trapping centers because no other states are available to tunnel into. At $V_G = V_{FB}$, no gate current would flow in the absence of trap states.

Another key difference between the experiments in Ref. 9 and the results in Ref. 13 is that the cathode is supply limited in the portion of the I-V sweep between V_{FB} and 0 V for the devices investigated in Ref. 9. Figure 1 showed that LV-SILC remains significant under these bias conditions. In p-channel metal-oxide-semiconductor (PMOS) devices, the nondegenerately n-doped body of the PMOS device (n-well) Fermi level is more than a few k_BT below the n-well conduction band (CB) edge. This adds complexity to the model for LV-SILC transport because the emission of tunneling electrons is energetically favorable for states below the cathode Fermi level. This opens up the possibility of tunneling from trap states in the cathode to trap states in the anode, (i.e.,) a two-trap tunneling process becomes a viable transport mechanism. This process is illustrated for a PMOS device biased near V_{FB} in Fig. 3. Interface traps that are closest to the cathode Fermi level have the highest emission probability because the barrier height is smaller than for traps that are significantly below the cathode Fermi level. Tunneling of VB holes from the p+ polysilicon into n-well interface traps is also a possibility, but the high barrier height for this process makes it less likely.

While papers have been subsequently published by other researchers after the discovery of the LV-SILC effect,[14–17] there is still some confusion regarding the details of the mechanism and whether traps at one or both of the contact interfaces give rise to LV-SILC. In this paper, we will provide our interpretation of the phenomena in ultrathin SiON films to clarify LV-SILC effects in n-channel MOS (NMOS) devices. We will show that interface traps at both cathode and anode interfaces participate in LV-SILC transport, so that LV-SILC is a two-trap tunneling process.

II. EXPERIMENT

Three-terminal NMOS devices with 1.2 nm equivalent oxide thickness device-grade SiON dielectrics fabricated through plasma nitridation in a 90 nm full-flow complementary MOS process[18] are stressed at 378 K in inversion at a gate voltage of +2.2 V. The channel length is 1×10^{-4} cm and the gate oxide area is 3×10^{-7} cm^2. All device terminals are connected during stress. Only the gate terminal is biased during the sense operation and is performed either with all terminals connected or with one terminal floating. To attain relatively large Si–SiON interface trap densities, in addition to the gate stress voltage, a substrate voltage of $V_B = -6$ V is also applied during stress, as it has been shown that substrate bias increases trap generation rates through electron heating in the silicon.[12,19] Strictly speaking, LV-SILC is a steady-state current when $V_B = 0$ V during stress since recovery effects have been observed when a substrate voltage is applied.[12] However, meaningful analysis of LV-SILC phenomena can still be obtained because for a given gate stress voltage, temperature, and time, the current increase remains

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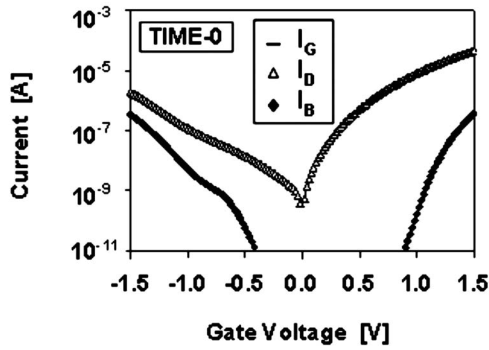

FIG. 4. Time zero NMOS terminal currents at 378 K.

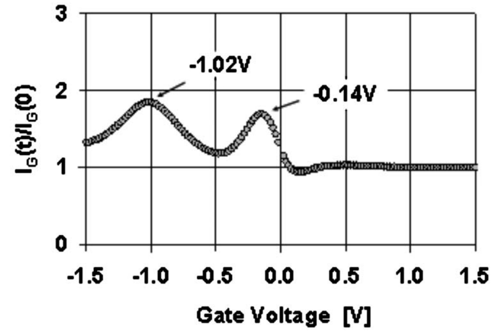

FIG. 6. $I_G(t)/I_G(0)$ at 378 K with all terminals connected during the sense operation.

significantly larger when a substrate bias is applied during stress.[12] For the time period ranging from 30 to 3600 s after stress at the highest temperature (378 K) in our experiment, the gate current recovery is only a few percent. This is an overestimate of the impact of recovery on our results since the actual time at 378 K is much less than 3600 s because after the poststress *I-V* data are acquired at 378 K, the devices are subsequently cooled to lower temperatures (338 and 298 K) for additional characterization.

III. RESULTS

In this section, we present carrier separation data of fresh and poststress NMOS devices. We analyze band diagrams to determine the possible poststress LV-SILC transport paths involving interface states. We consider the possibilities of interface trap generation at the polysilicon-SiON interface, at the *p*-well-SiON interface, and at the drain-SiON (NSD-SiON) interface in the overlap region in our analysis.

A. Carrier separation

We utilize carrier separation to analyze the effects of interface trap generation on gate, drain, and substrate currents. The time-zero *I-V* characteristics for the three-terminal NMOS devices that will be stressed are shown in Fig. 4. The pertinent features of Fig. 4 are, (1) for $V_G>0$ V, the gate current is dominated by the tunneling of CB electrons supplied by the drain terminal. Therefore, $I_G \sim I_D$. (2) For $V_G>1$ V, electrons from the *p*-well VB can tunnel into the *n*+ polysilicon CB. Since a hole will be generated in the *p*-well for every tunneling VB electron, a substrate hole current will arise. (3) For $V_G<0$ V, a substrate current arises: (i) when electrons tunnel from *n*+ polysilicon to the *p*-well CB followed by diffusion out the *p*-well contact, (ii) when electrons tunnel from *n*+ polysilicon into as-grown interface traps at the *p*-well-SiON interface followed by recombination with holes in the *p*-well, or (iii) when holes are injected from the *p*-well VB into the *n*+ polysilicon VB. A drain current arises when electrons tunnel from *n*+ polysilicon to the *p*-well CB then diffuse into the drain contact or tunnel from *n*+ polysilicon into the NSD region. In our devices, $I_G \sim I_D$ for $V_G<0$ V. From this analysis, it can be seen that a drain current arises when the drain supplies tunneling carriers or when carriers that have been injected from the gate into either the NSD or pwell CB flow out of the drain contact. This can also be seen by comparing the substrate current with the drain floating versus all three terminals connected, as shown in Fig. 5. In the off state, the substrate current is indeed higher with the drain floating since the electrons injected from the gate flow out of the *p*-well rather than drain contact. Note that in the on state, I_B is also higher with the drain floating (until *p*-well VB tunneling becomes significant) due to increased generation rates resulting from the *p*-well going into deep depletion without the drain to supply inversion layer electrons.

The poststress increase in NMOS gate, drain, and substrate currents sensed with all device terminals connected are shown in Figs. 6–8, respectively. Unlike the SiO_2 films in Fig. 1, two LV-SILC peaks appear in the gate current for NMOS SiON films when all device terminals are connected during sense as shown in Fig. 6. Two LV-SILC peaks in PMOS SiON films have also been reported.[16,20] Three

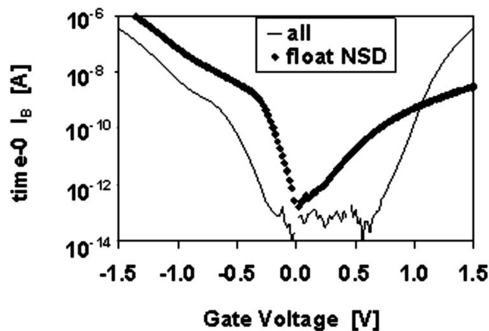

FIG. 5. Time zero I_B vs V_B characteristics at 378 K both with and without the drain floating during the *I-V* sweep.

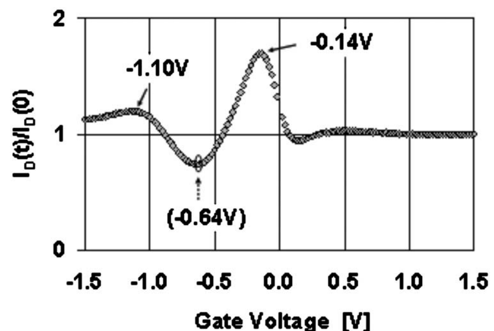

FIG. 7. $I_D(t)/I_D(0)$ at 378 K with all terminals connected during the sense operation.

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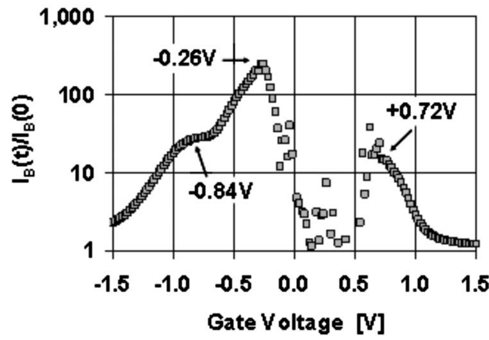

FIG. 8. $I_B(t)/I_B(0)$ at 378 K with all terminals connected during the sense operation.

LV-SILC peaks are present in the NMOS drain current when all three terminals are connected during sense as shown in Fig. 7. One of these peaks manifests itself as a dip in the poststress drain current at $V_G=-0.64$ V, where $I(t)<I(0)$. This dip in I_D is only seen when a substrate bias is applied during stress, where a large p-well interface trap density results. In Fig. 8, three LV-SILC peaks are observed in the NMOS substrate current when all device terminals are connected during the sense operation. The differences in the LV-SILC spectra between and SiO_2 and SiON may be due to differences in stress-induced defects. While electron spin resonance has shown that P_b centers[21] are created at the $Si-SiO_2$ interface following electrical stress,[22] a class of defect called the K_N center is observed at or near the Si–SiON interface after negative-bias-temperature-instability stress.[23] The K_N center appears to have a narrower energy density of states compared to P_b centers.[23] Another difference between stress generated $Si-SiO_2$ and Si–SiON interface traps is that for the Si–SiON interface, only acceptor interface states are observed when NMOS samples are stressed with $V_G>0$ V,[12] whereas only donor states are observed when PMOS devices are stressed at $V_G<0$ V.[20] In contrast, traps at the $Si-SiO_2$ interface can be amphoteric.[24,25] Beyond noting these differences between the defects at the $Si-SiO_2$ and Si–SiON interfaces, it is not within the scope of this work to develop a comprehensive explanation of the microscopic differences in traps generated at the $Si-SiO_2$ versus Si–SiON interface.

To interpret the LV-SILC data for SiON, the possible origins of a current increase resulting from the introduction of interface traps must be determined. Low probability transport mechanisms such as electrons tunneling into n+ polysilicon interface traps followed by recombination with holes are not considered since the density of holes is small in such a heavily n+ doped electrode. For the cases where electrons tunnel into interface traps in the heavily doped n+ polysilicon or NSD regions, since electrons tunnel into unoccupied states above the Fermi level, and the Fermi level is within a few k_BT of the CB, a steady-state current results when the captured electron is thermally emitted into the CB.

We begin with the possible mechanisms whereby electron tunneling between n+ polysilicon and the p-well via interface traps can result in an increase in the steady-state substrate current: Mechanism 1_{B1}: for $V_G<0$ V, electrons tunnel from the n+ polysilicon CB into p-well interface traps, followed by recombination with holes in the p-well. Mechanism I_{B2}: for $V_G<0$ V, electrons tunnel from n+ polysilicon interface traps into p-well interface traps, followed by recombination with holes in the p-well. Mechanism I_{B3}: for $V_G<0$ V, electrons tunnel from the n+ polysilicon VB into p-well interface traps, followed by recombination with holes in the p-well. Mechanism I_{B4}: for $V_G>0$ V, electrons created in the p-well through band-to-band-tunneling (BTBT) in deep depletion tunnel from the p-well CB into n+ polysilicon interface traps, followed by thermal emission into the n+ polysilicon CB. Mechanism I_{B5}: for $V_G>0$ V, electrons tunnel from the p-well VB into n+ polysilicon interface traps, followed by thermal emission into the n+ polysilicon CB.

The mechanisms whereby electron tunneling between n+ polysilicon and the p-well via interface traps can result in an increase in the steady-state drain current are the following. Mechanism I_{D6}: for $V_G<0$ V, electrons tunnel from n+ polysilicon interface traps into the p-well CB. These electrons result in a drain current when they diffuse into the drain region. Mechanism I_{D7}: for $V_G>0$ V, electrons tunnel from p-well interface traps into n+ polysilicon interface traps, followed by thermal emission into the n+ polysilicon CB. In this scenario, electrons that occupy p-well interface traps are supplied by the drain; giving rise to a drain current. Mechanism I_{D8}: for $V_G>0$ V, electrons tunnel from p-well interface traps into the n+ polysilicon CB. The electrons that occupy p-well interface traps are supplied by the drain, resulting in a drain current.

The mechanisms whereby electron tunneling between n+ polysilicon and the NSD overlap region via interface traps can result in an increase in the steady-state drain current are the following: Mechanism I_{D9}: for $V_G<0$ V, electrons tunnel from n+ polysilicon interface traps into the NSD CB. Mechanism I_{D10}: for $V_G<0$ V, electrons tunnel from n+ polysilicon interface traps into NSD interface traps, followed by thermal emission into the NSD. Mechanism I_{D11}: for $V_G<0$ V, electrons tunnel from the n+ polysilicon CB into NSD interface traps, followed by thermal emission into the NSD CB. Mechanism I_{D12}: for $V_G>0$ V, electrons tunnel from NSD interface traps into the n+ polysilicon CB. The electrons that occupy NSD interface traps are supplied by the drain, resulting in a drain current.

The only mechanism that we will consider whereby hole tunneling between n+ polysilicon and the p-well via interface traps can result in an increase in the steady-state substrate current is Mechanism I_{B13}: for $V_G<0$ V, electron hole pairs are created in the p-well via interface traps when the p-well is at midgap potential, followed by injection of holes from the p-well VB into the n+ polysilicon VB.

B. Analysis of transport paths

We begin with the analysis of the I_G peak at −1.02 V seen in Fig. 6. The nearest corresponding drain and substrate current peaks are at −1.10 V (Fig. 7) and −0.80 V (Fig. 8), respectively. Band diagrams for $V_G\sim-1.1$ V and $V_G\sim-0.8$ V are shown in Figs. 9 and 10. In this voltage range, the three possible transport paths that can lead to an

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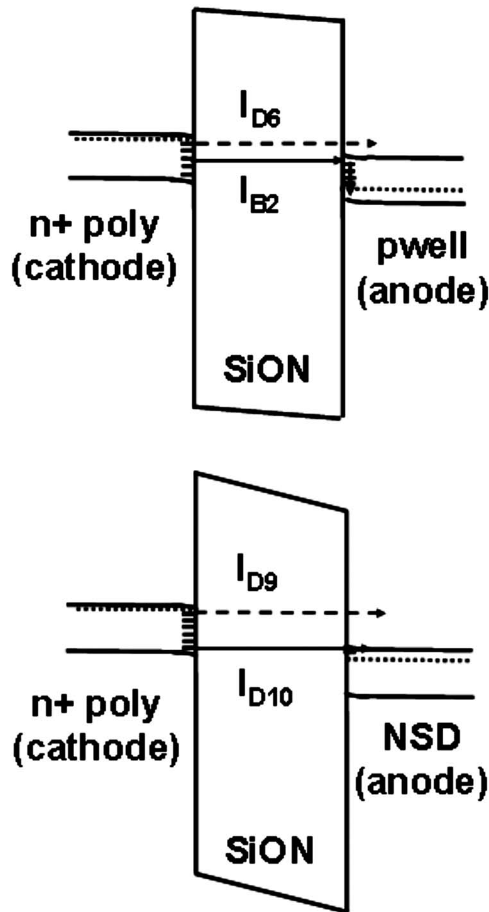

FIG. 9. Band diagrams for LV-SILC at $V_G \sim -1.1$ V for (a) tunneling processes between $n+$ polysilicon and p-well and (b) tunneling processes between $n+$ polysilicon and NSD.

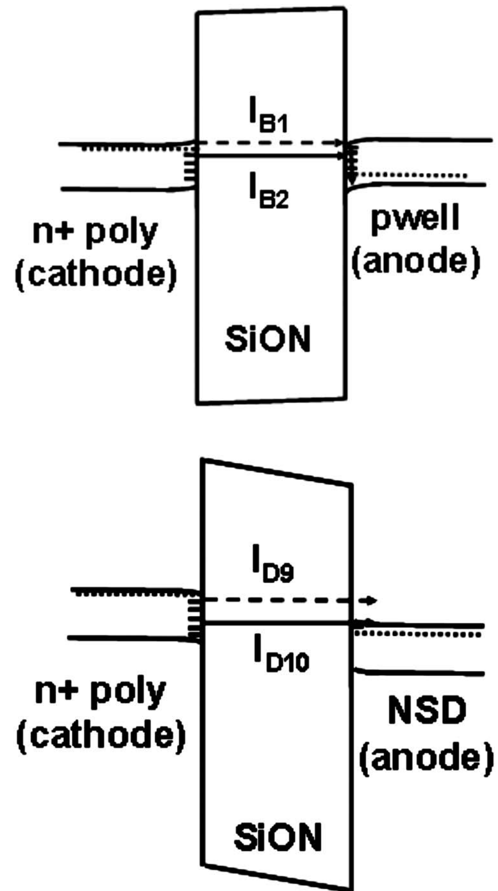

FIG. 10. Band diagrams for LV-SILC at $V_G \sim -0.8$ V for (a) tunneling processes between $n+$ polysilicon and p-well and (b) tunneling processes between $n+$ polysilicon and NSD.

increase in substrate current are electron tunneling from the $n+$ polysilicon CB into p-well interface traps followed by recombination with holes (mechanism I_{B1}), electrons tunneling from $n+$ polysilicon interface traps to p-well interface traps followed by recombination with holes (mechanism I_{B2}) or electrons tunneling from the $n+$ polysilicon VB into p-well interface traps followed by recombination with holes (mechanism I_{B3}). Therefore, the I_G peak at V_G=−1.02 V requires traps at the p-well-SiON interface. The least likely is mechanism I_{B3} due to the higher barrier height for this process and is therefore not shown in Figs. 9 and 10. Since the p-well is depleted at V_G=−0.8 V, electron tunneling occurs against the direction of the oxide electric field. The driving force for tunneling is the energy separation of the cathode and anode Fermi levels. As the substrate current peak at V_G=−0.8 V does not precisely align with the gate current peak at V_G=−1.02 V, this I_G peak has a drain current component.

The transport paths that can give rise to a LV-SILC drain current in this voltage range are also shown in Figs. 9 and 10. All involve emission from traps at the $n+$ polysilicon interface. The least likely path is mechanism I_{D10} in Figs. 9(b) and 10(b) because (i) the barrier height for tunneling is high for this process, as tunneling electrons must be emitted from interface traps near the $n+$ polysilicon VB edge, and (ii) the energy range of traps that can capture tunneling electrons in the NSD is narrow due to the proximity of the NSD Fermi level to the NSD CB. For gate voltages near V_{FB}, the most likely explanations for drain current LV-SILC are tunneling from $n+$ polysilicon interface traps into the p-well CB, followed by diffusion in the drain region (mechanism I_{D6}) or tunneling from $n+$ polysilicon interface traps into the NSD CB (mechanism I_{D9}). We subsequently show that the correct explanation is mechanism I_{D6}.

We will concurrently analyze the dip in I_D centered at V_G=−0.64 V and the peak in I_D at V_G=−0.14 V shown in Fig. 7. Note that in Fig. 8, there is a plateau in $I_B(t)/I_B(0)$ at V_G=−0.64 V rather than a roll-off in degradation as the voltage is swept from the I_B peak at V_G=−0.84 V toward 0 V. This indicates that traps at the p-well interface may still participate in LV-SILC at V_G=−0.64 V. Figure 10 (V_G=−0.8 V) and Fig. 11 (V_G=0.2 V) show that the only LV-SILC paths that lead to an increase in I_D in this voltage range involve tunneling into the small-area NSD overlap region. An increase in I_D after stress cannot be explained by electron tunneling from $n+$ polysilicon interface traps into the p-well CB followed by diffusion into the drain because it is not energetically possible in this voltage range since all $n+$ polysilicon interface traps will be at a lower energy than the p-well CB. To explain the drop in I_D at V_G=−0.64 V after stress, we must find a mechanism that reduces the number of electrons flowing out of the drain contact relative to un-

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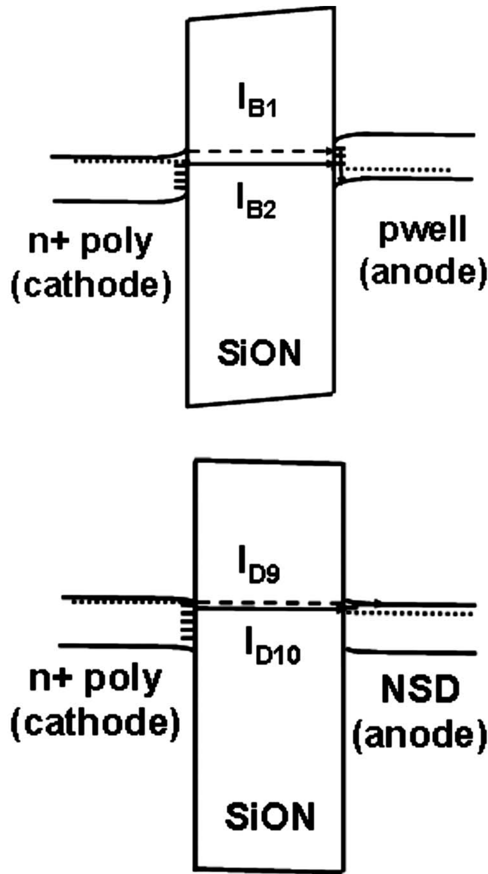

FIG. 11. Band diagrams for LV-SILC at $V_G \sim -0.2$ V for (a) tunneling processes between n+ polysilicon and p-well and (b) tunneling processes between n+ polysilicon and NSD.

stressed condition. The poststress I-V characteristics are shown in Fig. 12. In the off state, the increase in substrate current due to tunneling into p-well interface states is a significant contribution to the total current until $V_G > \sim -0.5$ V. A possible explanation for the dip at $V_G = -0.64$ V is electron tunneling from the n+ polysilicon into p-well interface traps that are in close proximity to the NSD edge. This reduces the number of electrons that flow out of the drain contact relative to time zero. A drop in I_D would occur until the magnitude of the gate voltage is reduced to a small enough value that the energy range of p-well interface traps that can participate in LV-SILC has diminished. Thereafter, LV-SILC in the gate terminal is

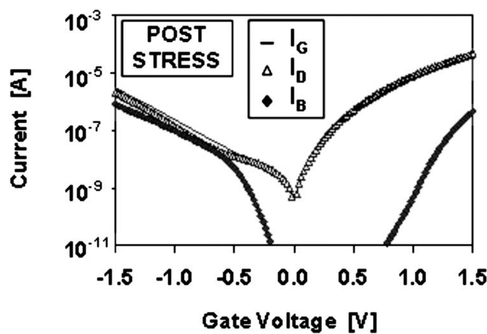

FIG. 12. Poststress NMOS terminal currents at 378 K. The time zero I-V curves for this device are shown in Fig. 4.

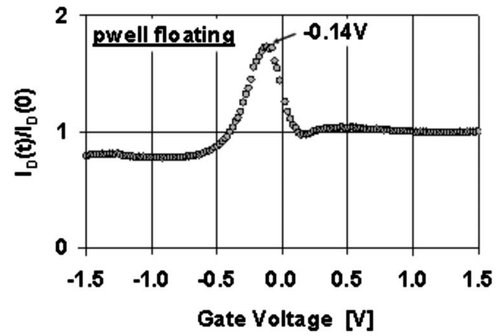

FIG. 13. $I_D(t)/I_D(0)$ at 378 K with the p-well floating during the sense operation.

dominated by tunneling into the NSD region, resulting in the coincident LV-SILC peaks in the drain and gate currents at $V_G = -0.14$ V seen in Figs. 6 and 7.

The poststress increase in I_D sensed with the p-well floating is shown in Fig. 13. The dip at $V_G = -0.64$ V vanishes, which confirms that its origin is the reduction in the number of electrons that are injected into the drain contact relative to the unstressed condition due to recombination in p-well interface traps. In Fig. 13, the drain current peak at $V_G = -1.10$ V has also disappeared, verifying that it is due to tunneling from n+ polysilicon interface traps into the p-well CB, followed by diffusion of these electrons into the drain contact (mechanism I_{D6}). Also from Fig. 13, the LV-SILC mechanisms shown in Fig. 9(b) where electrons tunnel into the NSD region can be eliminated as the origin of the drain current peak at $V_G = -1.10$ V. Therefore, traps at both n+ polysilicon-SiON and p-well-SiON interfaces participate in LV-SILC when the device is sensed near V_{FB} for the n+ polysilicon over p-well region. Only the drain current peak at $V_G = -0.14$ V remains with the p-well floating, so that this LV-SILC peak is indeed due to tunneling between the n+ polysilicon and NSD overlap region. The possible transport paths are electrons tunneling from n+ polysilicon interface traps into the NSD CB (mechanism I_{D9}), and electrons tunneling from n+ polysilicon interface traps into NSD interface traps, followed by thermal emission into the NSD CB (mechanism I_{D10}). Mechanism I_{D9} is more probable due to the narrow energy range of traps at the NSD interface that can participate in the LV-SILC process in mechanism I_{D10}.

We now examine the LV-SILC peak in the substrate current at $V_G = -0.26$ V seen in Fig. 8. From Fig. 11, the transport paths involving electron tunneling that can lead to an increase in I_B at $V_G = -0.26$ V are electron tunneling from the n+ polysilicon CB into p-well interface traps followed by recombination with holes (mechanism I_{B1}) and electron tunneling from n+ polysilicon interface traps to p-well interface traps followed by recombination with holes (mechanism I_{B2}). The poststress activation energy (ΔH) for I_B is shown in Fig. 14. The substrate current for the peak at $V_G = -0.26$ V is thermally driven with an activation energy of 0.43 eV, which is on the order of $\frac{1}{2}E_G(\mathrm{Si})$. Additionally, the surface potential at $V_G = -0.26$ V is at approximately midgap for the p-well. Accordingly, this LV-SILC peak in the substrate current appears to be limited by electron-hole pair generation through midgap defects in the p-well created during stress. If the

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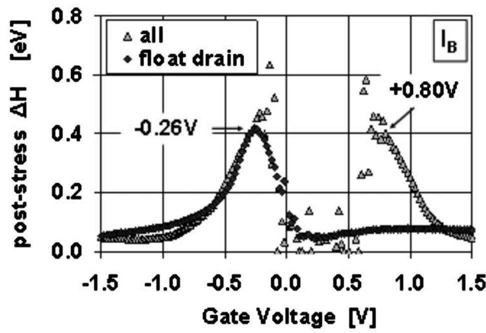

FIG. 14. Poststress substrate current activation energy vs gate voltage both with and without the drain floating during the sense operation.

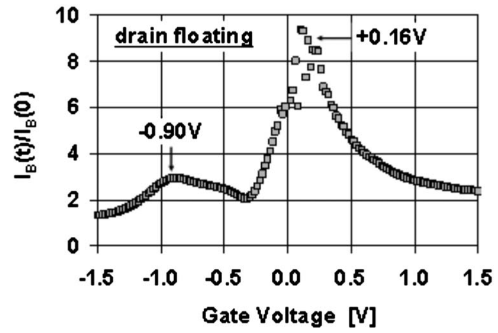

FIG. 16. $I_B(t)/I_B(0)$ at 378 K with the drain floating during the sense operation.

resulting hole is injected from the p-well into the $n+$ polysilicon, a substrate current would appear (mechanism I_{B13}). Therefore, in this voltage range, LV-SILC in the substrate terminal requires traps at the p-well interface. In Fig. 14, the peak in the ΔH versus V_G characteristic appears whether the drain is connected or floating, indicating that this is not a gate controlled diode surface state generation current[26,27] flowing through the p-well/NSD junction. The poststress activation energy for I_G is nearly identical to the substrate current at $V_G = -0.26$ V as shown in Fig. 15, indicating that the creation of electron-hole pairs through midgap defects in the p-well does indeed result in carrier (hole) injection into the gate terminal. This is the only LV-SILC peak that was observed to be dominated by hole tunneling. Note that no corresponding LV-SILC gate current peak is observed in Fig. 6. This appears to be consequent of the orders of magnitude difference between the gate and substrate currents. At time zero, the substrate current is 300 fA at $V_G = -0.26$ V. After stress, the increase in I_B at $V_G = -0.26$ V is 65 pA, while the magnitude of I_G is 100 times larger. The presence of a gate current LV-SILC component is detected only in the thermal activation of the gate current.

The change in substrate current with the drain floating is shown in Fig. 16. The gate current has the same features as Fig. 16 (not shown). The peak at $V_G = -0.90$ V is still present, in agreement with our analysis showing that traps at the p-well interface contribute to LV-SILC in this voltage range. Another peak in I_B appears at $V_G = +0.16$ V when the drain is floating. At this bias, I_G has decreased from 16 nA to 5 pA since the floating drain cannot supply inversion layer electrons. Concurrently, I_B has increased from 90 fA to 5 pA due to higher carrier generation rates resulting from the device being in deep depletion, so that this peak represents a small increase in current after stress. From Figs. 14 and 15, I_G and I_B are not strongly thermally activated at $V_G = +0.16$ V. Accordingly, carrier creation in the p-well is not dominated by either band gap or midgap generation. The most likely explanation for the LV-SILC peak in I_G and I_B at $V_G = +0.16$ V is the injection of electrons from the p-well CB created by BTBT into $n+$ polysilicon interface traps (mechanism I_{B4}), followed by thermal emission into the $n+$ polysilicon CB, as shown in Fig. 17.

We now turn our attention to the LV-SILC peak in the substrate current at $V_G = +0.72$ V that is detected when all terminals are connected during the sense procedure as shown in Fig. 8. There are no corresponding peaks in either I_G or I_D as shown in Figs. 6 and 7, respectively. Figure 14 shows that this peak has an activation energy of 0.4 eV, which is too high for tunneling of p-well VB electrons into $n+$ polysilicon interface states to be a viable explanation since the traps that are unoccupied are too close to the $n+$ polysilicon CB edge to result in a 0.4 eV tunneling barrier. This activation energy is also too high for BTBT, and generation of electron-hole pairs in the p-well through states within the silicon band gap is unlikely at this voltage since the p-well is in strong inversion. Tunneling of holes from the $n+$ polysilicon VB into p-well interface traps can also be ruled out since this would result in a LV-SILC peak in I_D due to recombination of inversion layer electrons (supplied by the drain) with the holes

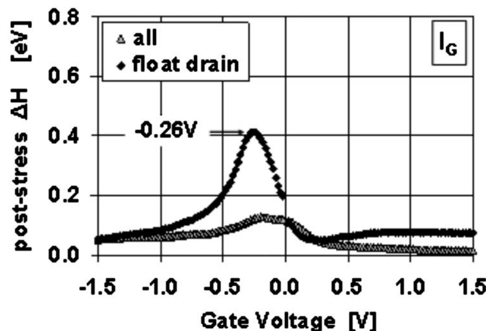

FIG. 15. Poststress gate current activation energy vs gate voltage both with and without the drain floating during the sense operation.

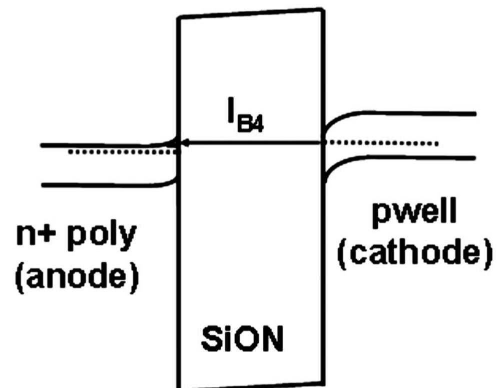

FIG. 17. Band diagram for LV-SILC at $V_G \sim +0.2$ V for tunneling processes between $n+$ polysilicon and p-well. The origin of electrons in the p-well CB is BTBT in the p-well space charge region.

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that are captured in p-well interface traps. Accordingly, there is no adequate explanation for this I_B peak that involves a tunneling process between $n+$ polysilicon and p-well. The most likely explanation is that electrons in the NSD surface space charge region tunnel from the NSD VB into traps and are subsequently emitted through a 0.4 eV thermal barrier into the NSD CB. The resultant hole is injected into the p-well VB (mechanism I_{B14}). For this peak, the sum of $V_G+\Delta H \sim E_G(\mathrm{Si})$ is consistent with a thermal emission tunneling process. Accordingly, the I_B peak at $V_G=+0.72$ V requires traps at the NSD-SiON interface and does not have an I_G component. Therefore, this peak in the substrate current is not a LV-SILC process. An I_D component must also be present but cannot be detected due to the much larger magnitude of the drain current. It is possible that the traps that give rise to this peak in the substrate current are the same that resulted in the dip in I_D at $V_G=-0.64$ V, as they are in approximately the same spatial location and energy position in the p-well band gap.

IV. DISCUSSION

Using carrier separation techniques in three-terminal devices to detect the increase in current with all terminals connected during sense, coupled with separate measurements where one terminal is floating during sense, a total of six peaks can be resolved in the poststress I-V spectra of SiON dielectrics. Five of these peaks (of which one is observed only when the drain is floating) give rise to LV-SILC, where carriers tunnel between either $n+$ polysilicon and p-well or between $n+$ polysilicon and NSD via interface traps at one or both interfaces. The sixth peak is due to thermal tunneling emission in the NSD/p-well junction. While poststress C-V measurements on these same samples detect only two interface trap peaks, both of which are located at the p-well interface,[12] LV-SILC provides a more sensitive resolution of the interface state spectra and detects traps at both polysilicon and p-well interfaces. Of the five trap peaks that contribute to LV-SILC, three are observed in the substrate current and three are observed in the drain current. Three peaks are of sufficient magnitude to be resolvable in the gate current, and a fourth peak in the gate current can identified from the poststress thermal activation energy. Our analysis shows that the most likely physical explanations for the five LV-SILC trap peaks observed in our data are as follows.

(1) $V_G \sim -1.02$ V: This peak is comprised of three components; electrons tunneling from $n+$ polysilicon interface traps into p-well interface traps, electrons tunneling from the $n+$ polysilicon CB into p-well interface traps, and electrons tunneling from $n+$ polysilicon interface traps into the p-well CB. Accordingly, this peak senses traps at both interfaces.

(2) $V_G=-0.64$ V: This peak (corresponding to a reduction in I_D) is due to electrons tunneling from the $n+$ polysilicon CB into p-well interface traps near the NSD edge. The capture of these electrons into p-well interface states reduces the number of electrons that flow out of the drain relative to the unstressed condition due to the trapped electrons recombining with holes. This peak senses traps at the p-well interface near the NSD.

(3) $V_G=-0.26$ V: This peak is due to electron-hole pair generation through midgap traps at the p-well interface, with the resulting hole tunneling from the p-well into $n+$ polysilicon. This is the only LV-SILC peak where holes are the dominant carriers that are injected across the gate dielectric. This peak senses traps at the p-well interface.

(4) $V_G=-0.14$ V: This peak is due to electrons tunneling from $n+$ polysilicon interface traps into the NSD CB. This peak senses traps at the $n+$ polysilicon interface.

(5) $V_G=+0.16$ V: This peak is only observed with the drain floating and is due to tunneling of p-well CB electrons created through BTBT into $n+$ polysilicon interface traps. For this peak, traps involved in the LV-SILC process are located at the $n+$ polysilicon interface.

TABLE I. Summary of the NMOS interface trap peaks sensed by LV-SILC in each device terminal.

V_{peak} (V)	Terminals sensing traps at polysilicon-SiON interface	Terminals sensing traps at p-well-SiON interface
−1.02	I_D, I_G	I_B, I_G
−0.64		I_B, I_D, I_G
−0.26		I_B, I_G
−0.14	I_D, I_G	
+0.16	I_B, I_G	

When LV-SILC in the gate terminal is sensed at V_{FB}, traps at both $n+$ polysilicon and p-well interfaces are involved in the transport process. It has been suggested that LV-SILC is only due to tunneling from the $n+$ polysilicon CB to p-well interface states because this transition represents the minimum barrier height for this system.[14] However, the $n+$ polysilicon depletes as the gate voltage is swept toward 0 V, while interface traps below the Fermi level remain occupied. Accordingly, occupied $n+$ polysilicon interface traps that are located at energies just below the $n+$ polysilicon Fermi level would be expected to play a significant role in the LV-SILC process, which we have shown in this work through carrier separation measurements. The presence of the drain current LV-SILC peak near V_{FB} is consequent of a two-trap tunneling process.

V. CONCLUSIONS

For NMOS devices with ultrathin SiON gate dielectrics sensed at V_{FB}, poststress carrier separation measurements confirm that LV-SILC as measured in the gate current is a two-trap tunneling process involving traps at both $n+$ polysilicon-SiON and p-well-SiON interfaces. In the off state, LV-SILC in the substrate current only probes traps at the p-well-SiON interface. Depending on the value of the sense voltage chosen, LV-SILC in the drain terminal can probe traps at the $n+$ polysilicon-SiON interface or p-well-SiON interface. These findings are summarized in Table I.

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