REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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REV																				
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REV																				
SHEET	15	16	17	18	19	20	21	22												
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE
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DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE

REVISION LEVEL

MICROCIRCUIT, MEMORY, DIGITAL, 512K X 36 SYNCHRONOUS STATIC RANDOM ACCESS MEMORY (SRAM), 2.5 V, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-08234**

SHEET
1 OF 24

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	08234	01	N	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes N, Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Maximum operating speed
01		512K X 36 CMOS SRAM	250 MHz
02		512K X 36 CMOS SRAM	200 MHz
03		512K X 36 CMOS SRAM	167 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N	Certification and qualification to MIL-PRF-38535 for plastic encapsulated microcircuit (PEM)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Thin quad flat pack (TQFP)
Y	See figure 1	165	Fine ball grid array (FBGA)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q and V.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD})	-0.3 V dc to + 3.6 V dc
Voltage range on V_{DDQ}	-0.3 V dc to V_{DD}
Voltage range on any output in tri-state	-0.5 V dc to V_{DDQ} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	
01	1.26 W
02	1.08 W
03	0.99 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	4.08 °C/W 3/
Case Y	4.0 ˚C/W 3/
Junction temperature (T_J)	+140°C 4/
Output current	20 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	2.375 V dc to 2.625 V dc
Supply voltage to I/O (V_{DDQ})	2.375 V dc to V_{DD}
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	1.7 V dc to V_{DD} + 0.3 V dc 5/
Input low voltage range (V_{IL})	-0.3 V dc to 0.7 V dc 5/
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation. AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Tested initially and after any design or process changes that may affect these parameters.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Overshoot: $V_{IH}(AC) < V_{DDQ}$ +1.5V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).

ASTM Standard F1192-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

JEDEC Solid State Product Outline MO-216 - Thin Profile, Square and Rectangular, Ball Grid Array Family, 1.00 & 0.08MM Pitches

JEDEC Solid State Product Outline MS-026 - Low/Thin Profile Plastic Quad Flat Package, 2.00 mm Footprint, Optional Heat Slug

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests are used to test this device. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes N, Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q and V shall be in accordance with MIL-PRF-38535

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q and V, the requirements of MIL-PRF-38535.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $2.375\ V \le V_{DD} \le 2.625\ V$ $2.375\ V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/		Group A Subgroups	Device Type	Limits		Units
						Min	Max	
Output HIGH Voltage	V_{OH}	I_{OH} = -1.0 mA		1, 2, 3	All	2.0	---	V
Output LOW Voltage	V_{OL}	I_{OL} = 1.0 mA		1, 2, 3	All	---	0.4	V
Input HIGH Voltage	V_{IH}			1, 2, 3	All	1.7	V_{DD} + 0.3 V	V
Input LOW Voltage	V_{IL}			1, 2, 3	All	-0.3	0.7	V
Input Leakage Current	I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	1, 2, 3	All	-5	5	uA
		Input Current of MODE	Input = V_{SS}			-30	---	
			Input = V_{DD}			---	5	
		Input Current of ZZ	Input = V_{SS}			-5	---	
			Input = V_{DD}			---	30	
Output Leakage Current	I_{OZ}	GND ≤ V_I ≤ V_{DDQ}, output disabled		1, 2, 3	All	-5	5	uA
V_{DD} Operating Supply Current	I_{DD}	V_{DD} = max, I_{OUT}=0 mA $f = f_{MAX} = 1/t_{CYC}$	4-ns cycle, 250 MHz	1, 2, 3	01	---	350	mA
			5-ns cycle, 200 MHz		02	---	300	
			6-ns cycle, 167 MHz		03	---	275	
Automatic CE Power-Down Current - TTL Inputs	I_{SB1}	V_{DD} = max, device deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ $f = f_{MAX} = 1/t_{CYC}$	4-ns cycle, 250 MHz	1, 2, 3	01	---	160	
			5-ns cycle, 200 MHz		02	---	150	
			6-ns cycle, 167 MHz		03	---	140	
Automatic CE Power-Down Current - CMOS Inputs	I_{SB2}	V_{DD} = max, device deselected, $V_{IN} \le 0.3V$ or $V_{IN} \ge V_{DDQ} - 0.3V$, f = 0	All speeds	1, 2, 3	All	---	70	mA
Automatic CE Power-Down Current - CMOS Inputs	I_{SB3}	V_{DD} = max, device deselected or $V_{IN} \le 0.3V$ or $V_{IN} \ge V_{DDQ} - 0.3V$, $f = f_{MAX} = 1/t_{CYC}$	4-ns cycle, 250 MHz	1, 2, 3	01	---	135	mA
			5-ns cycle, 200 MHz		02	---	130	
			6-ns cycle, 167 MHz		03	---	125	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $2.375\ V \le V_{DD} \le 2.625\ V$ $2.375\ V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/		Group A Subgroups	Device Type	Limits		Units
						Min	Min	
Automatic CE Power-Down Current - TTL Inputs	I_{SB4}	V_{DD} = max, device deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0	All speeds	1, 2, 3	All		80	mA
Snooze Mode Standby current	I_{DDZZ}	$ZZ \ge V_{DD} - 0.2V$		1, 2, 3	All		80	mA
Input Capacitance 1/	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V, V_{DDQ} = 3.3V	Case X	4	All		5	pF
			Case Y				9	
Clock Input Capacitance 1/	C_{CLK}		Case X	4	All		5	pF
			Case Y				9	
Input/Output Capacitance 1/	$C_{I/O}$		Case X	4	All		5	pF
			Case Y				9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $2.375\ V \le V_{DD} \le 2.625\ V$ $2.375\ V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Clock Cycle Time	t_{CYC}	See Figure 5 as applicable. 4/ 8/ 9/	9, 10, 11	01	4.0	---	ns
				02	5.0	---	
				03	6.0	---	
Clock HIGH	t_{CH}		9, 10, 11	01	1.7	---	ns
				02	2.0	---	
				03	2.2	---	
Clock LOW	t_{CL}		9, 10, 11	01	1.7	---	ns
				02	2.0	---	
				03	2.2	---	
Data Output valid after CLK rise	t_{CO}		9, 10, 11	01	---	2.6	ns
				02	---	3.0	
				03	---	3.4	
Data Output hold after CLK rise	t_{DOH}		9, 10, 11	01	1.0	---	ns
				02	1.3	---	
				03	1.3	---	
Clock to Low-Z 5/ 6/ 7/	t_{CLZ}		9, 10, 11	01	1.0	---	ns
				02	1.3	---	
				03	1.3	---	
Clock to High-Z 5/ 6/ 7/	t_{CHZ}		9, 10, 11	01	---	2.6	ns
				02	---	3.0	
				03	---	3.4	
$\overline{OE}$ Low to Output valid	t_{OEV}		9, 10, 11	01	---	2.6	ns
				02	---	3.0	
				03	---	3.4	
$\overline{OE}$ Low to Output Low-Z 5/ 6/ 7/	t_{OELZ}		9, 10, 11	01	0		ns
				02	0		
				03	0		
$\overline{OE}$ High to Output High-Z 5/ 6/ 7/	t_{OEHZ}		9, 10, 11	01	---	2.6	ns
				02	---	3.0	
				03	---	3.4	
Address setup before CLK rise	t_{AS}		9, 10, 11	01	1.2	---	ns
				02	1.4	---	
				03	1.5	---	
$\overline{ADSC}$, $\overline{ADSP}$ Setup before CLK rise	t_{ADS}		9, 10, 11	01	1.2	---	ns
				02	1.4	---	
				03	1.5	---	
$\overline{ADV}$ setup before CLK rise	t_{ADVS}		9, 10, 11	01	1.2	---	ns
				02	1.4	---	
				03	1.5	---	
$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup before CLK rise	t_{WES}		9, 10, 11	01	1.2	---	ns
				02	1.4	---	
				03	1.5	---	
Data Input setup before CLK rise	t_{DS}		9, 10, 11	01	1.2	---	ns
				02	1.4	---	
				03	1.5	---	

See footnotes at end of table.

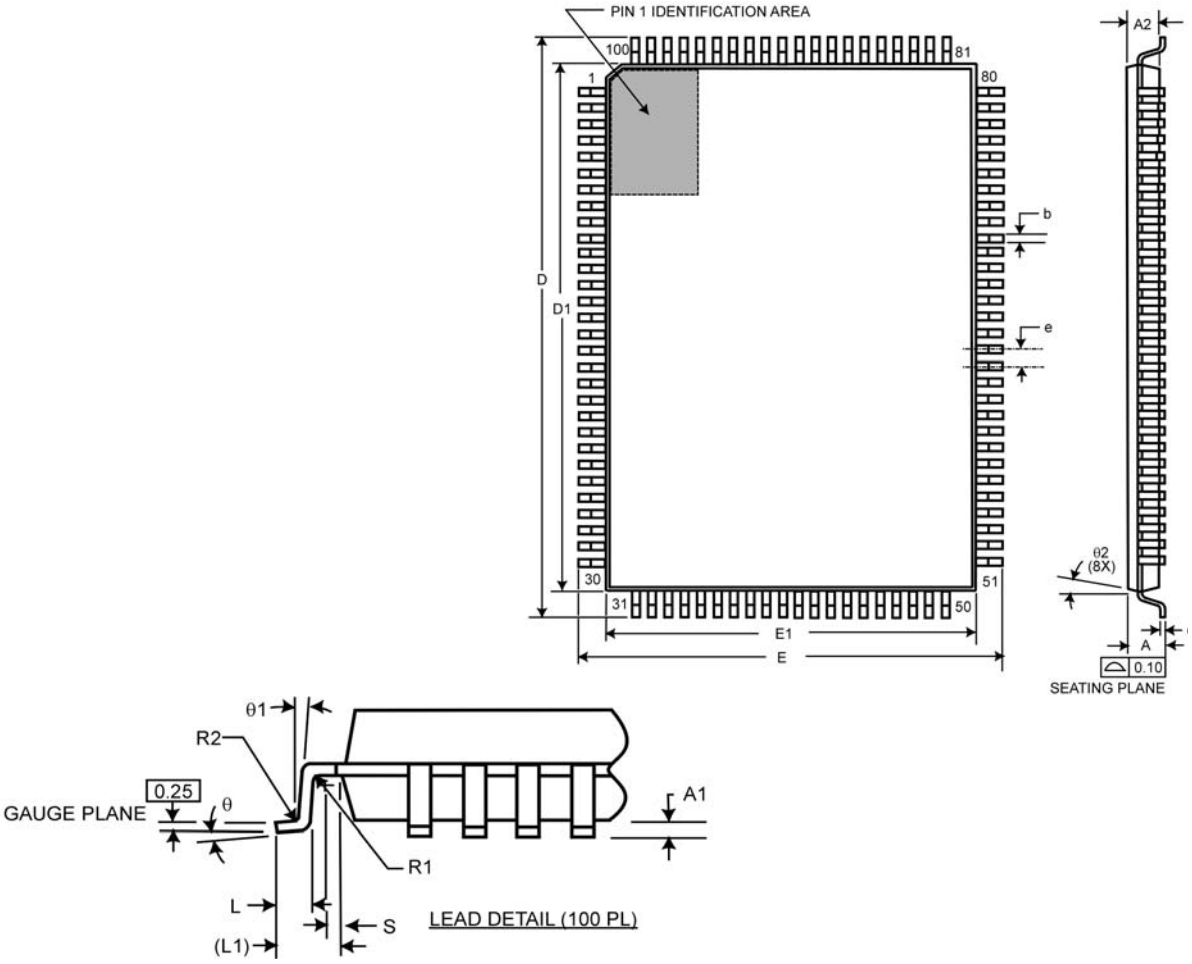
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $2.375\ V \le V_{DD} \le 2.625\ V$ $2.375\ V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Chip Enable setup before CLK rise	t_{CES}		9, 10, 11	01	1.2	---	ns
				02	1.4	---	
				03	1.5	---	
Address Hold after CLK rise	t_{AH}		9, 10, 11	01	0.3	---	ns
				02	0.4	---	
				03	0.5	---	
$\overline{ADSC}$, $\overline{ADSP}$ hold after CLK rise	t_{ADH}		9, 10, 11	01	0.3	---	ns
				02	0.4	---	
				03	0.5	---	
$\overline{ADV}$ hold after CLK rise	t_{ADVH}		9, 10, 11	01	0.3	---	ns
				02	0.4	---	
				03	0.5	---	
$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_X$ hold after CLK rise	t_{WEH}		9, 10, 11	01	0.3	---	ns
				02	0.4	---	
				03	0.5	---	
Data input hold after CLK rise	t_{DH}		9, 10, 11	01	0.3	---	ns
				02	0.4	---	
				03	0.5	---	
Chip Enable hold after CLK rise	t_{CEH}		9, 10, 11	01	0.3	---	ns
				02	0.4	---	
				03	0.5	---	
Device Operation to ZZ	t_{ZZS}	$ZZ \ge V_{DD} - 0.2V$	9, 10, 11	All	---	$2t_{CYC}$	ns
ZZ recovery time	t_{ZZREC}	$ZZ \le 0.2V$	9, 10, 11	All	$2t_{CYC}$	---	ns
ZZ active to snooze current 7/	t_{ZZI}		9, 10, 11	All	---	$2t_{CYC}$	ns
ZZ inactive to exit snooze current 7/	t_{RZZI}		9, 10, 11	All	0	---	ns

TABLE I. Electrical performance characteristics - Continued.

1/ Tested initially and after any design or process changes that may affect these parameters.
2/ All voltage referenced to ground.
3/ Overshoot: $V_{IH}(AC) < V_{DDQ} + 1.5V$ (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -2$ (Pulse width less than $t_{CYC}/2$).
4/ Power up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time, $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
5/ t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in Figure 4 (b), AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
6/ At any given voltage and temperature , t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
7/ This parameter is sampled and not 100% tested.
8/ Timing reference level is 1.25V when V_{DDQ} = 2.5V.
9/ Test conditions shown in figure 4 (a), AC Test Loads unless otherwise noted.

Case X (see notes)

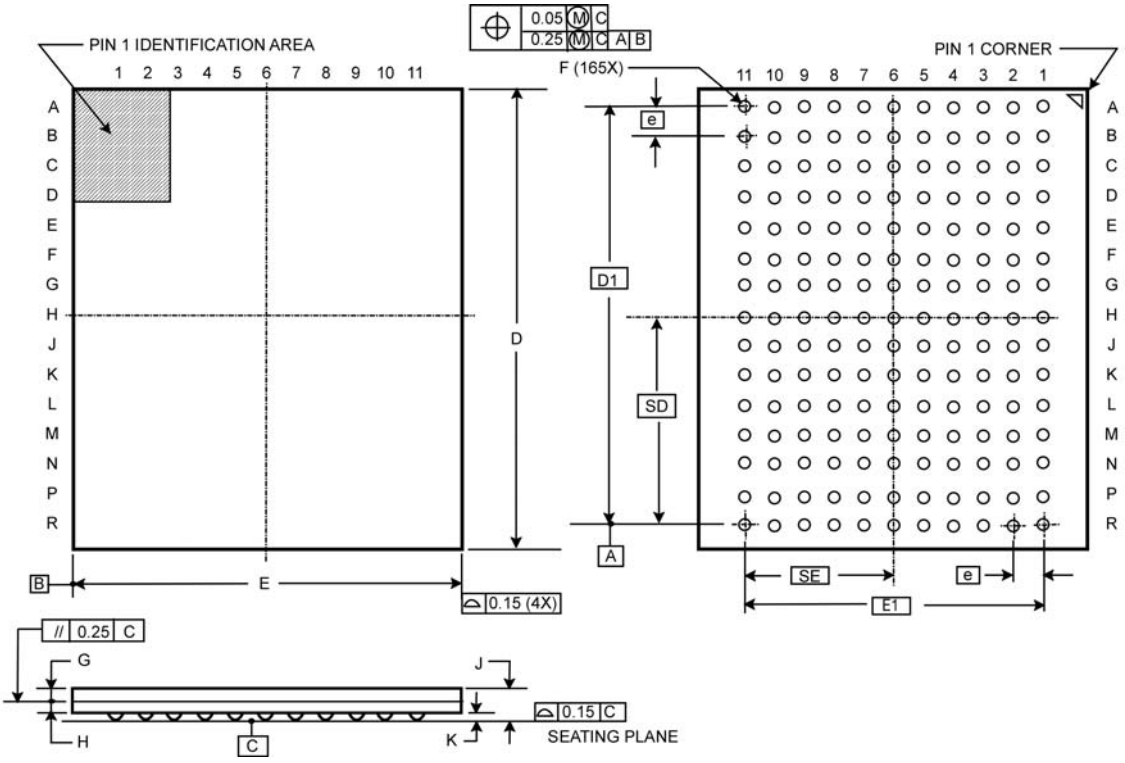


Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	---	---	1.60	e	---	0.65	---
A1	0.05	---	0.15	L	0.45	0.60	0.75
A2	1.35	1.40	1.45	L1	---	1.00	---
b	0.22	0.30	0.38	R1	0.08	---	0.20
c	---	---	0.20	R2	0.08	---	0.20
D	21.80	22.00	22.20	θ	0°	---	7°
D1	19.90	20.00	20.10	θ1	0°	---	---
E	15.80	16.00	16.20	θ2	11°	12°	13°
E1	13.90	14.00	14.10	N	100		

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.
2. Ref: JEDEC MS-026 (BHA)

Figure 1. Case outlines.-continued.

Case Y (see notes)

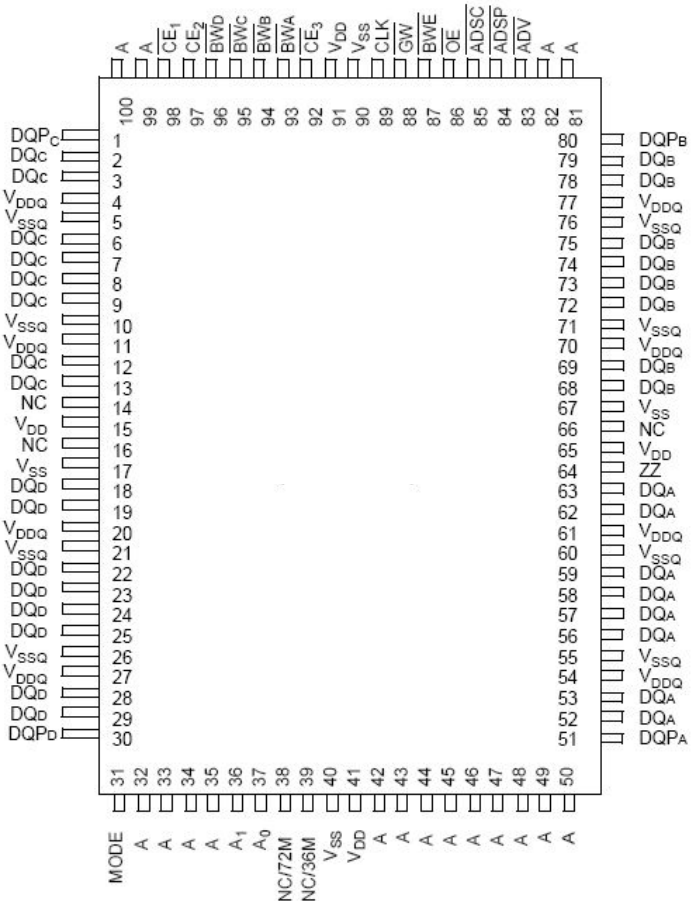


Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
D	14.90	15.00	15.10	H	0.31	0.36	0.41
D1	---	14.00 BSC	---	J	---	---	1.40
E	12.90	13.00	13.10	K	0.29	0.35	0.41
E1	---	10.00 BSC	---	SD	---	7.00 BSC	---
e	---	1.00 BSC	---	SE	---	5.00 BSC	---
f	0.44	0.50	0.64	N	165		
g	0.48	0.53	0.58				
D	14.90	15.00	15.10				

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.
2. Ref: JEDEC MO-216 for ball pattern.

Figure 1. Case outlines.- continued

Case X (100TQFP)



Case Y (165 FBGA)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Figure 2. Terminal connections.

Pin definitions

Pin	Name	Function
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the 128K address locations.** Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. A_1, A_0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte Write Select Inputs, active LOW.** Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW.** Sampled on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, active LOW.** Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input Clock	**Clock Input.** Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, active LOW.** Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH.** Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW.** Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, active LOW.** Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW.** When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW.** When asserted LOW, addresses presented to the device are captured in the address registers. A_1, A_0 are also loaded onto the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ADSP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.** When asserted LOW, addresses presented to the device are captured in the address registers. A_1, A_0 are also loaded onto the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, active HIGH.** When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQPx	I/O- Synchronous	**Bidirectional Data I/O lines.** As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit.** Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin must be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit.** Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit.** Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected and connected to V_{DD}. This pin is not available on TQFP packaging.
TCK	JTAG-clock	**Clock input to the JTAG circuitry.** If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available in TQFP packaging.
V_{DD}	Power Supply	**Power Supply Inputs to the core of the device.**
V_{SS}	Ground	**Ground for the core of the device.**

FIGURE 2. Terminal connections- continued

Pin definitions. – continued.

Pin	Name	Function
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O circuitry.**
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry.**
MODE	Input-Static	**Selects Burst Order.** When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC	----	**No Connects.** 36M, 72M, 144M, 288M, 576M and 1G are address expansion pins and are not internally connected to the die.

FIGURE 2. Terminal connections- continued

Truth Table 1/ 2/ 3/ 4/ 5/

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L-H	Tri-State
Snooze Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Partial Truth Table for Read/Write 1/ 6/

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A - DQ_A and DQP_A	H	L	H	H	H	L
Write Byte B - DQ_B and DQP_B	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C- DQ_C and DQP_C	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D - DQ_D and DQP_D	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Figure 3. Truth table and device operations.

Notes:
1/ X = "Don't Care." H = Logic HIGH, L = Logic LOW.
2/ $\overline{\text{WRITE}}$= L when any one or more Byte Write enable signals ($\overline{\text{BW}}_A$, $\overline{\text{BW}}_B$, $\overline{\text{BW}}_C$, $\overline{\text{BW}}_D$) and $\overline{\text{BWE}}$ = L or $\overline{\text{GW}}$ = L. $\overline{\text{WRITE}}$= H when all Byte write enable signals ($\overline{\text{BW}}_A$, $\overline{\text{BW}}_B$, $\overline{\text{BW}}_C$, $\overline{\text{BW}}_D$), $\overline{\text{BWE}}$, $\overline{\text{GW}}$= H.
3/ The DQ pins are controlled by the current cycle and the $\overline{\text{OE}}$ signal. $\overline{\text{OE}}$ is asynchronous and is not sampled with the clock.
4/ The SRAM always initiates a read cycle when $\overline{\text{ADSP}}$ is asserted, regardless of the state of $\overline{\text{GW}}$, $\overline{\text{BWE}}$, or $\overline{\text{BW}}_{[A;D]}$. Writes may occur only on subsequent clocks after the $\overline{\text{ADSP}}$ or with the assertion of $\overline{\text{ADSC}}$. As a result, $\overline{\text{OE}}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{\text{OE}}$ is a don't care for the remainder of the write cycle.
5/ $\overline{\text{OE}}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all date bits are tri-state when $\overline{\text{OE}}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{\text{OE}}$ is active (LOW).
6/ Table only lists a partial listing of the byte write combinations. Any combination of $\overline{\text{BW}}_X$ is valid. Appropriate write will be done based on which byte write is active.

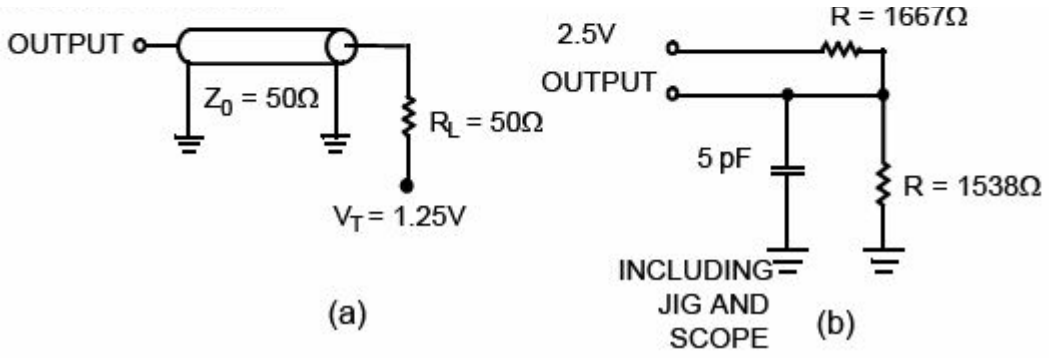
Interleaved Burst Address Table
(MODE = Floating or V_{DD})

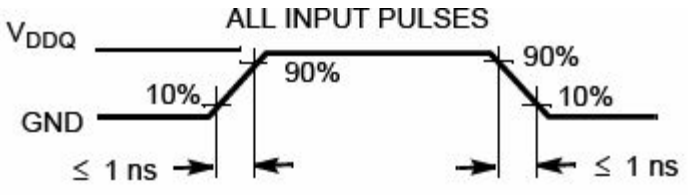
First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table
(MODE = GND)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Figure 3. Truth table and device operations.–continued.

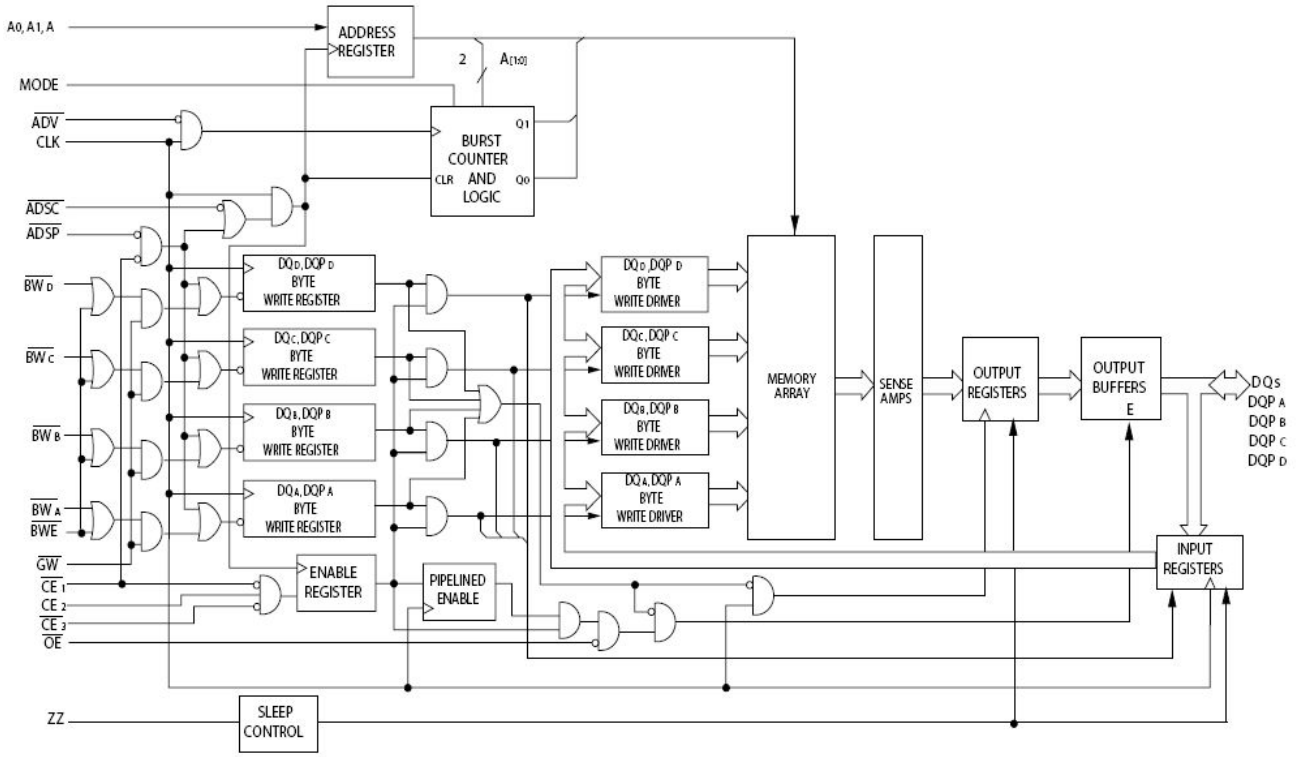




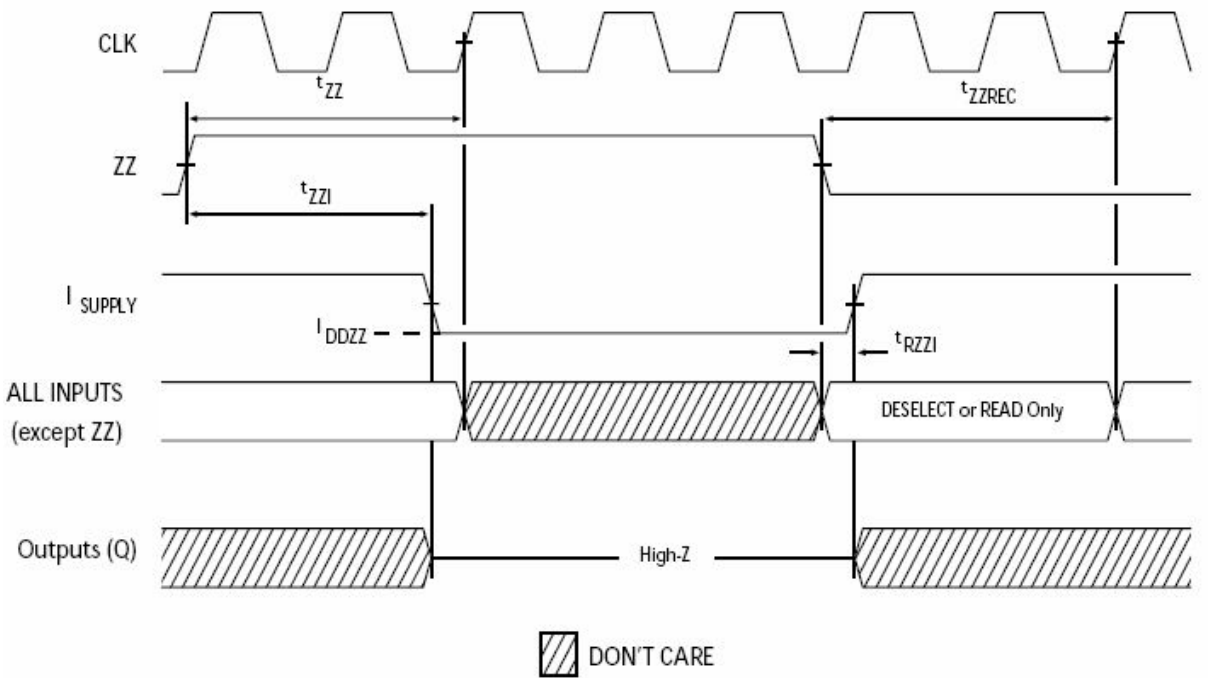
NOTES:
1. Use these output load circuits or equivalent for testing.
2. Capacitive load consists of all components of the test environment, including jig and scope.

Figure 4. Output load circuits.

BLOCK DIAGRAM



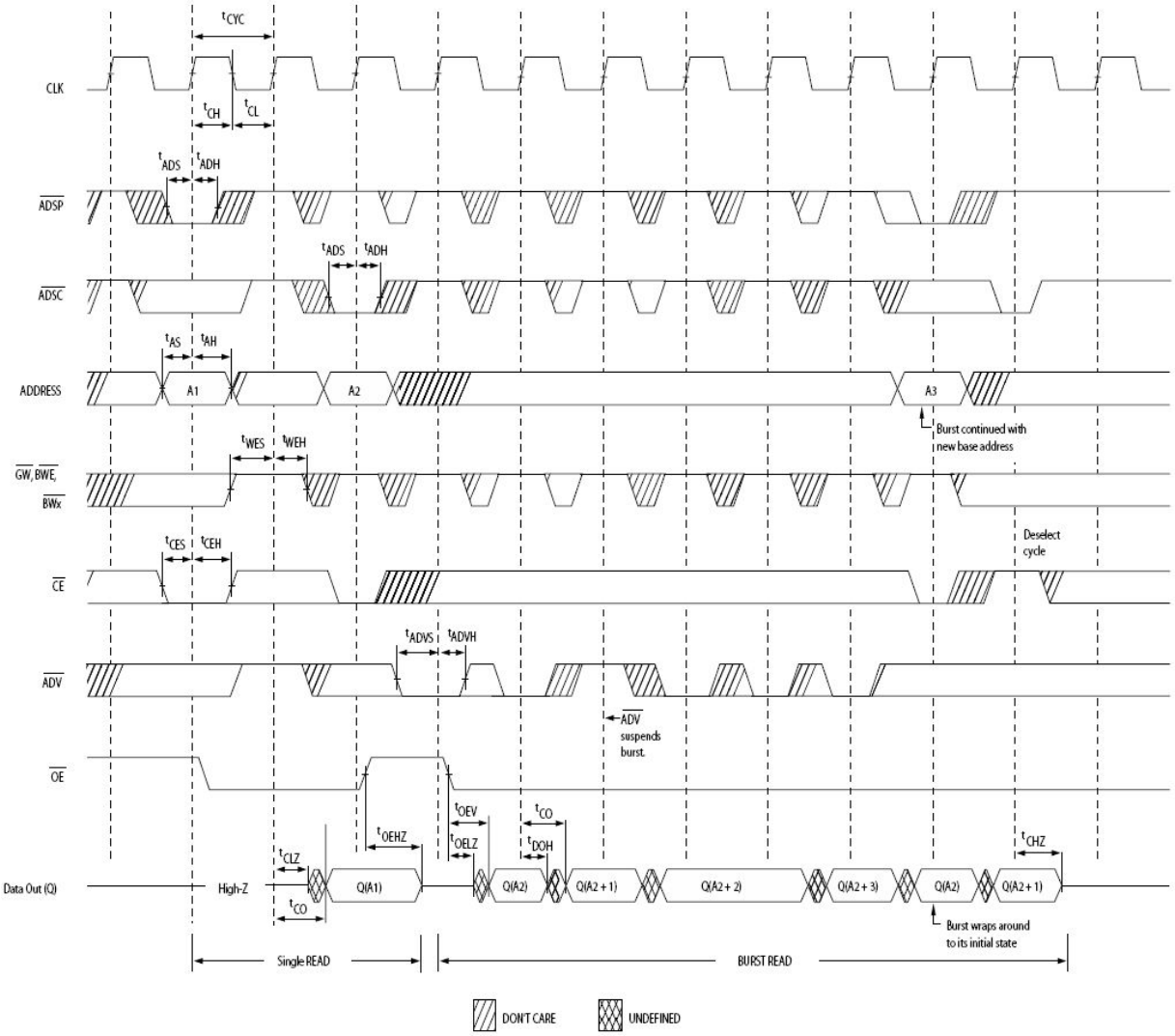
ZZ MODE TIMING 1/ 2/



NOTES:
1/ Device must be deselected when entering ZZ mode. See the Truth Table for all possible signal conditions to deselect the device.
2/ DQs are high-Z when exiting ZZ sleep mode.

Figure 5. Timing waveforms.

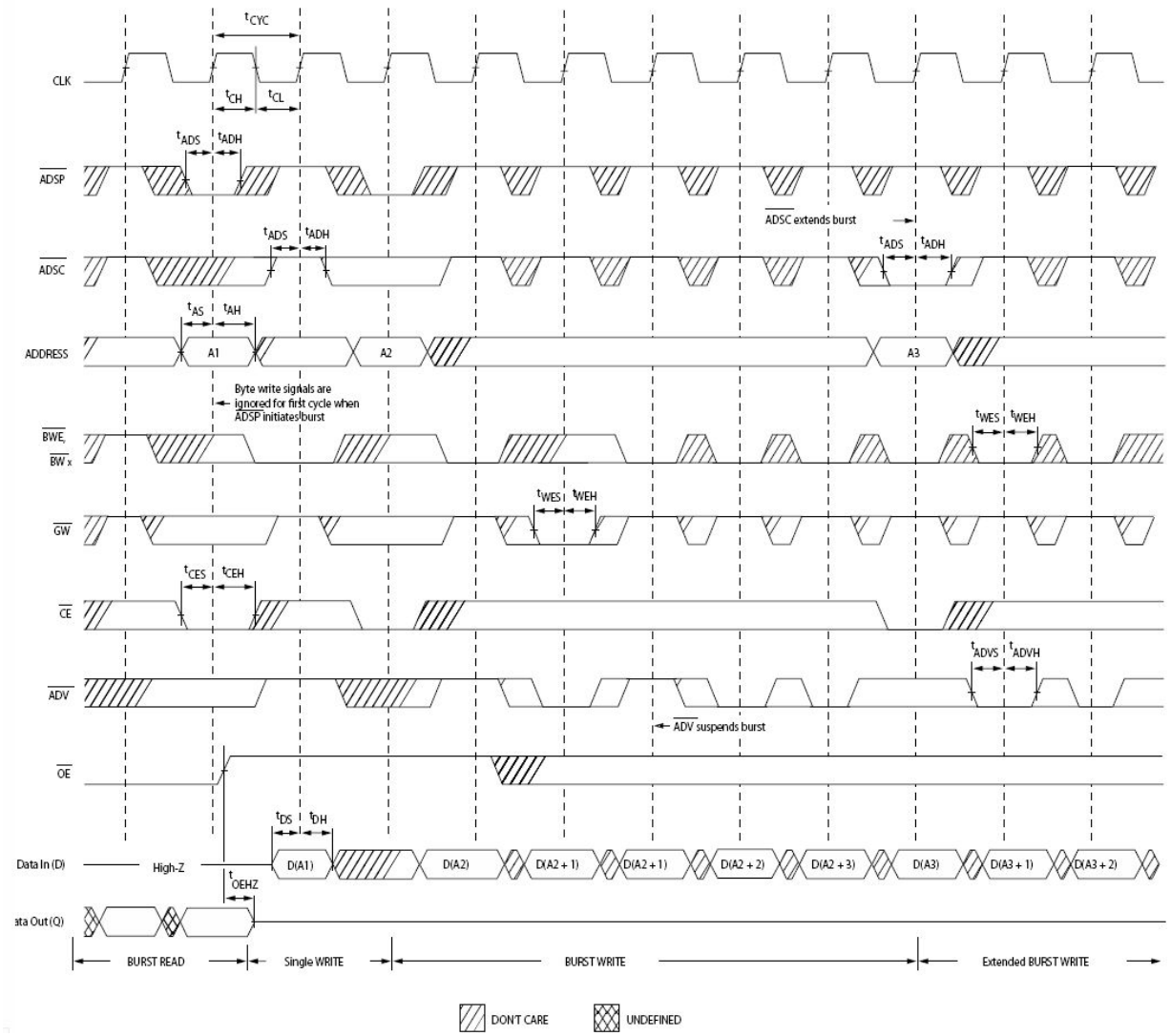
READ CYCLE TIMING 3/



NOTES:
3/ On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Figure 5. Timing waveforms - continued

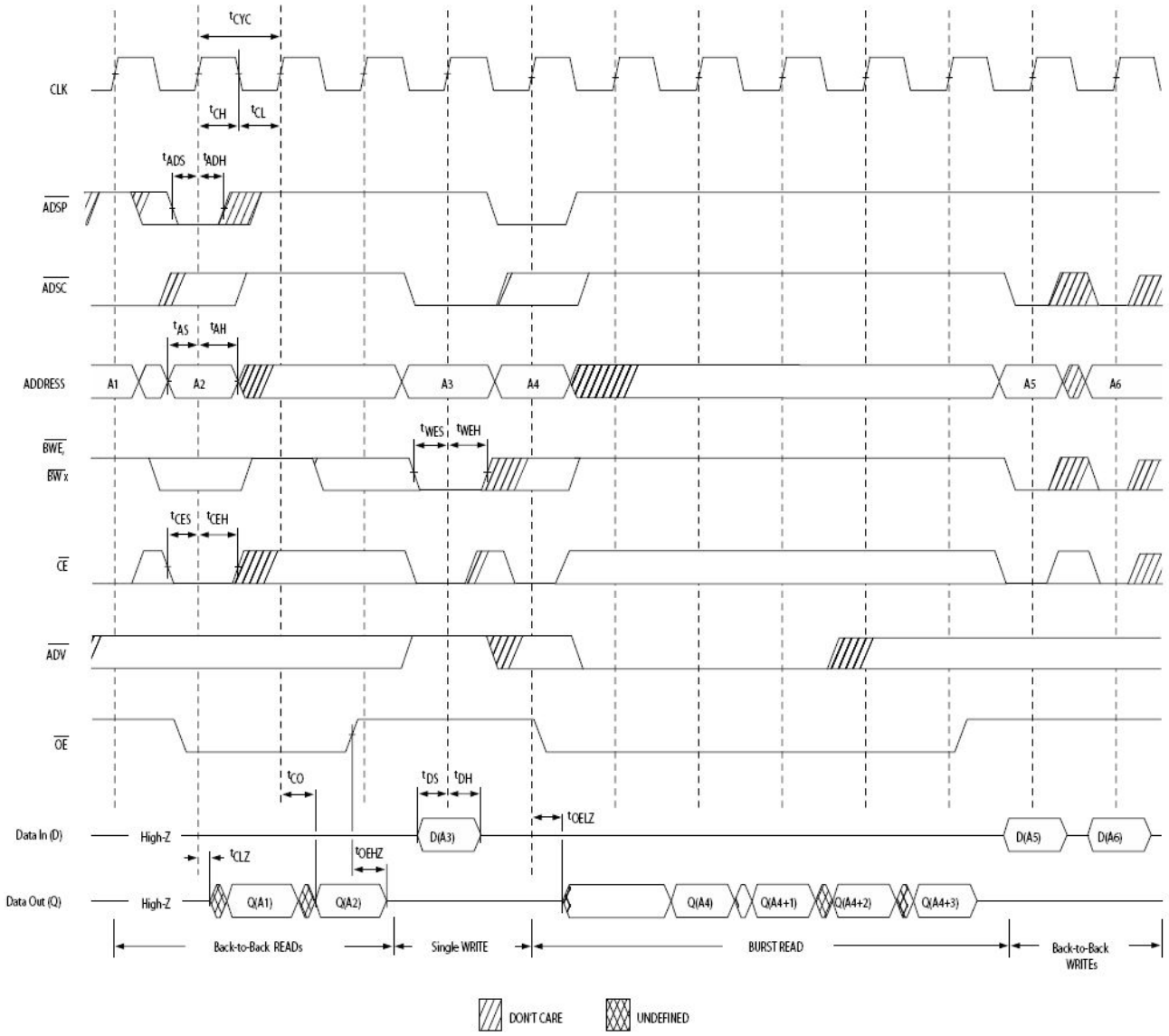
WRITE CYCLE TIMING 4/



NOTES:
4/ Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Figure 5. Timing waveforms - continued

READ / WRITE CYCLE TIMING 5/ 6/



NOTES:
5/ The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.
6/ $\overline{\text{GW}}$ is HIGH.

Figure 5. Timing waveforms - continued

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/

Line No.	Test Requirements	Subgroups (In accordance with MIL-PRF-38535, Table III)		
		Device Class N	Device Class Q	Device Class V
1	Interim electrical parameters (See 4.2)			1, 7, 9
2	Static Burn-In I Method 1015	Not Required	Not required	Required
3	Same as Line 1			1*, 7* Δ
4	Dynamic Burn-In (Method 1015)	Required	Required	Required
5	Same as Line 1			1*, 7* Δ
6	Final Electrical Parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A Test Requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7,8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7,8A, 8B, 9, 10, 11
8	Group C End-Point Electrical Parameters	2, 3, 7, 8A, 8B	2, 3,7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D End-Point Electrical Parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E End-Point Electrical Parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.
8/ Group A testing is not required if the requirements of MIL-PRF-38535 appendix B paragraph (B.4.2.a) have been accomplished.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	All device types
I_{SB2}, I_{SB4}	±10% of specified value in table I
I_X, I_{OZ}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q and V. Qualification inspection for device classes N, Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein. Group A testing is not required if all tests have been performed during final electrical of the 100% Screening test. See footnote 8/ for table IIA.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes N, Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes N, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes N, Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25ºC ±5ºC, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q and V.

5.2 Special Class N handling. Class N device is rated as a Moisture Sensitivity Level 3 part when tested per J-STD-020A. Device will be baked and dry packed when shipped from the manufacturer. Device will require a 125°C dry bake for 24 hours prior to installation if prolonged exposure on normal factory floor of the end user has occurred.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

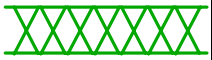
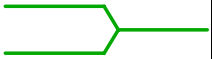
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the

system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-XX-XX

Approved sources of supply for SMD 5962-08SMD are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0823401NXA	6S055	DPA1380DV2525003A
5962-0823402NXA	6S055	DPA1380DV2520003A
5962-0823403NXA	6S055	DPA1380DV2516603A
5962-0823401NYA	6S055	DPA1380DV2525005A
5962-0823402NYA	6S055	DPA1380DV2520005A
5962-0823403NYA	6S055	DPA1380DV2516605A

1/ The lead finish shown for each PIN is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
6S055	DPA Components International 2251 Ward Avenue Simi Valley, CA 93065

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.