Low Leakage Power 8T SRAM Cell based on Self Controllable Voltage Level Logic

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Abstract - Low power and SRAM cells are in high demand nowadays. This paper presents a stable differential SRAM cell that consumes low power. The planned cell has similar structure to traditional 6T SRAM cell with the addition of two buffer transistors, one tail junction transistor and one complementary word line. Attributable to stacking result, the planned cell achieves lower power dissipation. This work proposes a sturdy, low power overwhelming, high noise tolerant differential 8T SRAM cell. Associate in nursing analysis on impact of method and voltage variations on varied parameters like browse current, access delay, browse stability, hold power etc. are given. This paper compares the performance of 3 SRAM cell topologies, that conventional 6T Cell, low power 8T SRAM LPT8 and the proposed SVL based 8T SRAM. All the simulations are carried out in Tanner EDA13.0V, 250nm model files.

Keywords - Self Controllable Voltage Level (SVL); 8T SRAM; Low Power SRAM; Cache Memory; Memory Design.

I. INTRODUCTION

STATIC RANDOM ACCESS MEMORY (SRAM) are used as cache memory that is embedded in silicon chip, System-on-Chip (SoC), Network-on-Chip (NoC) product. This can be attributable to the very fact that they're quick compared to DRAM (such as DRAM) and main memory (DRAM) They're unreal on an equivalent die with processors. As expressed by ITRS,90% of the processor's chip space is occupied by SRAM Terribly high increment in processor's speed is ascertained in recent years, however, the speed of memory has not got such an out sized increment. Thus, a spot between activity capability of memory and processor is widening with time. To cut back that gap, semiconducting material business is embedding memory on give the shape of cache memory. So as to realize quicker cache memory, SRAM cell needs to be faster.

For increasing the speed, the threshold voltage of MOSFETs needs to be decreased. However, there is a limit up to which threshold voltage can be decreased. Furthermore, due to fluctuation in threshold voltage there is a large variation in static noise margin (SNM). Moreover, the noise margin is a more critical parameter at the time of read operation than at the time hold operation. SNM is affected by technology and supply voltage scaling thus, an SRAM cell is required to be faster and disturb-free during read operation. SRAM cells are used in almost all digital systems and high-performance processors. Emerging applications, like wireless body sensing network, bioelectronics and implanted medical instruments demand for power efficient SRAM. Design of a power efficient SRAM cell is one of the most important factors while trying to achieve better chip performances. More than 40% of the active energy is consumed because of leakage currents in modern high-performance processors.

An array of SRAM cells is a major source of leakage currents in modern high-performance processors because a large number of transistors are used in today's on-chip cache memory. Therefore, it is imperative to design a low leakage SRAM cell By reducing the supply voltage (VDD), dynamic power Decreases quadratically and first-order leakage power decreases linearly. Therefore, by operating the cell in subthreshold region (i.e. by lowering the supply voltage below threshold voltage), it is possible to achieve low power SRAM cell In deep sub-micrometer (below 100-nm) technologies, 6T SRAM cell faces many challenges in the subthreshold region. Conventional 6T SRAM (Fig.2) cells exhibit poor read stability when operated at low supply voltage. Due to poor read SNM in a 6T SRAM cell, read upset may occur (i.e. Data stored in a cell may flip during a read operation). The 6T cell also shows larger variability (less reliable) in sub-micrometer technology due to variation in process Parameters to overcome the problem of read stability, several SRAM cells are proposed which have some additional supportive peripherals circuits.

These cells can be classified into two categories – single-ended SRAM cells and differential SRAM cells, Generally, a single-ended SRAM cell is not that much robust as a differential one. Therefore, it needs some additional compensation technique to maintain reliability as proposed in. Bit- line leakage in a single-ended SRAM cell is data dependent. This is because the overall bit- line leakage depends strongly on the data stored by the cell column being accessed. Therefore, there is a variation in the bit- line leakage from one cell column to another due to which access time distribution for an SRAM cell is highly dispersed. Moreover, single-ended SRAM cells suffer from sense margin problem during read operation. To improve read stability several differential SRAM cells are also proposed. These cells show improvement in read stability at an expense of larger area penalty. Furthermore, to improve the variability of an SRAM cell a transmission gate based 8T SRAM cell (TG8T) is proposed. However, this cell sub-

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The contribution of this paper is summarized as follows:

• The proposed cell uses differential structure. Therefore, its sense margin is improved.

• It shows larger read current, Transistor sizing is an important factor shorter read delay, better read stability.

• SVL LP8T also shows robustness to process parameter and voltage variations.

• The proposed cell also shows higher read current to leakage current ratio and less leakage power consumption.

The rest of the paper is organized as follows. In Section II, LP 8T cell and its operation in read, write and hold mode are described. In Section III, the simulation results and discussion are presented. Finally, Section IV concludes this paper.

II. 8T SRAM CELLS DESIGN

In this work, a low-power 8T SRAM cell (LP8T) is proposed (see Fig. 1). In order to achieve improved performance and density, device scaling is done. The proposed cell is very similar to the conventional 6T, except the two extra buffer transistors (MN5/6), one tail-transistor (MN7) and one complimentary word line (WWLB). The proposed architecture is shown in Fig. 2.

However, this cell during read operation one of the buffer transistor (gate of which is connected to node, storing '1') conducts. Because of these buffer transistors, read stability is improved (explained in Section III-E). Because of tail transistor and WWLB, hold power consumption is minimized (explained in Section III-H). Transistor sizing is an important factor for an SRAM cell.

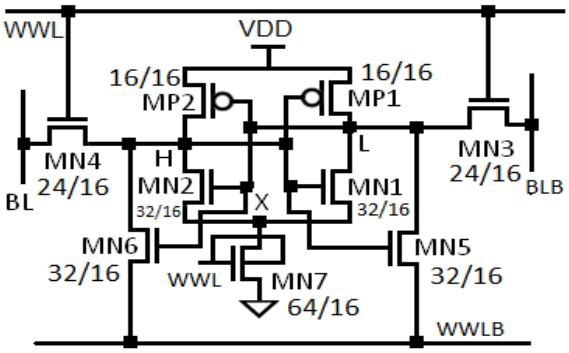

Figure 1: Low Power Consuming 8T SRAM cell (LP8T).

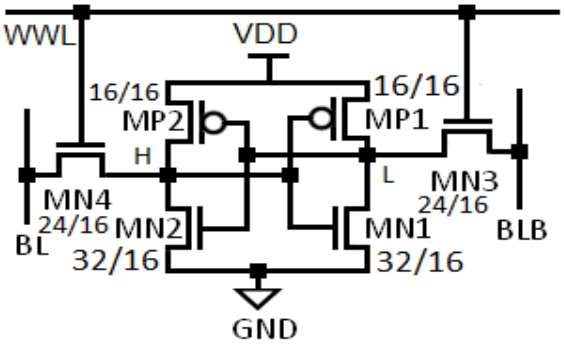

Figure 2: Standard 6T SRAM cell (D6T).

A. Read Operation

The read operation is performed by pre charging the bit-lines(BL and BLB) to VDD, then raising WWL to VDD and lowering WWLB to GND. Transistor MN7 is turned ON (as WWL is high) during read operation. Depending upon the content of the storage nodes (H/L), one of the buffer transistors (MN5/6) conducts. BLB/BL discharges through access transistors (MN3/4), followed by two paths, one through buffer transistor (MN5/6) and WWLB, other through pull-down transistor (MN1/2) and tail-transistor MN7. This results in faster read operation. For instance, if storage node H stores logic '1', pull-down transistor MN1 and buffer transistor MN5 conduct. Therefore, BLB finds two paths to discharge. One through MN3/1/7 and other through MN3/5/WWLB, while BL is held at VDD as MN6 and MN2 are OFF (due to logic '0' stored at node L) (see Fig. 4). The stored data is deciphered by sensing the potential difference between BL and BLB, as is done by the sense amplifier.

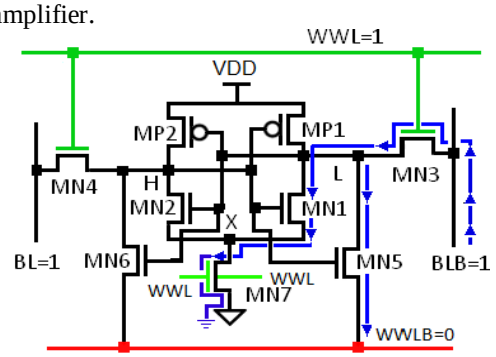

Figure 3: Read Operation of the proposed LP8T

B. Write Operation

During write operation WWL is raised to VDD. Therefore, the complementary of WWL (i.e. WWLB) is pulled down. Because of high WWL, both the access transistors (MN3/4) are ON. Transistor MN7 is kept ON (as WWL is high). Let's assume initially storage node H stores logic '1' and L stores logic '0'. Now to write '1' at L and '0' at H, BLB and BL are loaded with '1' and '0' respectively by write driver (not shown). Storage node H discharges through MN4 by BL. Simultaneously, voltage at node L increases towards VDD through MN3 by BLB (see Fig. 5). Note that, for brief initial time node L discharges through MN1/7 to GND and MN5 by WWLB but for brief final time node H discharges through MN2/7 to GND and MN6 by WWLB. Therefore, the desired data is written successfully.

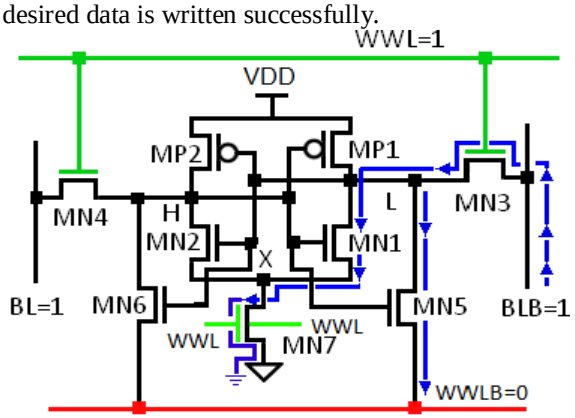

Figure 4: LP 8T SRAM cell

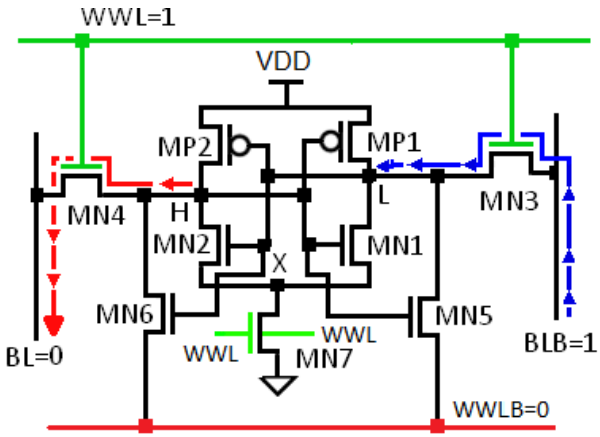

Figure 5: Write Operation of the proposed 8T SRAM cell

C. Hold Operation

The hold operation is performed by lowering WWL to GND (WWLB is at VDD). Thus, the access transistors MN3 and MN4 are OFF. Transistor MN7 is kept OFF during hold operation. The reason behind keeping WWLB at VDD and transistor MN7 OFF, are to achieve less leakage current. Leakage current increases on increasing the number of junctions due to extra cell transistors. However, the leakage current in the proposed cell is comparable to that of 6T SRAM cell.

III. SRAM USING SELF-CONTROLLABLE VOLTAGE LEVEL TECHNIQUE

A SRAM which provides low leakage power is designed in this paper. A new leakage current reduction circuit called an "improved Self-controllable Voltage Level (SVL)" circuit is developed and included to reduce the leakage power of SRAM. There are two well-known techniques that reduce leakage power (Pst). One is to use a multi-threshold-voltage CMOS (MTCMOS). It effectively reduces Pst by disconnecting the power supply through the use of high Vt MOSFET switches. However, there are serious drawbacks with the use of this technique, such as the fact that both memories and flip-flops based on this technique cannot retain data. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) that reduces Pst by increasing the substrate-biases. This technique also faces some serious problems, such as a large area penalty and a large power penalty due to the substrate-bias supply circuits requires low leakage power.

A. Upper SVL circuit

In the above figure shows Upper SVL circuit. The impedance of a MOS transistor increases with the width of the transistor.PMOS1 in the above circuit having width means it offers very high resistance in that path between Vdd and Vd. So that leakage in this SVL mode is very less. And also NMOS1\ and NMOS2 forms a working in normal mode of the cell.NMOS2 acts as a resister to reduce current in active mode. By connecting above way the leakage is further reduced.

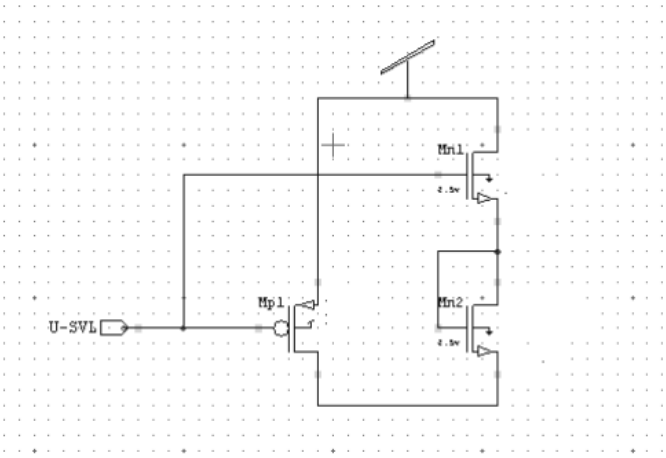

Figure 6: Upper SVL circuit

B. Lower SVL circuit

Below circuit represents lower SVL circuit. NMOS3 transistor work in the SVL mode and PMOS2 and PMOS3 transistor work in the normal mode of the cell. PMOS2 acts as a resistor to reduce leakage. These two techniques reduce leakage current compared to the previous SVL.

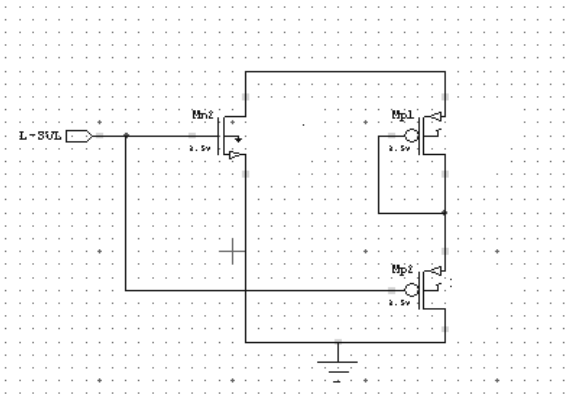

Figure 7: Lower SVL Circuit

Table 1. Sram Cell Svl Operation

MODE	Upper SVL Circuit	Lower SVL Circuit
Active	PMOS switch is turned on	NMOS switch is turned on
	VDD is supplied	VSS is supplied
Stand-by Mode	NMOS Switch is turned on	PMOS switch is turned on
	VD(<VDD) is supplied	S(>VSS) is supplied

The above circuits work with normal SVL circuits. The circuit consists of normal SRAM cell Using Stacking Technique and upper SVL circuit and lower SVL circuits and operation of the circuit explained with the table below.

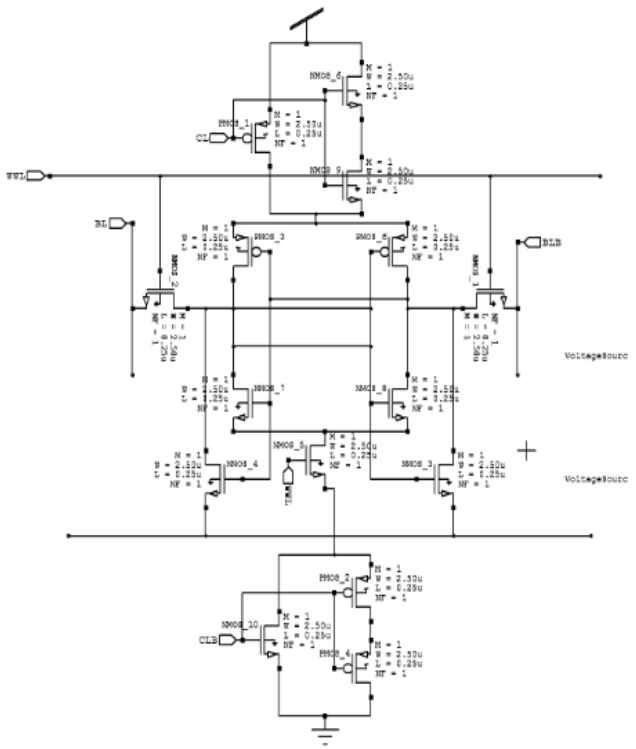

Figure 8: SVL Based 8T low Power SRAM

SIMULATION RESULTS

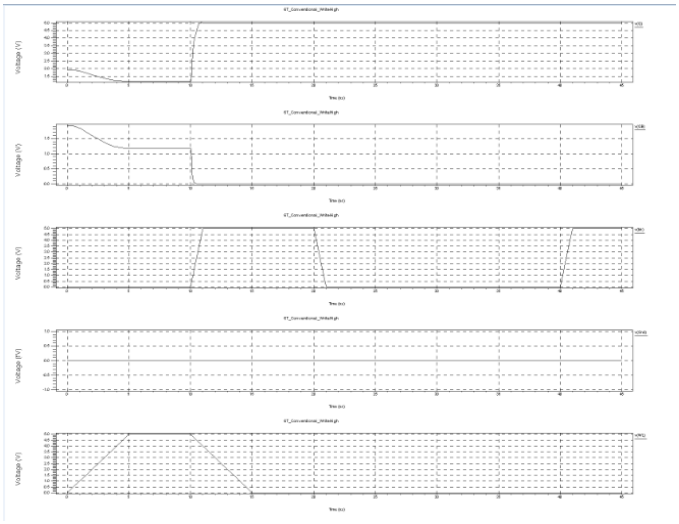

Figure 9: Simulation Result of SRAM

Table 2. SRAM Power Calculations

Circuit	Power Value
6T SRAM	1.038927e-002 watts
Low Power 8T SRAM (LP8T)	1.426784e-009 watts
Low Power 8T SVL	1.167866e-009 watts

IV. CONCLUSION

SVL circuit will play a major role in future. The effect of the SVL circuit on the leakage current through the load circuit (i.e., reduction in current) was examined. The SVL circuit and the load circuit were designed using technology. Sub-threshold memory design has received a lot of attention in the past years, but most of them use large number of transistor to achieve sub threshold region operation. The new technique inherently process variation tolerant, this makes the new approach attractive for Nano computing in which process variations is a major design constraint. In this circuit we have several advantages in different modes that is in operating mode high Vds to load circuits for high speed operation, in stand-by mode high Vt through - On MOS switches to load circuits for minimum stand-by leakage power, data retention, high noise immunity, small stand-by power dissipation, negligible speed degradation, negligible area overhead, high noise immunity, data retentions at stand-by mode. In this circuit the standby leakage power is reduced by which total average power also reduced and delays in SRAM Cell.

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