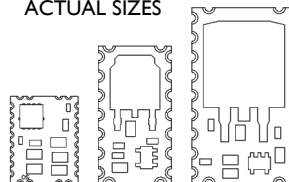# 300P-N-C Series
CMOS Power Switch
SMT, High Speed, High Voltage

ACTUAL SIZES

XSYSTOR

PRODUCT FLYER
August 2015

General Description

The 300PNC Series Complementary MOSFET Switches offers ease of integration to the GaN amplifier. They have clocked speeds of <<200nsec for Rise and Fall Times. With board space at a premium, its compact footprint allows direct placement on or near the RF Choke to the supply line. The current capacity of the switches are up to 40A average CW with good heat sinking, and are safe with momentary peak surges of current reaching >3X the average. The SMT switch is ideally driven by the 100 or 200 Series Controllers with direct connection to its GATE input port.
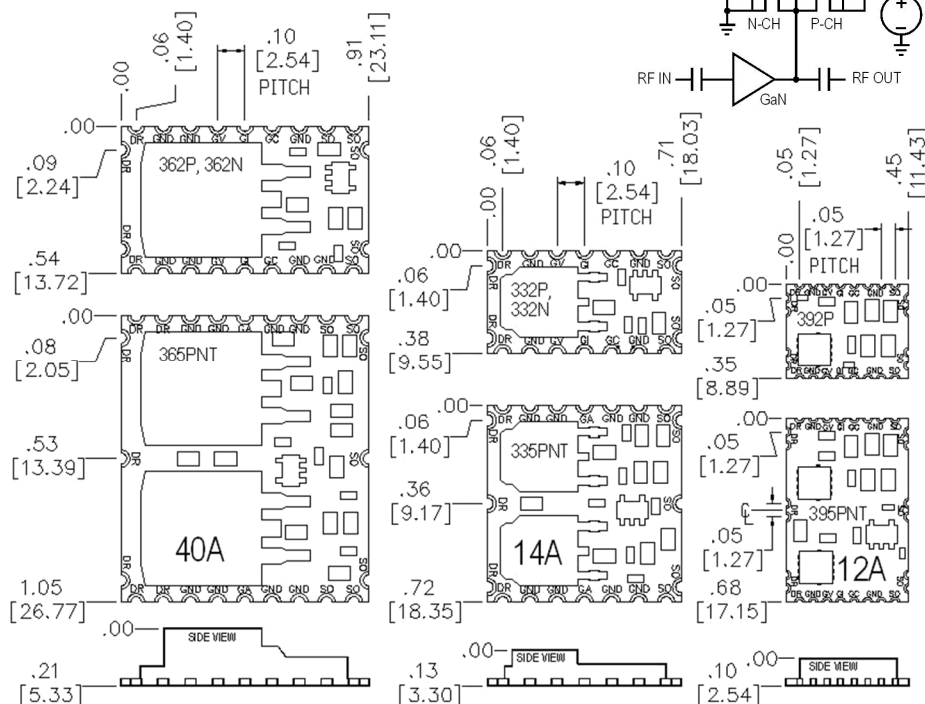
Features

- Rated for 100V
- Ultra-low Rds ON
- Operation up to 175°C, with derated voltage and current.
- Great for High-Speed Pulsed systems.
- Total switching times of <500 nsec when used together with 100 or 200 Series Controllers.
- Complementary P & N-channel MOS achieve Rise & Fall Times of <<200ns.
- Available in tape & reel.
- RoHS* Compliant

Specification Snapshot

Parameter	Min	Max
Source Voltage	+28 V	+80 V
Gate Voltage	0 V	+20 V
Drain Voltage	+28 V	+80 V
Rds ON (14 A Switch)		0.22 Ω
Rds ON (40 A Switch)		0.07 Ω
Turn-ON Propagation Delay		100 ns
Turn-ON Rise Time		70 ns
Turn-OFF Propagation Delay Complementary Pair Only		150 ns
Turn-OFF Fall Time		100 ns
Period for Pulsed Signals		5 ms
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of Drive Signal from Controller to 10% of Drain Voltage Output with load of 1KΩ. Faster speeds occur with decreased load resistance. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Typical Connection Diagram

FLEX-100 OR 200 SERIES CONTROLLER

10 11 12 13
GND DFB DRV VDS

N-CH   P-CH

RF IN —— GaN —— RF OUT

362P, 362N
.06 [1.40]
.10 [2.54] PITCH
.91 [23.11]
.09 [2.24]
.54 [13.72]

365PNT
.08 [2.05]
.53 [13.39]
1.05 [26.77]
40A

332P, 332N
.06 [1.40]
.10 [2.54] PITCH
.71 [18.03]
.38 [9.55]

335PNT
.06 [1.40]
.36 [9.17]
.72 [18.35]
14A

392P
.05 [1.27] PITCH
.45 [11.43]
.05 [1.27]
.35 [8.89]

395PNT
.05 [1.27]
.05 [1.27]
.68 [17.15]
12A

SIDE VIEW
.21 [5.33]
SIDE VIEW
.13 [3.30]
SIDE VIEW
.10 [2.54]

Ordering Information

332P0000	14 AMP PULSED SWITCH
332N0000	COMPLEMENTS 332P ONLY
335CT000	14 AMP PULSED SWITCH, POWER CMOS, TTL DRIVE
362P0000	40 AMP PULSED SWITCH.
362N0000	COMPLEMENTS 362P ONLY
365CT000	40 AMP PULSED SWITCH, POWER CMOS, TTL DRIVE
392P0000	12 AMP PULSED mini SWITCH
395CT000	12 AMP PULSED mini SWITCH POWER CMOS, TTL DRIVE

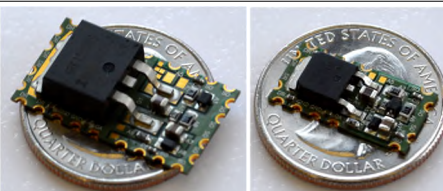P = P-CHANNEL MOSFET. STAND ALONE

N = N-CHANNEL MOSFET. NON STAND ALONE

C = COMPLEMENTARY P & N MOSFET
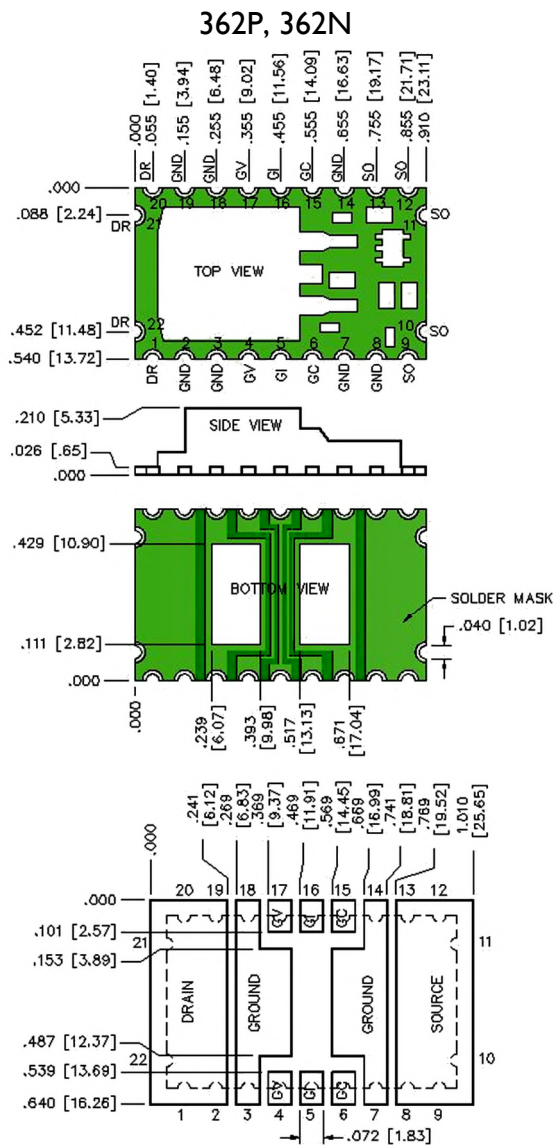
T = TTL INPUT DRIVE ONLY!

XSYSTOR INC.
18000 STUDEBAKER RD SUITE 700 MS 723
CERRITOS CA 90703
TEL: 888-968-7755   FAX: 888-968-7755
EMAIL: SALES@XSYSTOR.COM

Outline & Land Pattern_40A

362P, 362N

365CT

Switch I/O Pin Descriptions

GA is a gate input that receive signals from OTL or DRV outputs of Controller. Care should be taken from these respective TTL or Open Drain signals to prevent damage.

GI is a gate input connected to DRV of Controller. These ports are interconnected for P & N-Chan Pairs. For a Single Switch module GI is tied to GC.

GC is interconnected to like ports for P & N-Chan Pairs. It is only tied to GI for a Single Switch configuration.
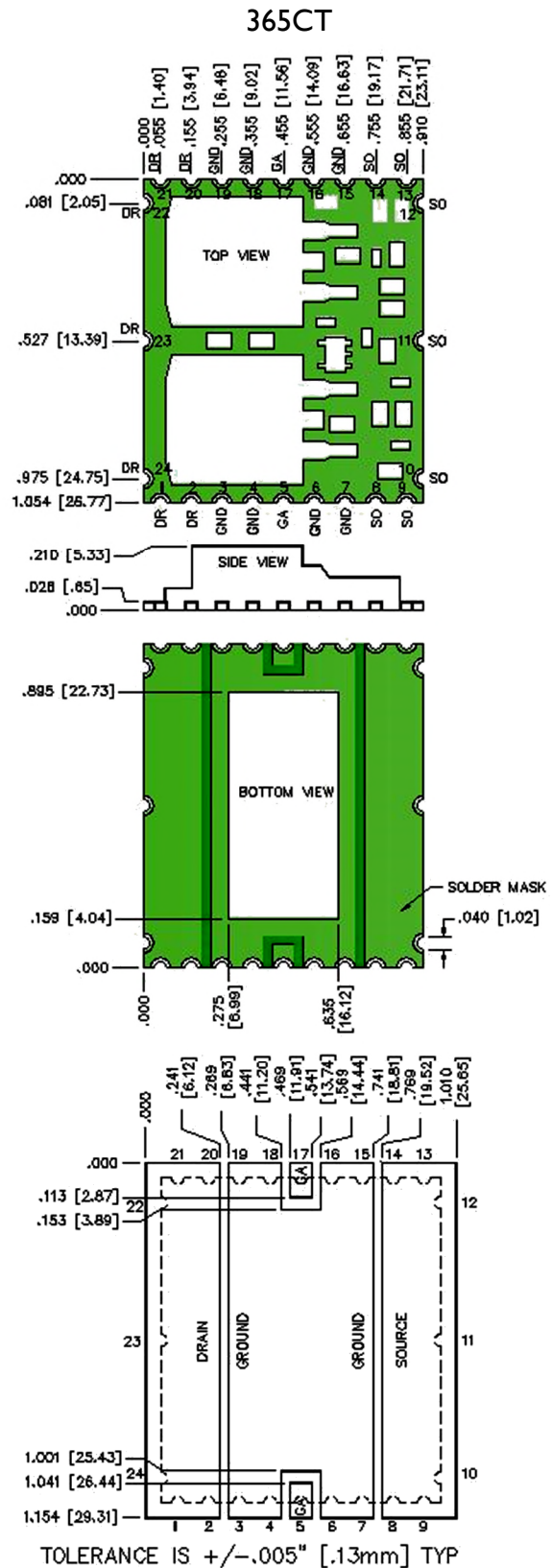
GV is interconnected to like ports for P & N-Chan Pairs. Otherwise, leave port open for a Single Switch configuration.

DR are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.

SO are source inputs that take up to +80V supply. Larger storage capacitance are attached here.

Typical Timing Diagrams

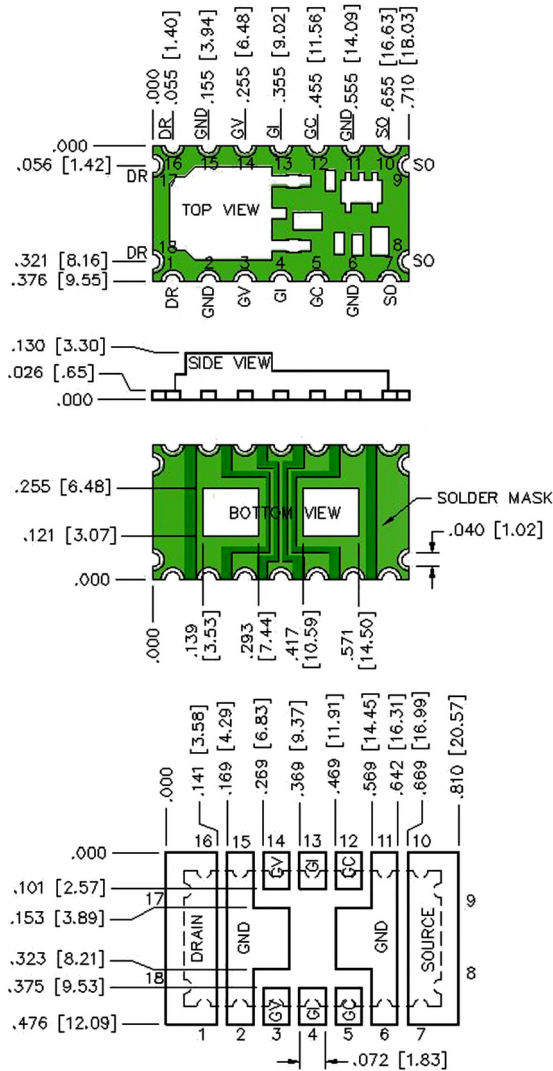Refer to Application Note XAN-2 for further details.

Model Number Color Code

0	1	2	3	4	5	6	7	8	9
■	■	■	■	■	■	■	■	■	□

Outline & Land Pattern_14A

332P, 332N

335CT

TOLERANCE IS +/−.005" [.13mm] TYP

Switch I/O Pin Descriptions

GA is a gate input that receive signals from OTL or DRV outputs of Controller. Care should be taken from these respective TTL or Open Drain signals to prevent damage.

GI is a gate input connected to DRV of Controller. These ports are interconnected for P & N-Chan Pairs. For a Single Switch module GI is tied to GC.

GC is interconnected to like ports for P & N-Chan Pairs. It is only tied to GI for a Single Switch configuration.

GV is interconnected to like ports for P & N-Chan Pairs. Otherwise, leave port open for a Single Switch configuration.
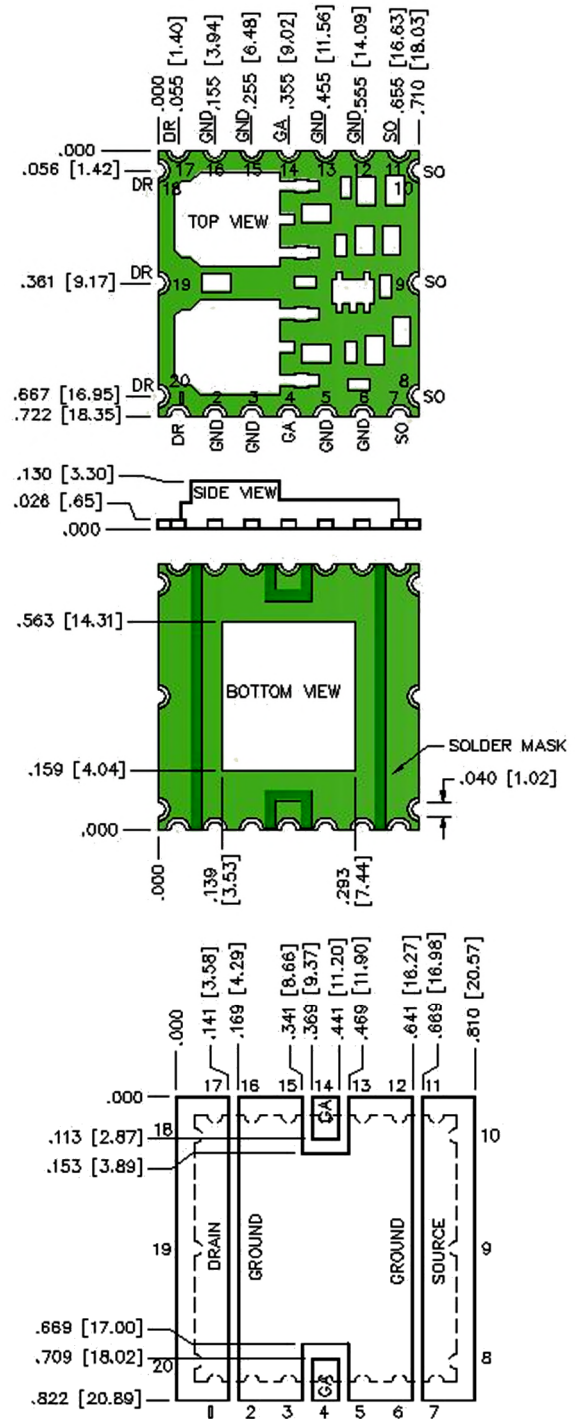
DR are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.

SO are source inputs that take up to +80V supply. Larger storage capacitance are attached here.

Typical Timing Diagrams
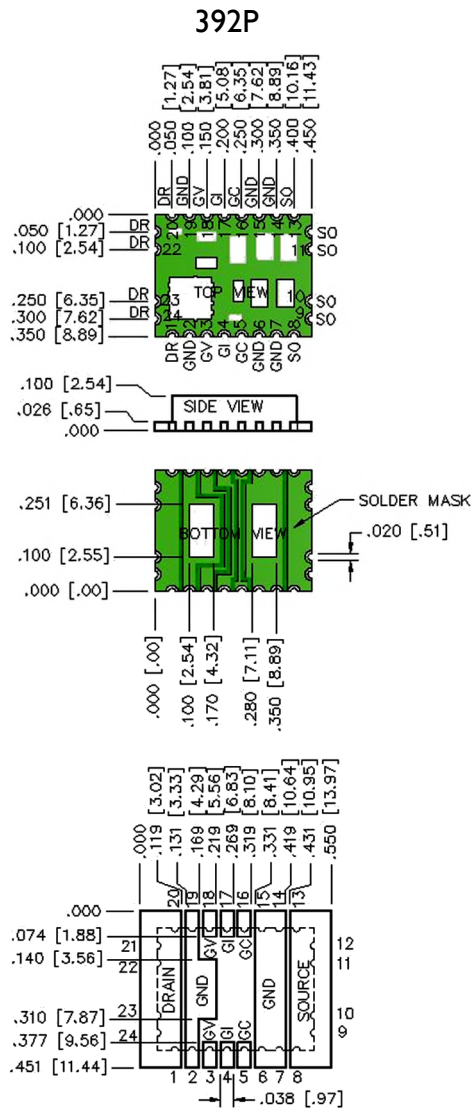
Refer to Application Note XAN-2 for further details.

Model Number Color Code

0	1	2	3	4	5	6	7	8	9

Outline & Land Pattern_12A

392P

395CT

TOLERANCE IS +/−.005" [.13mm] TYP

Switch I/O Pin Descriptions

GA is a gate input that receive signals from OTL or DRV outputs of Controller. Care should be taken from these respective TTL or Open Drain signals to prevent damage.

GI is a gate input connected to DRV of Controller. These ports are interconnected for P & N-Chan Pairs. For a Single Switch module GI is tied to GC.

GC is interconnected to like ports for P & N-Chan Pairs. It is only tied to GI for a Single Switch configuration.
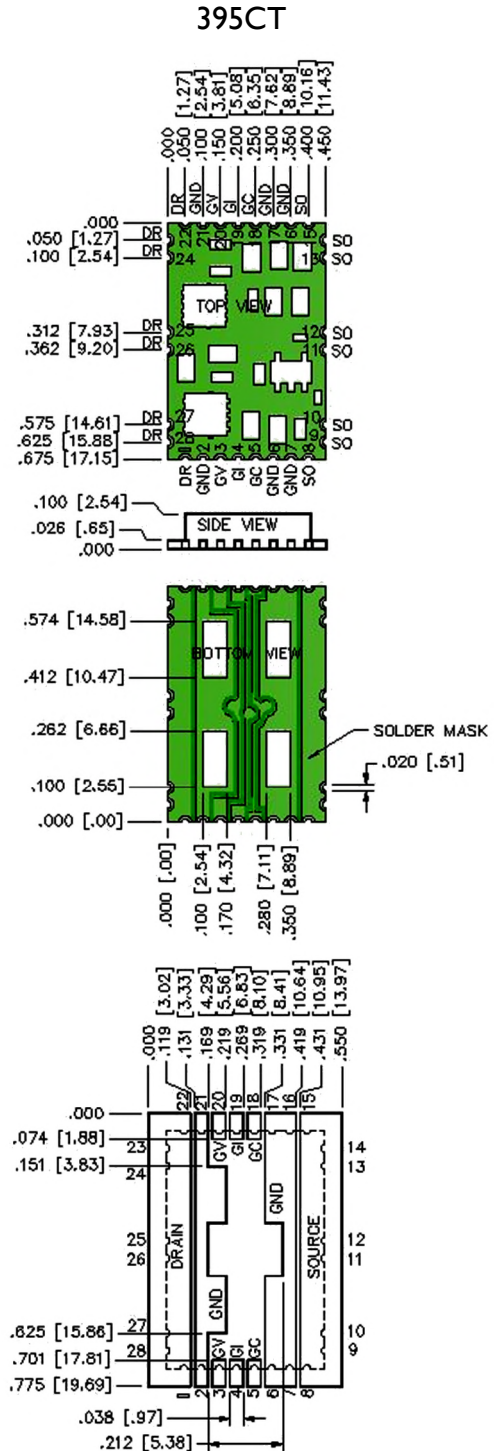
GV is interconnected to like ports for P & N-Chan Pairs. Otherwise, leave port open for a Single Switch configuration.

DR are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.

SO are source inputs that take up to +80V supply. Larger storage capacitance are attached here.

Typical Timing Diagrams

Refer to Application Note XAN-2 for further details.

Model Number Color Code

0	1	2	3	4	5	6	7	8	9

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