Design and Simulation of a Novel Dynamic Comparator for High Noise Immunity, High Speed and Low Power Applications

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Abstract - The paper here proposed a dynamic comparator design using CMOS (Complementary metal-oxide-semiconductor) logic is used. Being one of the most essential part of ADC design, comparator needs to be performing under high performance with low power consumption and high speed. The design was simulated using Tanner EDA tool in 180nm technology. Performance parameters such as power, delay and PDP (Power Delay Parameter) are compared with the exiting designs. For 1.2-V supply at 180nnm technology, the average power consumption was found to be extremely low (620.3nW). Delay of dynamic and double tail dynamic comparator are (940ps) or (346ps)and PDP is (214.7a) and energy is (49.63f). In comparison with the exiting dynamic comparator designs, the present implementation was found to offer significant improvement in term of power and speed.

Keywords: Dynamic comparator, dynamic clocked comparator, power gating, high-speed analog-to-digital converters (ADCs).

I. INTRODUCTION

Comparator is one of the fundamental building block in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area.

Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed.Many techniques, such as supply boosting methods, techniques employing body-driven transistors, current-mode design and those using dual oxide processes, which can handle higher supply voltages. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the dynamic comparatorstructure, a new double-taildynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors.

II. CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR

The schematic diagram of the conventional dynamic comparator. It is widely used in A/D converters, with high inputimpedance, rail-to-rail output swing, and no static power consumption. In this operation of the comparator. During the reset phase when CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Out*n*and Out*p*to *V*DD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = *V*DD, transistors *M*7 and *M*8are off, and *M*tail is on. Output voltages (Out*p*, Out*n*), which had been pre-charged to *V*DD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where *V*INP > *V*INN, Out*p*discharges faster than Out*n*, hence when Out*p*(discharged by transistor *M*2 drain current), falls down to *V*DD–|*V*thp|before Out*n*(discharged by transistor *M*1 drain current), the corresponding pMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus, Out*n*pulls to *V*DD and Out*p*discharges to ground. If *V*INP < *V*INN, the circuits works vice versa.

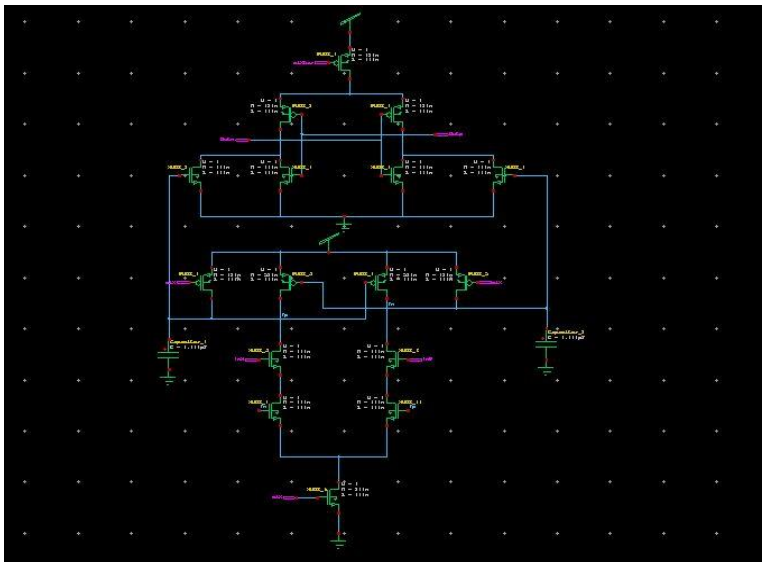

Fig. 1 Schematic diagram of the conventional dynamic comparator

Base double tail comparator uses cross coupled PMOS to speed up the latch operationwhile addition of two NMOS transistorwith input fn and fp use forpower reduction as it gives direct discharge path to our circuit.

III. MODIFIED DOUBLE TAIL DYNAMIC COMPARATOR

The double tail comparator architecture is used in low voltage applications because of its better performance in delay reduction.

Operation:

The schematic diagram of double tail comparator. The operation of the double tail comparator occurs in two phase which are reset phase and decision making phase. During reset phase CLK=0, Mtail1 and Mtail2 are in off state, M3 and M4 are in on state which pulls both the nodes fn and fp to VDD. so according to the input suppose Vinp>Vinn, then fn drops faster than fp. As long as fn continues falling, the corresponding PMOS control transistor starts to turn on, pulling fp node back to VDD. So another control transistor (Mc2) remains off, allowing fn to be discharged completely. The control transistor Mc1 is on when Mc2 is grounded which results in static power consumption so two more switches (Msw1 and Msw2) are added.

During the decision making phase the nodes fn and fp are pre charged to VDD and it starts its different discharging. As soon as the comparator detects that one of the fn/fp is discharging faster, control transistor will help to increase the voltage difference.

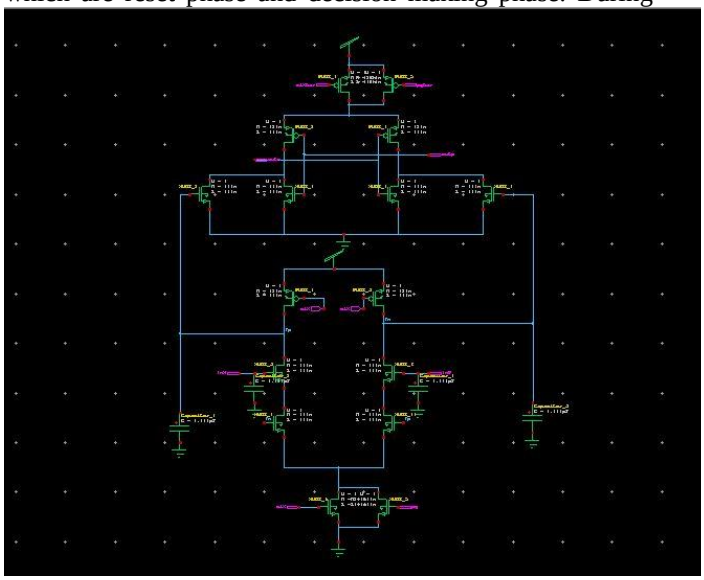

Fig.2 Schematic diagram of Modified dynamic comparator

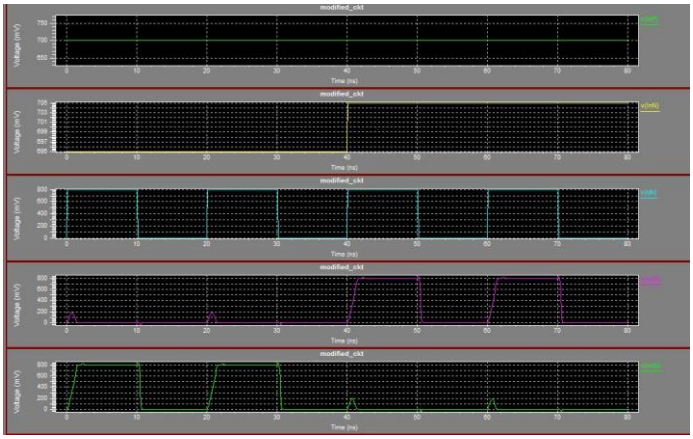

Fig.3 The output waveform of Modified dynamic comparator

Table 1 : Comparison Table

PARAMETERS	BASED PAPER DOUBLE -TAIL COMPERATOR	MODIFIED DOUBLE-TAIL COMPARATOR	Percentage Improvement
TECHNOLOGY	180nm	180nm	
APPLIED VOLTAGE	0.8v	0.8v	
POWER(nw)	904.58	761.48	15.81 %
DELAY(outp)(ns)	1.1577	0.8811	23.89 %
DELAY(outn) (ns)	1.1280	0.8749	22.43 %
PDP(outp) (fJ)	1.0472	0.6709	35.93 %
PDP (outpn) (fJ)	1.204	0.6662	44.66 %
ENERGY(fJ)	72.36	60.91	15.82 %

IV. RESULTS

To analyse the performance of the structures we have simulated the circuits at 180nm technology and output is been observed which is presented in tabular format below. The power consumption, delay, PDP and energy of dynamic comparator and double tail dynamic comparator are obtained and compared with both the designs.

V. CONCLUSION

Both the design methodologies have been compared and it is evident that there is performance improvement in the proposed circuit. Double tail technique is an effective way to reduce power consumption and delay. All the designs have been simulated at Tanner EDA 14.1 version.

VI. REFERENCES

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