An Article on Design Simulation of Latch Sense Amplifier in Low Power Operation for SRAM Application

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Abstract- A sense amplifier (SA) circuit that operates at low power and consumes less power in SRAM applications is proposed in this paper. The improvement in delay also describesby scaling down the size of transistor. We describe CMOS latch type voltage sense amplifier andusing MICROWIND&DSCH software we analyze its layout simulation result. According to analysis and simulation result we propose an advanced sense amplifier design that can able to increase power efficiency and boost the speed of SRAM.
Simulation of the operation of sense amplifier should be with non-ideal sources (with finite source resistance) to determine the significance of clock feed-through and kickback noise[1]. Large kickback noise interferes with sensing. To minimize power we erase DC paths from VDD to ground except during switching times.

Keywords- Sense amplifier, simulation, MICROWIND & DSCH, low power.

I. INTRODUCTION

Improvement in CMOS technology is continues to reduce power consumption and to reduce delay to be driven by the required to integrate more function in a small silicon area.
In 2010-2013 Deep Nano scale technologies [2] includes 32nm and 22nm processes appear to improve power, size, speed and increased integration of CMOS circuits we must scale down CMOS technologies.In the next four to eight years IC industry play the role of the key supportingindustries, and thelow power design for good performance of CMOS circuits will playimportant role.At present, high speed andlow power SRAM becomes one of the hot spot in the research area in the field ofdigital integrated circuit [3].
The voltage movement on the bit line, may be very small, e.g., 50 mV or less, and so determining if the voltage is moving upwards or downwards can be challenging. In addition, we would like our sense amplifier to drive the bit line to full, valid, logic levels [4].
In read/write operation of SRAM .In the read cycle, word-line WL is activated high to select row of the memory array. Thevoltage at BL is discharged across the capacitorand load transistorand current flow through the bit-line load transistors, accessed transistors, and driver transistors. Due to consuming more current by these transistors the operating power increases and accessspeed of the memory decreases.
To improve speed performance, and reduce power dissipation, we can use the Address Transition Detection (ATD) technique.
Although, the loss of DC current from drain voltage (VDD) through bit-line load transistorsstill occursby the pulsed word-line signal which causesmemory cells assertion.
Current in memory cells affectsby channel conductance of the transistor in a memory array. Low voltage supply decrease speed performance of SRAM significantly, by increasing the channel width or by amplifying voltage of bit-line we can increase the channel conductance. Amplifying voltage of word-line and bit-line is highly effective in low power operation [1].
In the SRAM Sense amplifier is the peripheral circuits that is used to improve speed and performance of the SRAM. Sense amplifier is also minimize, the power consumption of SRAM.Sense amplifier is used to amplifying the low voltage signals at bit line by sensing low voltage or current for fast data access.Although, delay in charging and discharging of capacitive load is large so the design of low power and fast sense amplifier has become themajor part in designing of high speed SRAM [3].

II. VOLTAGE LATCH TYPE SENSE AMPLIFIER

The voltage latch sense amplifier is shown in Fig.1:

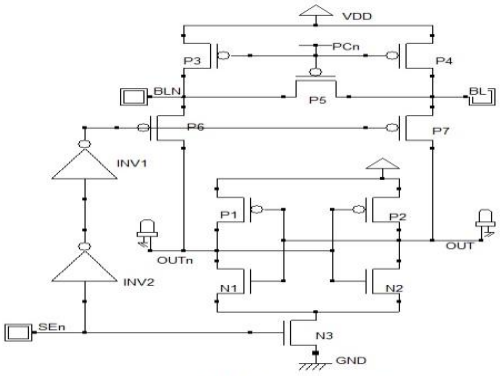

fig.1 Latch type Sense Amplifier

In this fig.1 transistorsP1, P2, N1 and N2 creating the main body of sense amplifier. Transistor N3 is used to control state of sense amplifier that are turn on/off by sense enable (SEn) signal. BL and BLN are the input/output of SRAM. When we write BL and BLN act as input and when we read from memory BL and BLN act as output of SRAM. Transistor P3 and P4 conclude in pre-charge circuit, BL and BLN pre-charge to VDD through P3 and P4. The transistor P5 works as balancing transistor that balances the initial voltage of two bit-lines. Initial voltage of bit-lines should be same this prevent bad turning of sense amplifier during signal amplification. The voltage difference between BL and BLN is transferred to sense amplifier by switching through transistor P6 and P7 that act as switch. The switching of transistor P6 and P7 is driven by thesignalSEn, this is also use to enable sense amplifier [5].
When PCn signal is pulling down, bit-lines are charged to VDD and transistor P5 maintain the voltage difference of bit-lines that occurs due to variation in device threshold. After that transistors P3, P4 and P5 are turn off and word line is activated to read the contents of memory. Now voltage at one of the bit-line pulled down for example WL=1, and content in memory is Q=1, QN =0 then voltage at BLN decreases this leads to output high. And if Q=0, and QN=1 then voltage at BL goes down this leads to output low. When voltage difference is high enough then transistor N3 turned ON as SEnsignal goes to high and sense amplifier is activated and amplify bit-line voltage quickly.

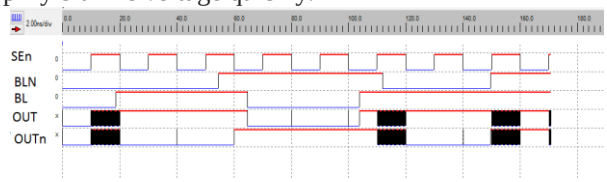

Fig.1.1 Timing Diagram of fig. 1

In sense amplifier that shown in fig.1 the voltage difference occurs at output due to change in device threshold of the transistor P6 and P7 so the output should be balance,for this we can adjust a balanced transistor between OUT and OUTn node.
The inverters are used in designing of sense amplifier so we should also design efficientinverter that minimizes the delay and power consumption.

III. REMOVING SENSE AMPLIFIER MEMORY

Fig.2 shows how the sense amplifier's memory can be erased. MOSFETs N4 and N5 are used to remove the sense amplifier's memory, all nodes must be actively driven to a known voltage (no floating or dynamically charged nodes).In sense amplifier the transistors N4 and N5 are off state, that breaking the connection between ground and VDD (so no current flows in the latch). The gates terminals of N1 and N2 are at VDD so their drain terminals are driven to ground. In other words, all nodes in the circuit are either pulled high to VDD or low to ground, when clock is low.

The timing diagram of removing sense amplifier memory is shown in fig.2.1:

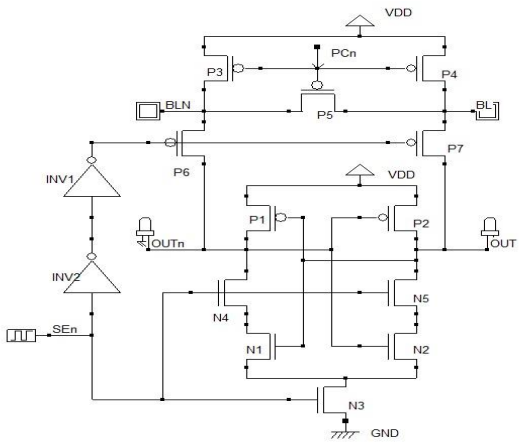

Fig.2 Latch type sense amplifier with removing memory

This circuit is designed in DSCH software [6] and simulation output waveform is obtained.

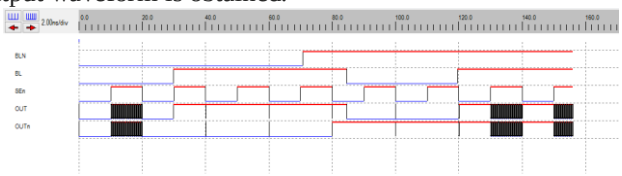

Fig.2.1 Timing Diagram of fig.2

IV. CONCLUSION

The performance of VLSI circuits is limited by signal delay, kickback noise and power used by CMOS chip. One of the methods to reduce power used by chip is low power operation. The low power operation affected by large kickback noise that interfacing with sensing in voltage sense amplifier. Proposed SA operates quite well at supply voltages from 1.2-1.0 V. It is good for wide range of Small-swing circuits. Applying such circuits in VLSI design allows reducing the power used by chip and improving the performance. Also by removing sense amplifier memory we can improve the performance.

V. REFERENCES

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