PVT Variations and Process Corners for a Low Leakage Power 7T SRAM cell

G.Surekha[1], Dr.N.Balaji[2], Dr.Y.Padma Sai[3]
[1]*GRIET,Hyderabad*
[2]*JNTUK,Kakinada*
[3]*VNRVJIET,Hyderabad*
(E-mail: yandamurisurekha@gmail.com)

Abstract— Low Power devices under subthreshold regions are being utilized widely in low energy applications. This research paper analyzes the variations of Power, Voltage and temperature for a 7T SRAM cell. Also an effort is made to analyze the process corners. This 7T SRAM cell reduces the static power as standard 6T SRAM cell consumes more static power in deep submicron process. The design is implemented using both 90nm and 180nm Technologies. The proposed 7T SRAM cell proved to be more efficient with reduced static power dissipations for Power, Voltage and Temperature (PVT) variations.

Keywords—*SRAM, static power,leakage power, sub threshold region, process corners.*

I. INTRODUCTION

A memory cell is the most important unit of any computing system [1]. The only picture we normally imagine when we hear the word memory is an allocated digital space which enables us to store data in the form of binary 0's and 1's. But for the system, it needs certain hardware to be allocated so as to maintain the so called "memory". The most basic memory unit that enables storing of data is the Static RAM cell [2]. The data (binary) is stored in a loop of inverters that are connected to each other. The voltage is looped between the two inverters which allow it to be retained for a proper amount of time [3]. But due to some other complications it was observed that lot of power was used to run the Processor unit as the SRAM cell is the main cell used for memory purpose. Then an attempt is made to reduce the power consumption of a memory cell for both ON and OFF conditions.

Reduction in power usage and power consumption to implement a standard memory cell is 6 Transistor Static Random Access Memory (6T SRAM) cell has been taking a tremendous change over the past three decades. Yet there always seems to be a scope for development so as to reduce the power consumed by the SRAM by a considerable factor [4]. The major area of concern for almost all the VLSI designers is to invoke and implement such a process where the power used or consumed by the 6T SRAM be lowered to the highest possible extent[5].

Many designers introduced the concept of using more transistors to implement the SRAM cell for its working [6]. For a standard 6T SRAM cell another nMOS transistor is added to reduce the power consumed and obtaining performance based SNM [7]. The paper is organized as follows section II describes the proposed method, section III discusses experimental results and section IV gives conclusion.

II. PROPOSED METHOD

Standard 6T SRAM Cell will not work properly at low voltages because of the division of voltage between access and pull down transistors [8]. To improve read and write performances in 6T cell so many methods are investigated [9]. But all these techniques are failed to use the 6T SRAM cell in lower voltages. Fig.1. shows the Standard 6T SRAM cell.

Proposed 7T SRAM Cell is shown in Fig.2. Extra NMOS (N_5) transistor is connected between V_{DD} and two cross coupled inverters. Whenever word line (WL) goes high NMOS (N_5) is in ON condition and the V_{DD} supplied to two cross coupled inverters is reduced to V_{DD} - V_{th} which not only reduces leakage power and also reduces dynamic power hence low power requirement is achieved using this proposed technique.

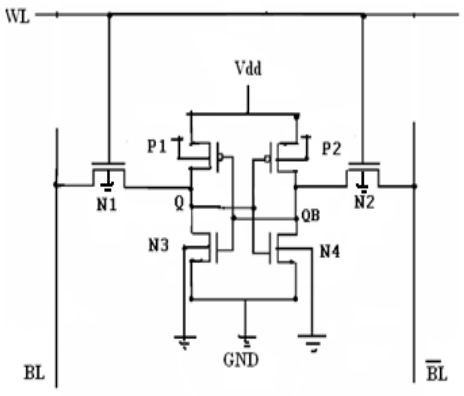

Fig.1. Standard 6T SRAM Cell.

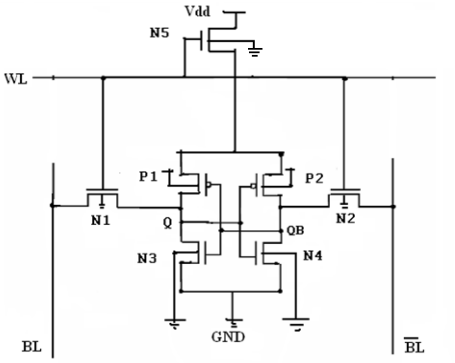

Fig.2. Proposed 7T SRAM Cell.

When data need to be read or write then only WL is high so that extra NMOS (N_5) transistor is ON condition hence reducing leakage power for total circuit when it is in idle condition.

Total power consumption of the circuit is the sum of dynamic, static and short circuit power is given by in equation (1).

$$P = P_{dynamic} + P_{static} + P_{sc} \ldots\ldots\ldots\ldots (1)$$

$$P = \alpha_{0\to1} C_L V_{dd}^2 f_{clk} + V_{dd}\left(I_{SC} + I_{Leakage} + I_{Static}\right) \ldots\ldots (2)$$

Dynamic power and static power is given by in equation (2) where α is activity factor and activity will performed between 0 and 1, $C_L, V_{dd}^2 and f_{clk}$ are the load capacitance, applied voltage and clock frequencies respectively. I_{SC} is short circuit current, $I_{Leakage}$ is the leakage current flowing through the circuit when it is in OFF condition and I_{Static} is the current flowing through the ON transistor. As the dynamic power and static power of the circuit is reduced using the proposed technique hence the overall power consumption of the circuit reduced greatly.

III. EXPERIMENTAL RESULTS

Comparison of Power consumption in all Process Corners for Proposed 7T SRAM cell with standard 6T SRAM cell is shown in Table.1.

TABLE.1.
Comparison Of Power Consumption for all Process Corners Of 6T SRAM Cell And 7T SRAM Cell at 27°C Temperature

Corners	6T SRAM	7T SRAM
NN	52.18 nW	30.09nW
FF	79.22 nW	50.0 nW
SS	34.73 nW	18.29 nW
SF	34.90 nW	19.03 nW
FS	74.70 nW	48.91 nW

The process corners are NN, FF, SS, SF and FS. Analyzing the proposed circuit in all process corners shows performance of the circuit. Process corner NN indicates NMOS and PMOS transistors are in normal mode operation, FF indicates NMOS and PMOS transistors are in fast mode operation, SS indicates NMOS and PMOS transistors are in slow mode operation. SF indicates NMOS slow, PMOS fast and FS indicates NMOS fast and PMOS slow. Comparison of Power consumption in all Process Corners for Proposed 7T SRAM cell with standard 6T SRAM cell at 27° is shown in Fig.3. These results are obtained at typical process corners and at room temperature. The left most bar graph shows the power dissipation of 6T and 7T at normal room temperature.

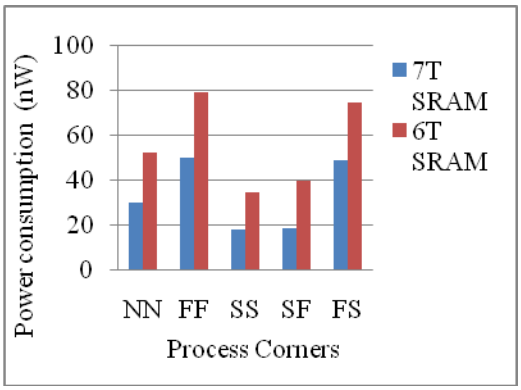

Fig.3. Comparison of Process Corners for Proposed 7T SRAM cell with standard 6T SRAM cell at 27°C.

Comparison of all Process Corners for Proposed 7T SRAM cell at different temperatures is shown in Table.2.

TABLE.2.
Comparison of all Process Corners for proposed 7T SRAM Cell at different temperatures

T / PC	27°C	30°C	33°C	36°C	40°C
SS	18.2 nW	18.78 nW	19.29 nW	19.81 nW	20.51 nW
SF	19.03 nW	19.54 nW	20.06 nW	20.60 nW	21.33 nW
NN	30.09n W	31.04 nW	32.01 nW	33.01 nW	34.34 nW
FS	48.91 nW	50.51 nW	52.12 nW	53.73 nW	55.98 nW
FF	50 nW	51.62 nW	53.27 nW	54.94 nW	57.22 nW

Comparison of all Process Corners for Proposed 7T SRAM cell at different temperatures is shown in Fig.4. A Change in temperature affect power. In Fig.4 for all the process corners and different temperatures the proposed 7T SRAM cell is analyzed.

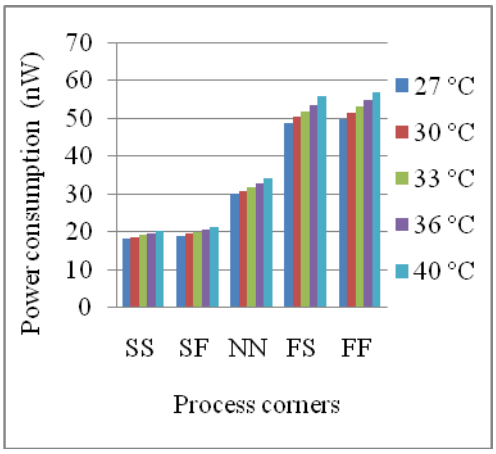

Fig.4. Comparison of all Process Corners for proposed 7T SRAM Cell at different temperatures

Power Consumption of 7T SRAM cell at different temperatures and different voltages is shown in Table 3.

TABLE.3
Power Consumption of 7TSRAM Cell at different Voltages and different Temperatures

T \ V	800mV	1V	1.2V
27°C	12.89 nW	30.09 nW	62.34 nW
30°C	13.29 nW	31.04 nW	64.13 nW
33°C	13.69 nW	32.01 nW	65.94 nW
36°C	14.10 nW	33.00 nW	67.78 nW

Power Consumption of 7T SRAM cell at different temperatures and different voltages is shown in Fig.5.

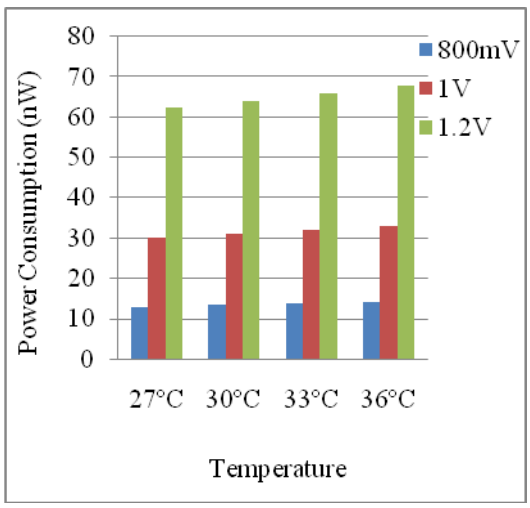

Fig.5. Power consumption of 7T SRAM cell at different temperatures and different voltages.

Comparison of total Power Consumption for 6T SRAM cell and 7T SRAM cell for different technologies is shown in Table.4.

TABLE.4
Comparison of total Power Consumption for 6T SRAM Cell and 7T SRAM Cell for different technologies

Technology(nm)	6T SRAM Power	7T SRAM Power
90	3.18nW	0.29 nW
180	2.887µW	0.3 µW

Comparison of total Power Consumption for 6T SRAM cell and 7T SRAM cell for different technologies is shown in Fig.6.

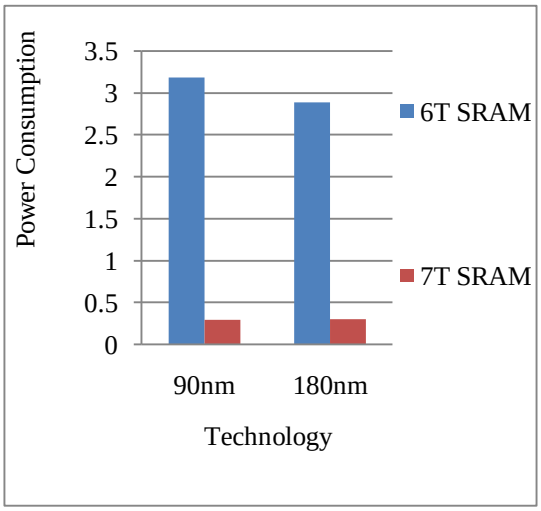

Fig.6. Comparison of total Power consumption for 6T SRAM cell with Proposed 7T SRAM cell for different technologies.

Leakage Power Comparison of 6T SRAM cell and 7T SRAM cell at different technologies is shown in Table.5.

TABLE.5
Leakage Power Comparison of 6T SRAM Cell and 7TSRAM Cell for different technologies

Technology(nm)	6T SRAM Power(nW)	7T SRAM Power(nW)
90	0.653	0.0033
180	0.873	0.00833

Leakage Power Comparison of 6T SRAM cell and 7T SRAM cell at different technologies is shown in Fig.7.

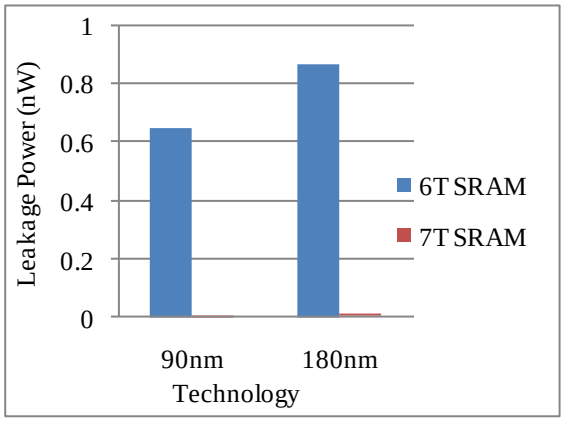

Fig.7. Leakage power Comparison of 6T SRAM cell with Proposed 7T SRAM cell at different technologies.

IV. CONCLUSION

An efficient 7T SRAM cell is proposed and implemented using both 90nm and 180nm Technologies. Also 7T SRAM cell is analyzed for different power, voltage and temperature variations. It is observed that 7T SRAM cell is consuming leakage power of only 0.0033 nW in 90nm technology and 0.00833 nW in 180nm technology when compared to 0.653nW of leakage power in 90nm technology and 0.873nW in 180nm technology for 6T SRAM cell. This proves that 7T SRAM cell is more efficient than 6T SRAM cell. Also it is observed that 7T SRAM cell consumes more area of 1.3μm^2 for each transistor than the 6T SRAM cell. Hence at the cost of the area increase a reduction of leakage power is achieved.

REFERENCES

[1]. N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley, 2011.

[2].Lin, Ming-Bo. (2011). Introduction to VLSI Systems: A Logic, Circuit, and System Perspective. CRC Press.

[3].J.M. Rabaey, Digital Integrated Circuits-Prentice-Hall, 1996.

[4].Kiat-Seng Yeo, Kaushik Roy-Low Voltage Low Power VLSI Subsysyems. Tata McGraw Hill,2009.

[5].M. C. Shiau, C. C. Yu, and K. T. Chen, "Single port SRAM having a lower power voltage in writing operation", TW pat. I426514 B, Feb. 11, 2014.

[6]. L. Chang et al., "An 8T-SRAM for variability tolerance and low-voltage operation in high-performance caches," IEEE J. Solid-State Circuits,
vol. 43, no. 4, pp. 956–963, Apr. 2008.

[7]."Stability Analysis of 7T-SRAM Cell" G. Surekha, Dr. N. Balaji, Dr. Y. Padma Sai 10th International Conference on Intelligent Systems and Control (ISCO 2016), IEEE Conference Publications,2016,pg no's 1-4.

[8]. S. Nalam and B. H. Calhoun, "5T SRAM With Asymmetric Sizing for Improved Read Stability," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2431-2442, Oct. 2011.

[9]. H.Pilo, J.Barwin, G.Braceras,etal.,An SRAM design in 65-nm and45-nm technology nodes featuring read and write assist circuits to expand operating voltage, Symposium on VLSICircuits, Digest of Technical Papers,2006, pp. 15–16.

First Author: Mrs.G.Surekha received the Bachelors degree in ECE from JNTU Hyderabad, India and did Masters degree in VLSI GRIET, Hyderabad. She is currently working as Associate Professor in the Department of Electronics and Communication Engineering in GRIET and doing Ph.D in JNTU Hyderabad,Telangana, India.

Second Author: Dr.N.Balaji received the Bachelors degree in ECE from Andhra university, Vishakhapatnam. He did masters degree and Ph.D in OU Hyderabad. Now he is currently working as Professor and Director, Admissions, Department of ECE, JNTUK, Kakinada, Andhra Pradesh, India.

Third Author: Dr.Y.Padma Sai received the Bachelors degree in ECE from Nagarjuna University, She did masters degree and Ph.D in OU Hyderabad. Now She is currently working as Professor, Head of the Department ECE in VNR Vignana Jyothi Institute Of Engineering And Technology. Hyderabad, Telangana, India.