Design of Power and Energy Efficient Approximate Multiplier in Xilinx

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Abstract- Multimedia and image processing applications, may tolerate errors in calculations but still generate meaningful and beneficial results. This work deals with a high speed approximate multiplier with TDM tree and carry prediction circuit. The modified multiplier utilizes an optimized TDM carry save tree which reduces the device utilization on FPGA as well as the combinational path delay and power consumption. The proposed design is analyzed using the simulation and implementation results on Xilinx Spartan 3E family.

Keywords- Approximate Carry Adder, Three Dimensional Reduction method, Approximate Multiplier

I. INTRODUCTION

Correct and exact models and calculations are not constantly suitable for capable use in media and picture preparing tasks. The model of rough computation depends on altogether unwinding completely correct and totally deterministic building squares while, structuring vitality productive frameworks. In computerized plans, whole number increase is one of the basic building squares, which profoundly influences the microchip and DSP execution. A quicker advanced circuit is acquired by actualizing a theoretical (forecast) approach. Theoretical advanced circuits depend on quicker task by utilizing a theoretical practical unit, which is a number juggling unit that utilizes an indicator for the convey motion, without really sitting tight for the convey proliferation. The theoretical unit predicts the convey of the at least one cells utilized in the advanced circuit without trusting that the real convey engendering will happen. This is like an indicator in the microchip. Here we have considered a theoretical multiplier which comprises of a prescient convey spare decrease tree utilizing three stages: fractional items recoding, halfway item dividing and speculative pressure. The theoretical tree use (m: 2) counters, and are quicker than customary blowers dependent on half adders and full adders. The tree is additionally contained a quick convey engender viper and a mistake correction circuit. Theoretical multipliers have higher speed contrasted with their ordinary partners.

II. PREVIOUS WORKS

in [10] Shows that inexact circuits have higher execution when contrasted with exact rationale circuits. Numerous inaccurate multipliers have been proposed in the writing [4] [6] [7] [13]. These plans utilize a truncated increase strategy. In [6], a vague exhibit multiplier is utilized, by disregarding chosen minimum critical bits in fractional items. An inaccurate multiplier with redress consistent has been proposed in [13]. A variable remedy steady vague multiplier is proposed in [4].This technique adjusts the revision term as indicated by segment n-k-1. On the off chance that fractional items in section n-k-1 are one, redress factor is expanded and, if every single halfway item in the above segment are zero, the remedy factor is diminished. In [7], an essential 2x2 multiplier square is recommended for developing bigger multiplier clusters. In every one of these plans the territory was observed to be high. In [11] another surmised multiplier with two estimated [4:2] blower has been proposed. This multiplier requires lesser zone when contrasted with multipliers utilizing truncation procedure anyway the blunder rate was observed to be high.

[12] Describes another estimated multiplier plan which uses forecast units for the convey flag and furthermore has lesser mistake rate when contrasted with [11]. SFUs (Speculative Functional Units) are expectation circuits that can be considered as discovery elements which are quicker than their non - theoretical partners, autonomously of the specific usage [8]. Thus inexact multipliers utilizing SFUs additionally mean to accomplish defer upgrades, in the meantime presenting less power and territory overheads. This multiplier uses Carry Save Adder (CSA) tree [14] for halfway item decrease, wherein the convey yields are proliferated instead of being safeguarded accordingly lessens the deferral. Prevalent CSA plans incorporate Wallace tree and Dadda multiplier. Wallace tree [1] [9] result in long and sporadic wires along the segments to interface with the CSA. The wire capacitance thus expands the postponement and vitality of the multiplier and the wires are hard to format. Dadda refined Wallace's technique by presenting a counter situation system that requires few quantities of counters in the decrease arrange yet at the expense of bigger Carry spread Adder (CPA) [2] [9]. The deferral from a contribution to a yield in a full snake isn't the equivalent. This deferral is subject to a specific progress (0-to-1, 1-to-0). Hence it is likewise conceivable to concoct

diverse acknowledge of a full snake wherein a particular flag way is favored concerning the others and has been planned so that a flag engendering of this way takes a negligible measure of time [3]. The CSA plot which deals with this postponement experiencing significant change is Three Dimensional Scheme (TDM) [3], where incomplete item exhibit is spoken to in reality. This is trailed by a theoretical viper [5].

III. PROPOSED METHOD

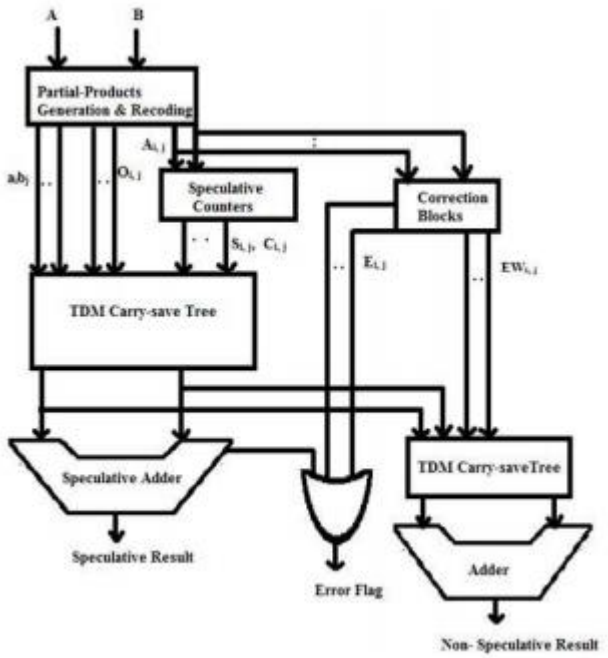

Fig.1: Architecture of Approximate Multiplier

A. Partial Product Recoding

Consider two partial products aibj and ajbi of the i+j-th column of the PPM. Now we will define two modified partial products:

Ai, j = aibj AND ajbi (1)

Oi, j = aibj OR ajbi (2)

Thus couple of partial products aibj and ajbi can be replaced with modified partial products Ai, j and Oi, j. The advantage of introducing such a recoding technique is the introduction of lower probability terms in the PPM. The probability of Ai, j is given by (.25)2 = 0.0625, much lower than the probability of the original partial product (i.e. 0.25). Alternatively the probability of Oi, j is 7/16. From the above two observations it can be concluded that speculative carry tree utilizes lower probability terms, to minimize the probability of misprediction. The introduction of recoded terms does not modify the total number of partial products, but introduces an additional very small delay for the recoded partial products. The figure below shows a 16 X 16 Partial Product Matrix (PPM) after being recoded.

B. Partial Product Partitioning Only the lower probability terms Ai, j is has been added in the speculation carry-save tree. Partial products that belong to the largest columns of PPM are singly recoded. In the figure given below the partial products in the columns 11, 12……22 are recoded.

C. Speculative Compression Although the probability Ai, j has been decreased with respect to the actual partial products, simple removal of Ai, j terms would bring about a large misprediction error probability. Thus, instead of omitting these terms we sum them in an approximate manner by using speculative compressors. A (m: 2) speculative counter has m inputs (x0….xm-1) and only two outputs Sum (S) and Carry (C). The speculation compressor counts the number of input bits and determines the output bits, on the supposition that not than more than three inputs are high. Analogously to full adders and half adders, the output C has a doubled weight with respect to S, so that 2C + S = x0 +x1……..+.xm-1 for: x0 +x1……..+.xm-1 3, it is not possible to represent sum x0 +x1……..+.xm-1, by using only C and S signals for all likely input configurations. The speculation counter computes the outputs based on the supposition that not more than three inputs are high: If this criterion is not met, an error occurs; the multiplication result is wrong and must be corrected.

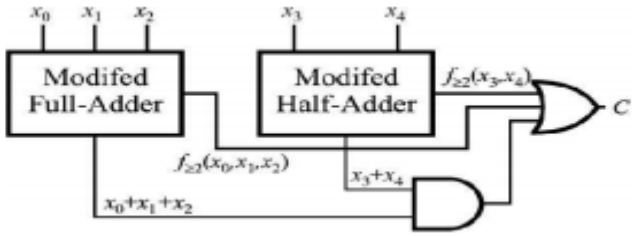

Fig.2: Speculative Compressor

IV. SIMULATION RESULTS

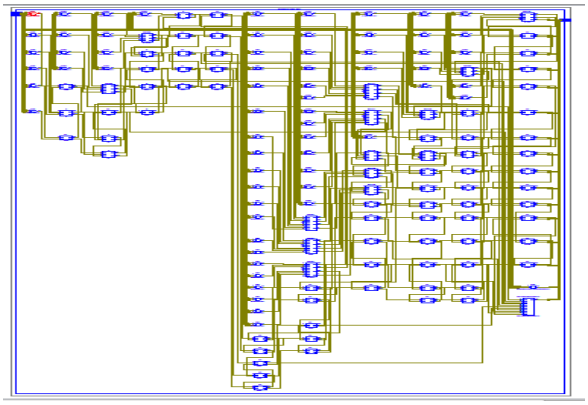

Fig.3: RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	88	960	9%
Number of 4 input LUTs	155	1920	8%
Number of bonded IOBs	32	108	29%

Fig. 4.Design Summary

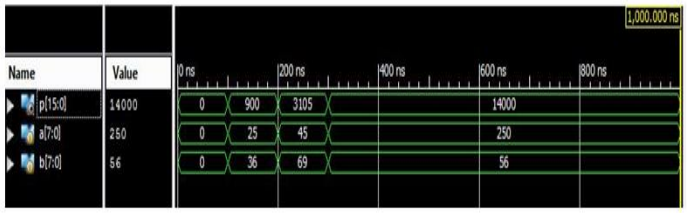

Fig.5: Approximate Multiplier output

V. CONCLUSION

Here a high speed approximate multiplier design has been proposed. Proposed design utilizes an optimised TDM tree. The circuit utilizes some of the partial product as well as a speculative compression tree to sum the recoded partial products. A speculative adder is used in the final carry propagate addition. The designs functionality have been verified using Xilinx ISE design suite 14.5 (web-edition). A comparison of the proposed design with conventional approximate multiplier showed that it has faster operation. The synthesis and simulation results showed that the proposed multiplier design gives 45.4% improvement in delay, lesser resource utilization and lesser power consumption as compared to multiplier without optimisation. In cases where multiplier speed is not critical, the use of speculative units remains unjustified. The performance of the approximate multiplier can further be improved by considering don't- care conditions and further by using variable latency adder instead of almost correct adder.

VI. REFERENCES

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