Design of Low Power High Performance 2-4 and 4-16 Mixed- Logic Line Decoders

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Abstract- This project involves a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoders. A 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed, by using mixed-logic 2-4 pre-decoders combined with standard CMOS post-decoder. All proposed decoders have full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at the 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

Index Terms- line decoder, mixed logic, pass transistor logic, transmission gate logic.

I. INTRODUCTION

The concept of digital data manipulation changes the society in attractive way even all the electronic gadgets are in digital formats. Due to invention of various digital IC technologies we are in VLSI era. These digital technologies have their own advantages and disadvantages. Due to invention of Bipolar Junction Technology (BJT) the first IC had been implemented that is TTL (Transistor- Transistor Logic). TTL logic provides higher packing density but slow turn off process. A new technology had been developed called ECL (emitter coupled logic) which is fastest logic but provides higher power dissipation. But unfortunately, in VLSI era, BJT is defeated by MOS technology. MOS provides lower power dissipation and high packing density than BJT. But again CMOS beat the MOS technology as it provides excellent static characteristics like lowest static power dissipation and highest Noise margin. But the problem with the CMOS ICs is their dynamic power dissipation and digital switching noise.

This problem is solved if we use differential amplifier. Because these amplifiers are not only less sensitive to noise but also enable us to bias amplifier and couple the amplifier stage together without the requirement for bypass and coupling capacitor. This born various technologies like SCL (source coupled logic), FSCL (folded Source Coupled Logic), MCML (MOS current Mode Logic). Static CMOS logic provides several advantages in designing digital circuit, that are low sensitivity to noise, good performance, low power consumption, etc. But it show some disadvantages while designing mixed mode ICs. In VLSI circuit, several logic gates switches simultaneously and resulting current causes switching noise. The mixed mode IC has both analog and digital circuit on single semiconductor die so this noise affect analog circuit through substrate coupling. This reduces speed and accuracy of mixed mode ICs. Various methods are used to reduce this noise in mixed mode ICs like separate analog and digital supply line, diffuse guard band, bonding pads etc. Source coupled logic(SCL) was developed to reduce this digital switching noise and it is most successful methods among all the constant current source technique.

Now a day's power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. Chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. Decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. Applications of decoders are wide; they include data de-multiplexing, memory address decoding, seven segment display etc. A decoder is a simple circuit that converts a code into a set of signals. It is named as decoder because it changes the big coded data into different simple combinations which can be used to drive any signal, but we will begin our study of encoders and decoders because they are simpler to design. Active instructions occur only within a sub-set of all instructions.

II. EXISTING SYSTEM

As a decoder, this circuit takes an n-bit binary number and produces an output on one of 2n output lines. It is therefore commonly defined by the number of addressing input lines and the number of data output lines. Typical

decoder/demultiplexer ICs might contain two 2-to-4 line circuits, a 3-to-8 line circuit, or a 4-to-16 line circuit.

A. 2-4 line decoder:

A 2–4 line decoder generates the 4 minterms D_{0-3} of 2 input variables A and B. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0.An inverting 2–4 decoder generates the complementary minterms I_{0-3}, thus the selected output is set to 0 and the rest are set to 1,In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gates show in below figure. whereas an inverting decoder requires 2 inverters and 4 NAND gates. both yielding 20 transistors. A 2-to-4 decoder truth table shown in below.

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

1.TRUTH TABLE OF THE 2–4 DECODER

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

2. TRUTH TABLE OF THE INVERTING 2–4 DECODER

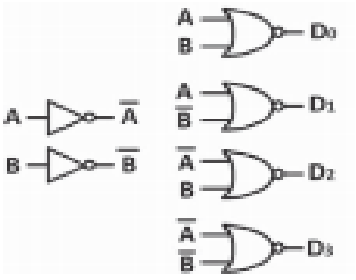

Fig.A: Non-inverting NOR-based decoder

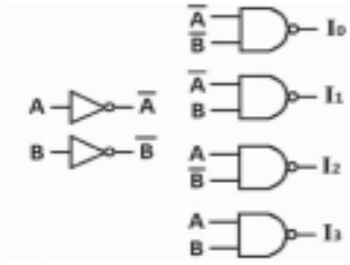

Fig.B: Inverting NAND-based decoder

B. 4–16 Line Decoder:

A 4–16 line decoder generates the 16 minterms D_{0-15} of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I_{0-15}. Such circuits can be implemented using a pre-decoding technique, according to which blocks of n address bits can be pre-decoded into 1-of-2n pre-decoded lines that serve as inputs to the final stage decoder Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gate and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

III. PROPOSED SYSTEM

Transmission gate logic (TGL) can efficiently implement AND/OR gates. It can be applied in line decoders. They are full-swinging, but not restoring for all input combinations.2-input AND/OR transmission gates shown in below

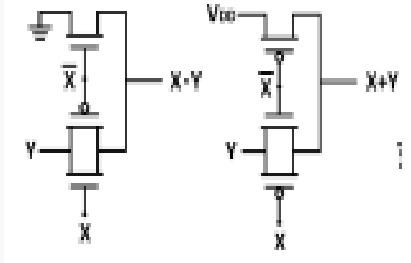

Fig.C: AND/OR gates using TGL

In PTL there are two main circuit styles: in first style use nMOS-only pass transistor circuits, like CPL. And in second circuit model use both nMOS and pMOS pass transistors, like DPL and DVL. The style we consider in this work is DVL (dual valued logic), which preserves the full swing operation of DPL with reduced transistor count .The 2-input DVL AND/OR gates are shown in below figures. They are full swinging but non-restoring, as well.

If complementary inputs are available, the TGL/DVL gates require only 3 transistors.

Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using

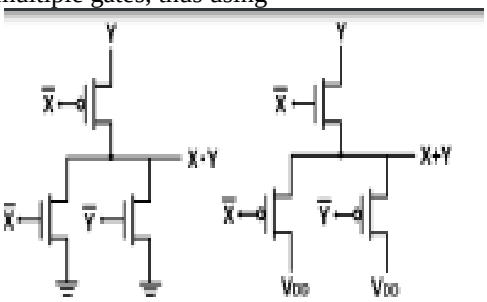

Fig.D: AND/OR gates using DVL

TGL and DVL can result to reduced transistor count. In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y as the control signal and propagate signal of the gate, respectively. Using a complementary input as the propagate signal is not a good, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the function (A B) or implication (A+ B) function, it is more efficient to choose the inverted variable as control signal. When implementing the (AB) or (A + B) function, either choice is equally efficient. Finally, when implementing the NAND (A+ B) or NOR (A B) function, either choice results to a complementary propagate signal, perforce.

A. 14 transistor 2-4 low power Topology:

Designing a 2–4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14.

Let us assume that, out of the two inputs, namely, A and B, we aim to eliminate the B inverter from the circuit. The Do minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. The D1 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. The D2 minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. Finally, The D3 minterm (AB) is implemented with a TGL gate, where B is used as propagated signal. This is best choice for eliminating B inverter. resulting in a 14-transistor topology (9 nMOS and 5 pMOS).

Following a similar procedure with OR gates, a 2–4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: I0 and I2 are implemented with TGL (using B as the propagate signal), and I1 and I3 are implemented with DVL (using A as the propagate signal). The B inverter can eliminated. Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation and area. The two new topologies are named "2–4LP" and "2–4LPI," where "LP" stands for "low power" and "I" for "inverting." Their schematics shown in below.

B. 15 transistor 2-4 High-performance Topology:

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, D0 and I3 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation and area. They are named "2–4HP" (9 nMOS, 6 pMOS) and "2–4HPI" (6 nMOS, 9 pMOS), where "HP" stands for "high performance" and "I" stands for "inverting." The 2–4HP and 2–4HPI schematics are shown in below.

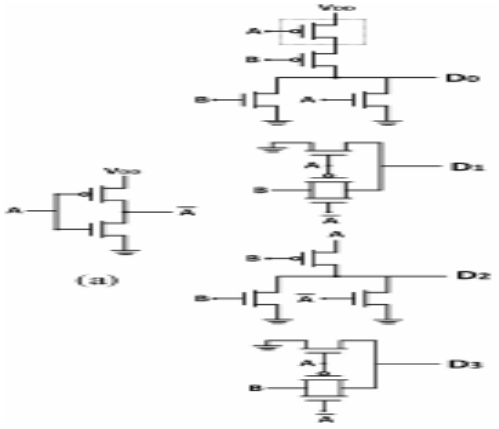

Fig.E: New 14-transistor 2–4 line decoders

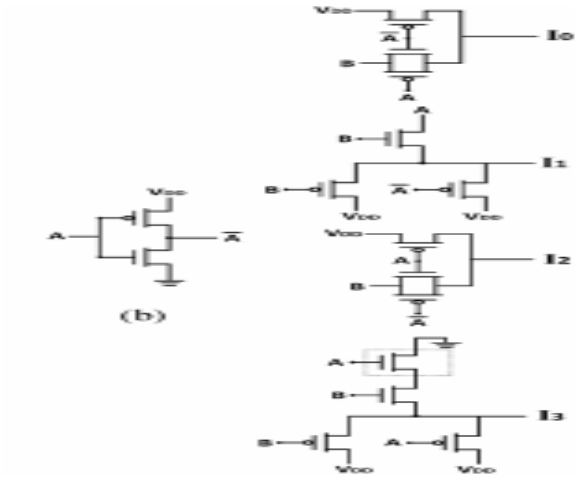

Fig.F: New 15-transistor 2–4 line decoders

C. 4-16 line decoders:

We implemented four 4–16 decoders by using the four new 2–4 as pre decoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The 4-16LP which combines two 2–4LPI pre decoders with a NOR-based post decoder; 4–16HP which combines two 2–4HPIpredecoders with a NOR-based post decoder 4–16LPI which combines two 2–4LP pre decoders with a NAND-based post decoder; and, finally, 4–16HPI which combines two 2–4HP pre decoders with a NAND-based post-decoder. The "LP" topologies have a total of 92 transistors, while the "HP" ones have 94, as opposed to 104 with pure CMOS.

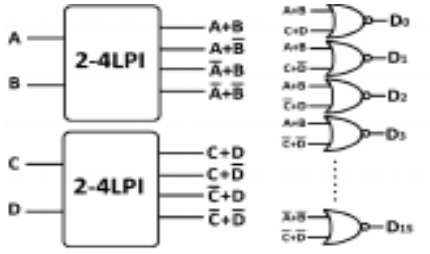

Fig.G :4-16LP line decoder

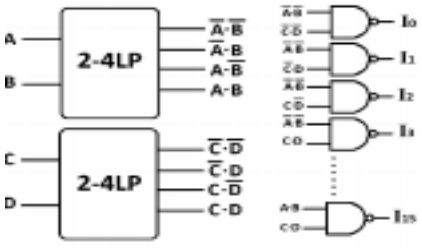

Fig.H :4-16LPI line decoder

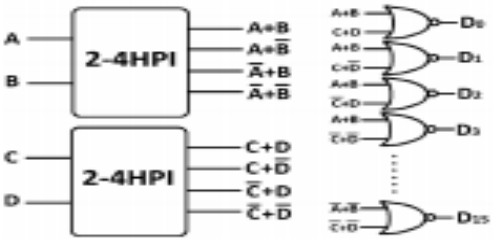

Fig. I: 4-16HP line decoder

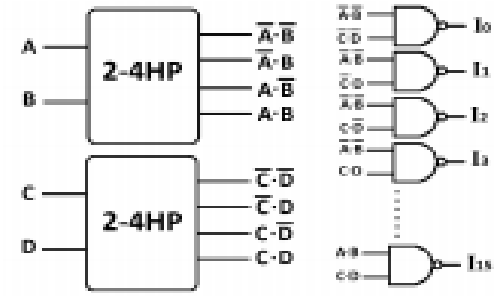

Fig.J: 4-16HPI line decoder

IV. EXTENSION

Proposed system of the project is done using 32 nm technology. CMOS Logic used in the project for 32 nm technology provides the layout design for a particular circuit which shows the area and the power required to design a circuit. In the extension of the project 18nm technology is used. Change in the nanometer technology gives the power difference. With the decrease in the nanometer technology in the extension particular area and power required for the 2-4 and 4-16 decoder will be reduced.

The extension process is exactly similar to the proposed one but when nanometer technology is changed in the software, VDD and Vbias changes which lets the output to give high performance than the proposed system.

V. RESULT

Schematic:

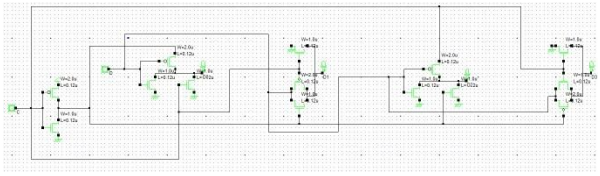

Fig.1: Schematic Design Of 2-4 Inverting Low Power Decoder

Layout Design:

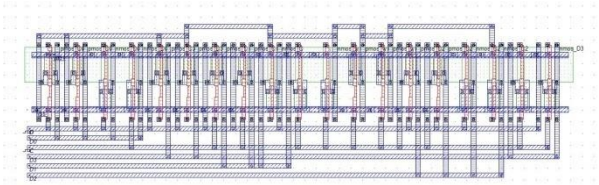

Fig.2: Layout Design Of 2-4 Inverting Low Power Decoder

Waveforms:

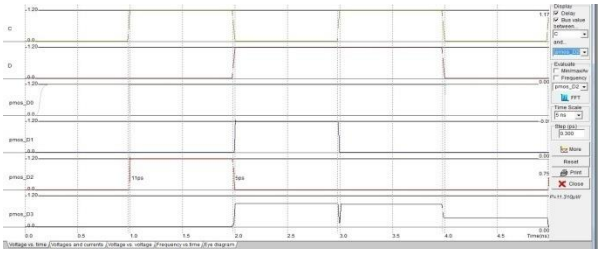

Fig.3 : Waveforms Of 2-4 Inverting Low Power Decoder.

Schematic:

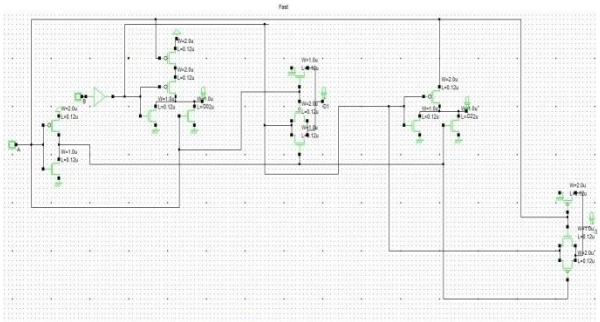

Fig.4: Schematic design of 2-4 inverting high performance decoder

Layout Design:

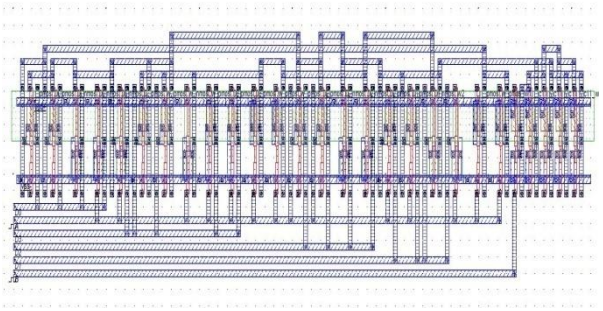

Fig.5: layout design of 2-4 inverting high performance decoder

Waveforms:

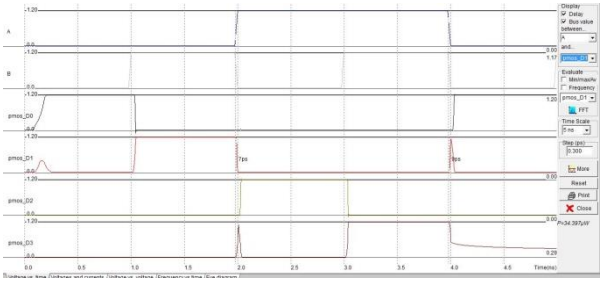

Fig.6: waveforms of 2-4 inverting high performance decoder

Schematic:

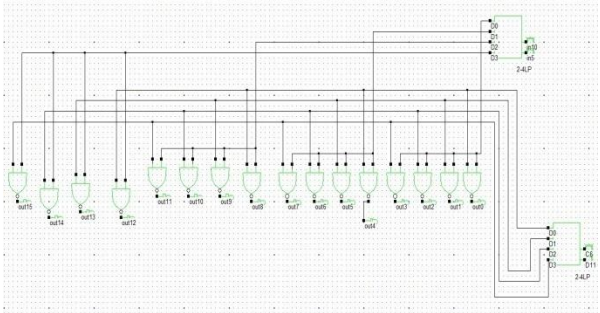

Fig.7: schematic design, of 4-16 inverting low power decoder

Layout Design:

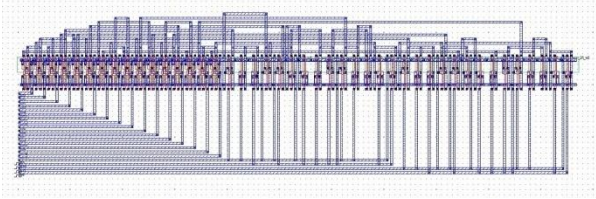

Fig.8: layout design of 4-16 inverting low power decoder

Waveforms:

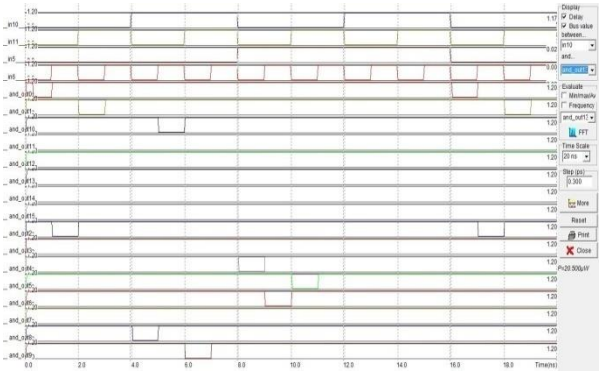

Fig.9: waveforms of 4-16 inverting low power decoder

Schematic:

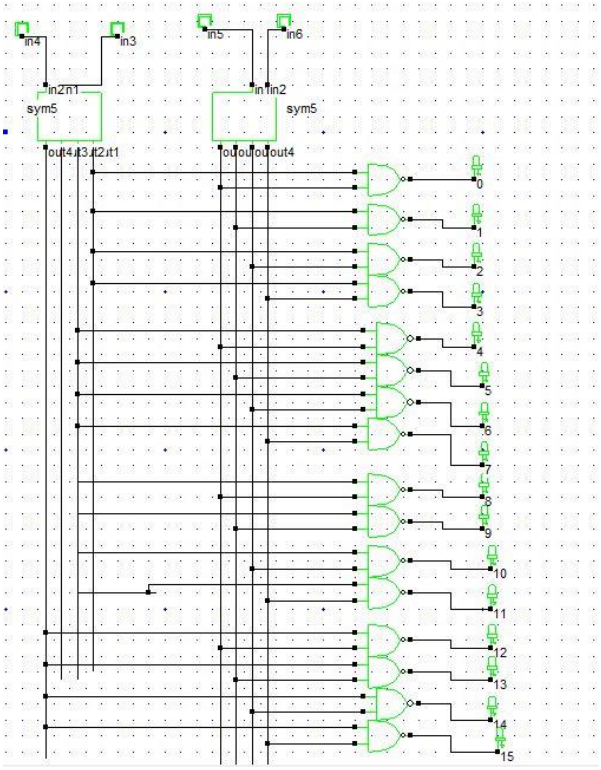

Fig.10: schematic design, of 4-16 high performance decoder

Layout Design:

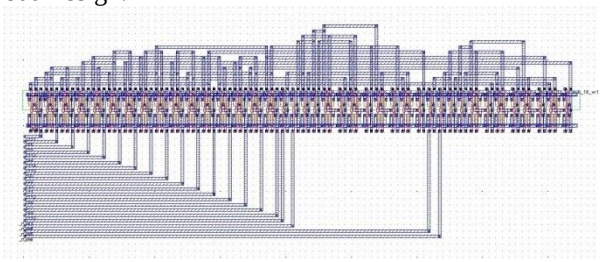

Fig.11: layout design of 4-16 high performance decoder

Waveforms:

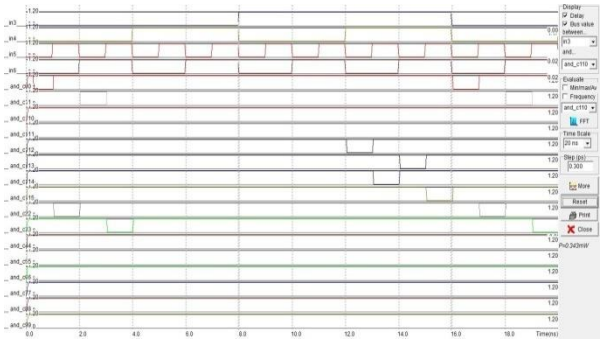

Fig.12: waveforms of 4-16 high performance decoder

Nanometer Technology	Design	Power
32nm	2-4 low power decoder	22.372mw
	4-16 low powerdecoder	28.224mw
18nm	2-4 low power decoder	15.819mw
	4-16 low powerdecoder	13.147mw

VI. CONCLUSION

From the above proposed method we have use mixed logic to design line decoders so that we achieve less delay, and also reduced number of gates. So that the area for the design will be reduced and also power consumption is less. It is possible that if the power is reduced then the temperature will also get reduced. Thus we propose the above design for area efficient and low power consumption for decoders.

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