Design Implementation of Folding & Interpolating ADC using Submicron CMOS Technology

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Abstract- The Analog-to-Digital Converters (ADCs) are basic interface in blended mode plan and the core of the cutting-edge sign preparing frameworks. Numerous applications like hard plate drive, wired and remote correspondence frameworks and so on request ADCs with high change speed and low control. For rapid applications, Flash ADC is generally utilized because of its parallel engineering. In any case, for N-bit goals, Flash ADC needs (2N-1) comparators and 2N resistors, which devour enormous power and possess huge area. Folding and Interpolating engineering is an elective way to deal with diminish the unpredictability of Flash ADC and keep high change rate. The entire design of Folding and Interpolating ADC is been depicted. Primary structure squares of this ADC are resistive stepping stool, collapsing speaker, Interpolator, Comparator and encoder. This exposition work centers on execution, recreation and portrayal of low control 6-piece collapsing and inserting ADC. The entire ADC design is actualized utilizing TSMC 0.18um CMOS innovation at 1.8V inventory voltage.

Keywords- Analog to Digital Converters (ADCs), Propagation delay, Offset Voltage, Power Dissipation.Transient Analysis, Differential amplifier

I. INTRODUCTION

Analog to digital converters (ADCs) are play main and important role in modem signal processing and communication systems. The digital domain provides advantages such as high security, easy storage capability, less noise affected and many other over the analog. The regenerative repeater is used in digital communication for long distance, Due to regenerative repeater the digital communication is more reliable. Due to such advantages, most of modern electronics are mainly digitally operated, permitting for advanced digital signal processing (DSP). But the real-world signal is in analog form, the signal coming from different transducer which is real world information in form of analog signal. This analog signal needs to convert in digital form. The facility of converting analog signal from different transducer into digital signal provides by Analog to Digital Converter (ADC) as shown in Figure 1. Similarly, after signal processing in digital domain, the signal is converted back into analog. This is done by Digital to Analog converter (DAC).

The applications of ADC contain process control, DC instruments, modems, thermocouple sensors, digital radio, video signal acquisition, communication systems, hard disk drive etc. The ADC should be introduced with low power and higher speed due to various reasons. First the quick advent of battery-operated portable system requires lowpower dissipation in order to extend battery life, and a lowest number of battery cells to lessening the volume and weight of the system. Another reason is the lesser feature sizes obtainable by today's VLSI technology. Reduced device dimension may create higher power density which results in failure.

Fig.1: Data Conversion Flow

By introducing analog pre-processing techniques, it is possible to reduce number of comparators in ADC design. So high speed ADC can be designed using folding and interpolating techniques. The folding and interpolating are called analog pre-processing. Figure 2 shows the block diagram of folding and interpolating ADC.

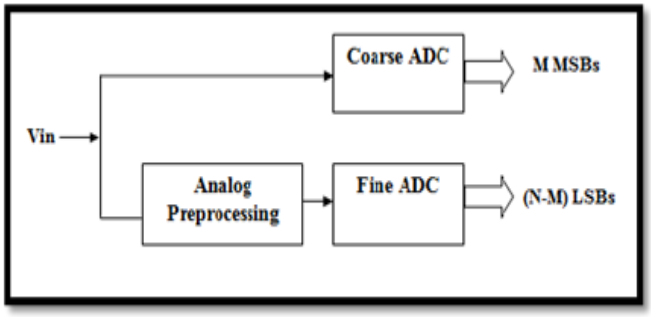


Fig.2: Folding and Interpolating ADC Block Diagram

The folding and interpolating ADC contains of a parallel functioning coarse converter and a fine converter.The input signal is directly quantizes by coarse converter, whereas the fine converter is led by the analog pre-processing. Folding amplifier, interpolation block, comparators and digital encoder are the basic building blocks of folding and interpolating ADC.Analog pre-processing block consists of folding amplifier and interpolator.

Folding amplifier folds the input signal by some factor called folding factor. The required number of comparators can be reduced by this folding factor. The number of comparators is further reduced by generating intermediate signals from the output of the folding amplifier. This is called interpolation.

ADC (Analog to digital convertor) offers connections between the analog signal world and the binary digital systems. So, it required in all digital signal processing applications and system. To convert the analog signal field to digital field can create from numerous types of transducers that convert position, physical phenomena, temperature, pressure, motion, images, sound, etc., to electrical signals. The applications of ADC such process control, workstations, digital radio, DC instrumentation, automatic test equipment, thermo-couple sensors, audio recording, strain gauges, compact disc and digital audio tape, weigh scales, modems, video signal acquisition and storage oscilloscopes. In current day technology such as CMOS VLSI technology, These A/D converters are simplyimplementable.

Before detailed architecture of different high-speed ADC is discussed, some commonly used terms describing the performance of data converters need to be reviewed.

Resolution: The number of bits of resolution refers to the smallest analog input level to cause change in the digital output word. Thus, an n-bit resolution implies that the converter can resolve 2n distinct analog levels.

LSB (Least Significant Bit): One LSB= (full-scale input voltage)/resolution.

For example, with input full scale= 5V and resolution=10 bits, then 1 LSB= 5/210 = 4.9mV.

Sampling Rate:Sampling rate or sampling frequency Fs is also an important characteristic of the ADC and defines the rate at which the analog input is sampled and converted to the digital domain. It is usually determined by the Nyquist bandwidth and must be larger than twice the inputfrequency

Accuracy: The absolute accuracy of a converter is defined to be the difference between expected and actual transfer responses, which includes the offset, gain, and nonlinearity errors. The relative accuracy is the accuracy after the offset andgain errors have been removed, which is usually referred to as the maximum INL error. Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bits, or as a fraction of an LSB.

For example, in order to achieve 1/2 LSB integral linearity, an 8-bit accuracy implies 1/28 = 0.4% matching, while a 12-bit accuracy implies 1/212 = 0.025% matching.

Signal to Noise Ratio (SNR): Signal to noise ratio (SNR) is the ratio of the signal power to the total noise power at the output. This is usually measured with sinusoidal input.

Signal-to-Noise and Distortion Ratio (SNDR): This is the ratio of the original input signal power to the background noise and distortion power, or equivalently, the rms ratio of the input signal amplitude to the noise and distortion amplitude.

Total Harmonic Distortion (THD): It is the ratio of the power of all harmonics to the power of the fundamental signal component.

The main criteria for selecting high speed ADC architectures are resolution and bandwidth. However, other requirements such as power dissipation, chip area, supply voltage, latency, operating environment and technology impact architecture selection. In this section, a brief comparison of high-speed ADC architectures is presented, emphasizing the advantages and disadvantages of each.

The flash ADC is the fastest way to convert an analog signal to digital codes because it requires only one clock cycle per conversion and is ideal for wide bandwidth applications. Figure 3 shows the architecture of a typical N-bit flash ADC. It consists of an array of (2N– 1) comparators. A resistor divider with (2N – 1) resistors provides the reference voltages for the comparators. The reference voltage for each comparator is one least significant bit greater than the reference voltage below it. The output of the comparators is fed into a digital encoder which generates the binary bits. One drawback of this type of converter is the requirement for (2N - 1) comparators and resistors. As a result, the flash ADC occupies a large die area and dissipates a significant amount of power. Thus, Flash ADC architecture is not suitable for high resolution (bits) ADC and its usage is limited up to 6-bit resolution.

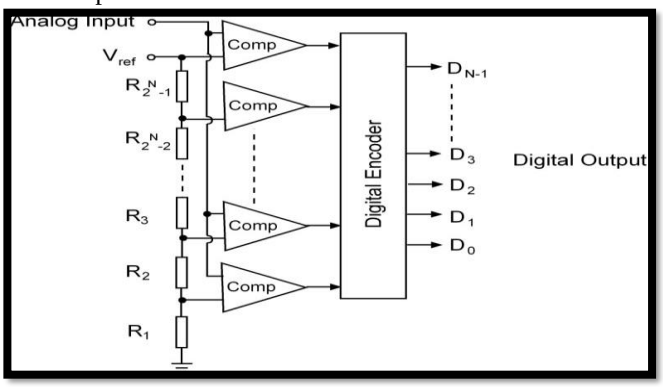


Fig.3: Flash ADC Topology

Figure 4 shows the block diagram of a two-step ADC consisting of a coarse quantizer, a digital to analog converter (DAC), a subtracter and a fine quantizer. The input signal is applied to a coarse quantizer flash ADC which generates the first M bits. Next, using an M-bit DAC, the output of the coarse quantizer is converted into an analog signal and subtracted from the input signal. The error signal is then quantized using a subsequent (N-M) -bit fine quantizer flash ADC which generates the remaining bits. The die area of the ADC is reduced by performing the conversion in two (or more) clock cycles.

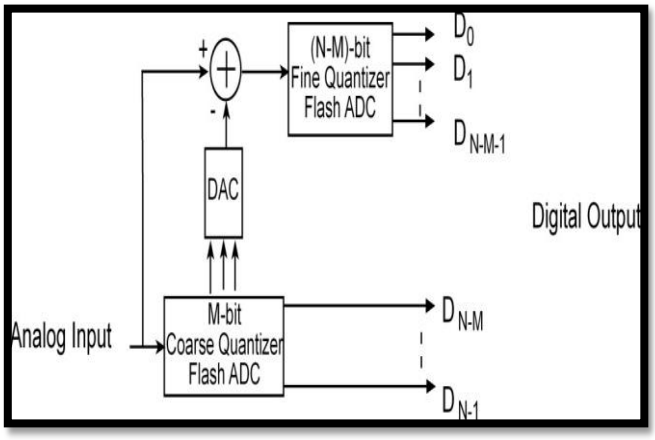


Fig.4: Two Step N-bit ADC Architecture

An N-bit folding analog to digital convertor works in a related manner to a two-step ADC using quantizing the received signal through a coarse quantizer flash ADC and by generating a remainder signal which is additional quantized by a fine quantizer flash ADC, as shown in figure 5.

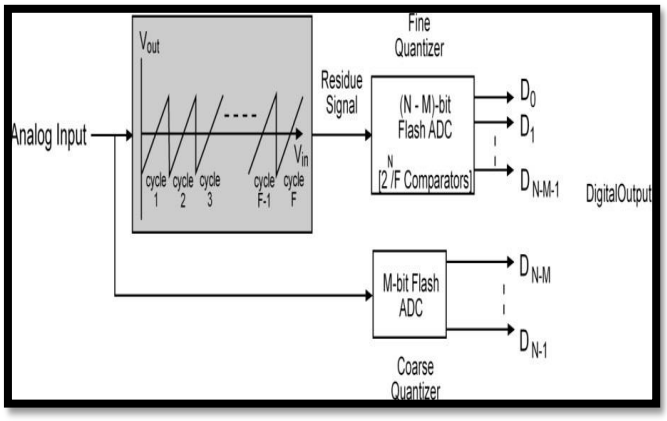


Fig.5: Folding ADC Topology

The remainder signal is produced by an analog folding circuit which decreases the dynamic range of the input signal using the folding factor F, therefore resulting in a decrease in the number of comparators. The factor of folding F is defined as the number of zero crossings in the folded signal for one full scale input signal. The fine quantizer produces the (N – M) bits. The coarse quantizer generates M* bits. Details of the folding block are illustrated in Figure 6. The input signal is fed to several folding amplifiers where it is compared to a set ofreference voltages. The folding amplifiers convert the input signal into a repetitive output signal phase shifted by 45o. The differential outputs of the folding amplifiers are then given to a comparator to convert the analog information into digital data. Lastly, a encoder with bubble error modification is used to get the binary digital codes.

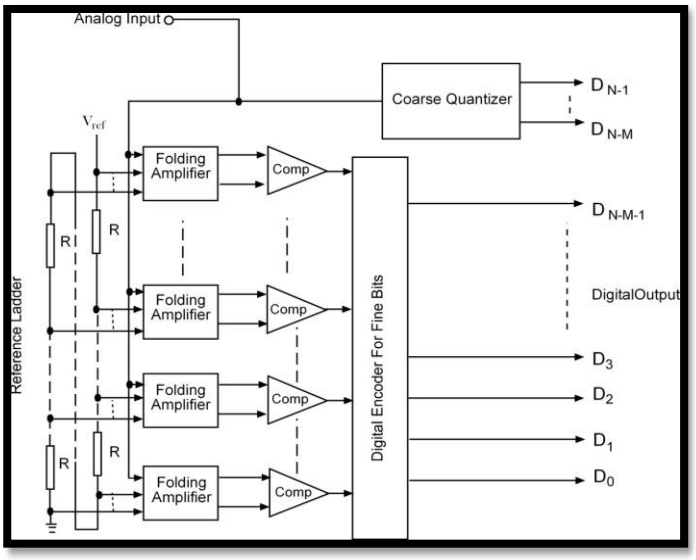


Fig.6: Folding ADC Architecture Showing Details

A way to minimize nonlinearities associated with the folding amplifier, as well as reduce the number of folding amplifiers is to average the folded signals by using an interpolating resistor string between the folding amplifiers and the comparators as illustrated in Figure 7.Interpolation is an effective way to reduce complexity and nonlinearities without significantly increasing circuit complexity, die area and power dissipation. The folding-interpolating ADC architecture was chosen for the implementation of the high-speed ADC.

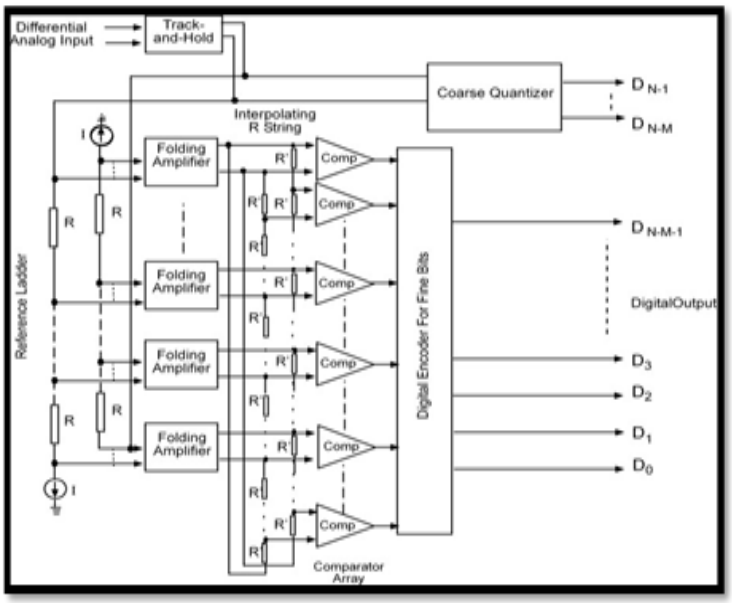


Fig.7: N-bit Folding and Interpolating ADC Architecture.

II. EXISTING ARCHITECTURES OF 6-BITS FOLDING AND INTERPOLATING ADC

Figure 8 demonstrations the block figure of a folding A/D converter. The folding and interpolating A/D converter has two distinct converters, that is, the coarse and the fine converter. The input signal is given into both converters in similar. The input voltage is fed to a pre-processing circuit represented as the "folding circuit," and the output of pre- processing is linked to a fine ADC for (N-n)-bits. The input signal is also connected to coarse ADC for n-bits.

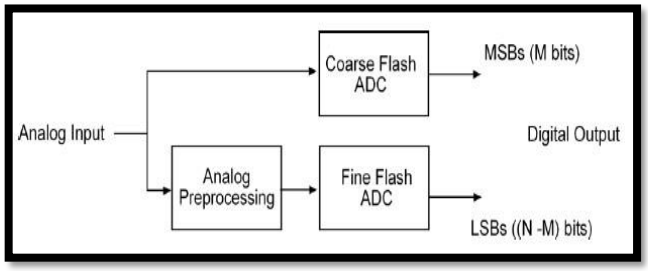


Fig.8: N-bit Folding ADC

In an N-bit flash ADC, the input signal is compared to $(2^N - 1)$ reference voltages [3]. As a result, many comparators and resistors are required to generate the digital codes for high resolution ADC. In a folding-Interpolating ADC, input analog preprocessing allows the number of comparators to be reduced by folding the signal using folding amplifiers. For a folding factor of F, the folded signal spans a much smaller dynamic range than the original input and as a result fewer comparators are required to convert the folded signal to yield the required resolution. The interpolation technique is used to generate intermediate signal from the folding amplifiers output. The interpolation is used to further reduce the number of comparators.

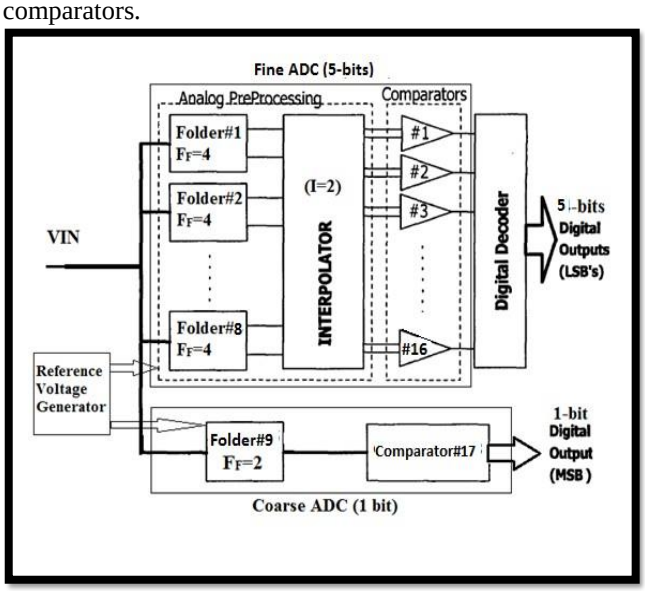


Fig.9: Architecture of 6-bits folding & interpolating ADC

The architecture of 6-bit folding ADC is presented in Figure 9. 5-bit fine A/D convertor and 1-bit coarse A/D convertor are connected parallel to generate 6 bits of digital data. The input signal and reference voltages are given to the fine and coarse converter over folding block. At the comparators the differential signals are applied as input. The comparators output is cyclic thermometer code. Lastly encoder changes cyclic thermometer code in binary code. In the architecture of Figure 9 two different paths are used to generate the digital output. This may lead to timing mismatches between the coarse and fine bit generation resulting in degradation of the resolution. This issue is not significant if the timing difference between the coarse and fine bits is negligible by comparison to the clock period. However, at high sampling frequencies, in the GHz range, bit synchronization is needed to align the coarse and fine bits.

III. PROPOSED FOLDING AND INTERPOLATING ADC

The folding amplifier, resistive ladder, interpolation, comparators and encoder are the basic building blocks of folding-interpolating A/D converter. Resistive ladder and Folding amplifier blocks are simulated using 0.18um CMOS technology with 1.8V supply voltage.

a. Resistive Ladder

In a folding & interpolating ADC, the reference voltage is needed for folding amplifier to compare input signal with it and get the differential output. So, we can use the Resistor ladder which is work as voltage divider. Resistor used in Circuit Diagram is 1k all the resistor with same value. Figure 10 illustrate the circuit of resistive ladder.

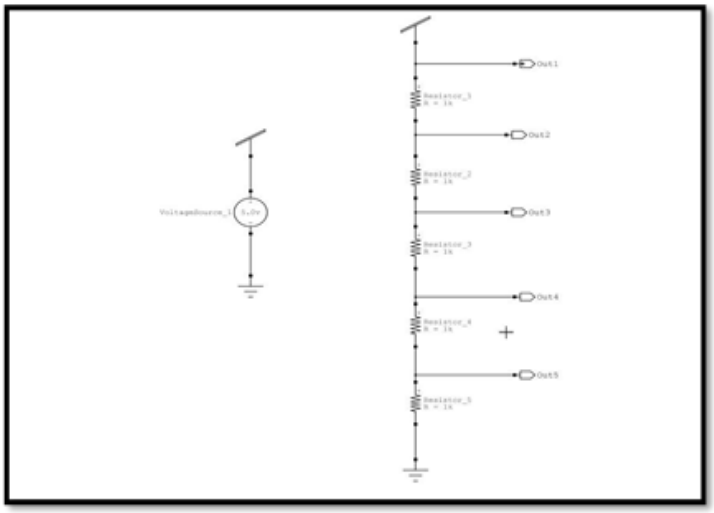


Fig.10: Circuit of Resistive ladder

b. Folding Amplifier

The differential pairs based voltage mode folding amplifier used. For achieve N folding factor of folding amplifier, N tail current

sources and N differential pairs are needed. This type of folding amplifier is shown in figure 11. By reference voltage Vref, the zero- crossing points are determined. Figure 11 shows 4 folding factor folding amplifier. It needs 4 cross-coupled differential amplifiers with tail current sources i1…. i4..,and Vr1…Vr4 indicates different reference voltages. The input of folding amplifier is input signal of converter and reference voltage Vr1…Vr4 Because of cross coupling in the differential amplifier in folding amplifier, two of tail currents are swapped to the load resistor R1 and other two are swapped to R2.

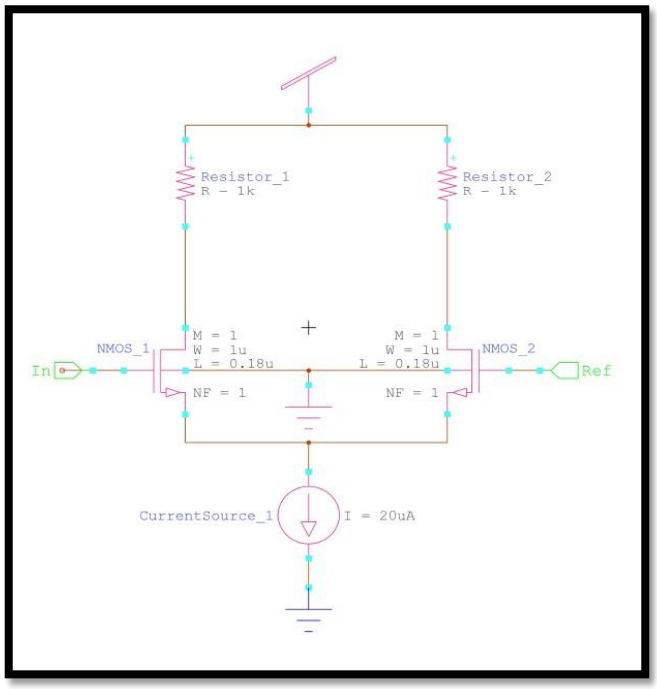


Fig.11: Circuit diagram of Basic Differential Amplifier

c. Generation of Zero Crossing Points

According to the architecture discusses in chapter 4, Eight folding amplifier are connected parallel to generate 32 zero crossing points. 32 zero crossing point in DCsimulation results shown in Figure 11.

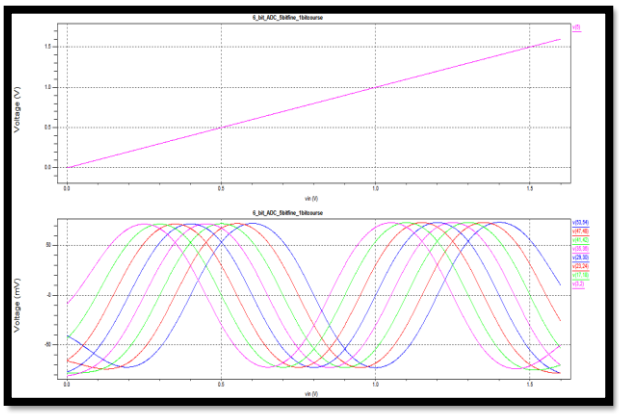
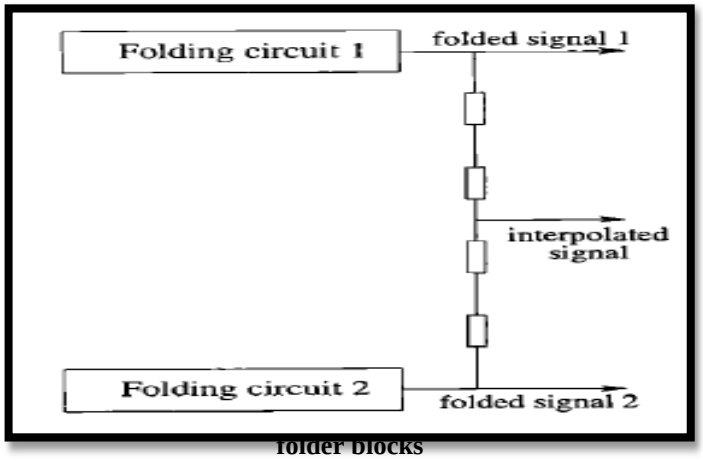


Fig.12: Generation of 32 Zero Crossing Points using eight folding amplifier

Which are define by reference voltage levels. Without growing number of folding amplifiers, the number of zero crossing points can increase by combine folding amplifiers with interpolation technique. The 64 reference voltages are produced through resistive ladder network. The frequency multiplication at the folder output as folding result. Lesser Folding factor and large parallel folder will help both folding and interpolating, but it will introduce large input capacitance. That's why here folding factor=4 and four such folding amplifier are chosen.

d. Resistive Interpolation

The Interpolation is technique to generate more folding waveforms without growing number of folding amplifiers. The interpolation of the folded signals can be done by two methods, namely current-mode interpolation and voltage-mode (resistive) interpolation. The technique used in current-mode interpolation is addition of currents reflected by current mirrors with different ratios. However, this method is complex, also the power require is more and due to the non-idealities of the current mirrors it is not very precise. Due to these the voltage mode resistive interpolation is favored. The resistive ladder is used to implement voltage mode interpolation. The design simplicity and low power operation is main advantages of voltage mode interpolation. However, greater factor of interpolating means greater nonlinearity error, Due to performing interpolation between nonlinear signals. The scheme uses factor of interpolation is 2 to escape zero crossing point error and non-linearity.



folder blocks

Fig.13: shows how the resistive interpolation technique can be implemented to generate intermediate signals from the output of folding amplifier. The principle of resistive interpolation is presented in figure 13. The resistors string serves as a resistor divider to interpolate the voltage between the two folding signals. Hence, additional folding signals are produced without employing more parallel folding amplifiers.

IV. SIMULATION RESULT

a. Simulation Results of Resistive Ladder

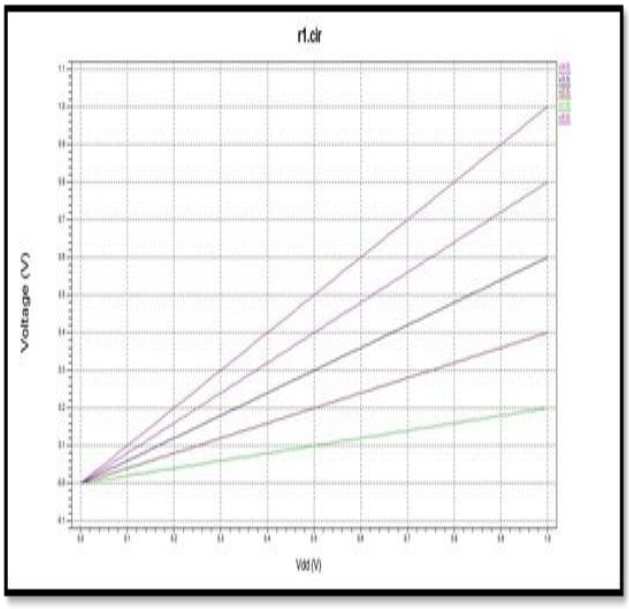


Fig.14: Waveform of Resistive Ladder as many voltage level

b. Simulation result of basic differential amplifier

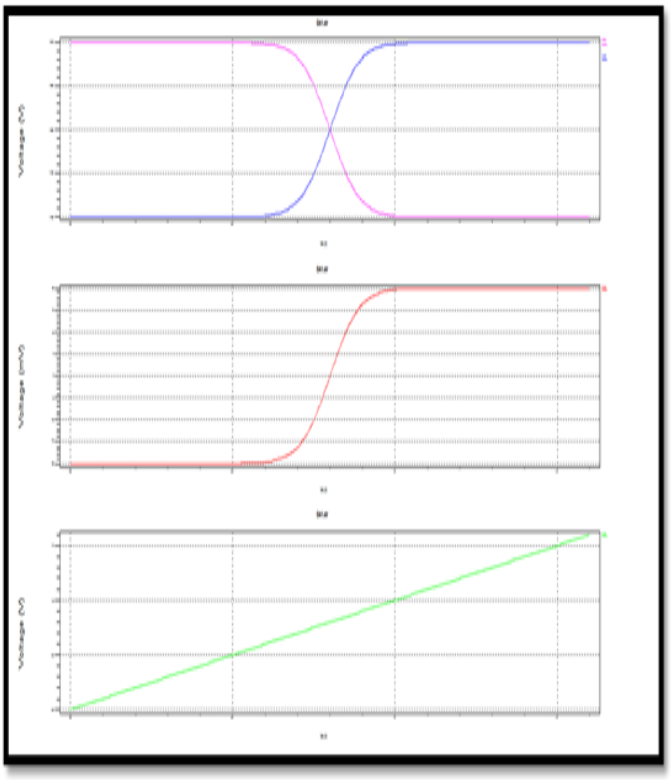


Fig.15: Transfer Characteristic of Single Differential amplifier (VIN=1.6V)

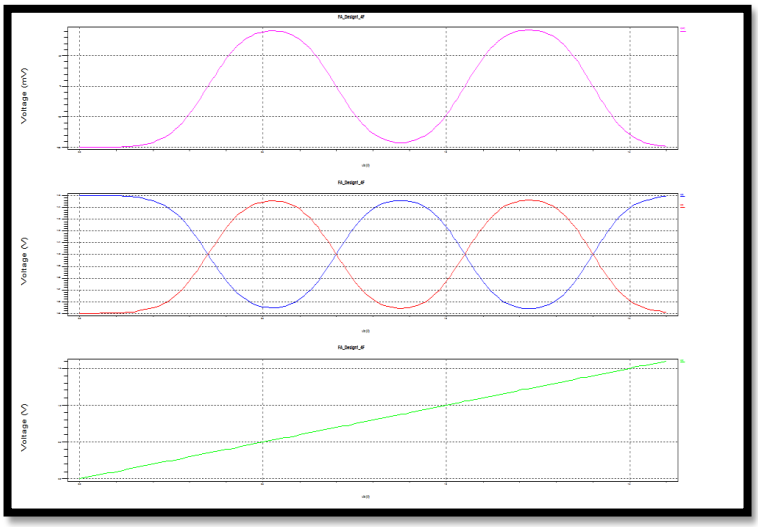


Fig.16: DC Analysis of Folding Amplifier with folding factor=4

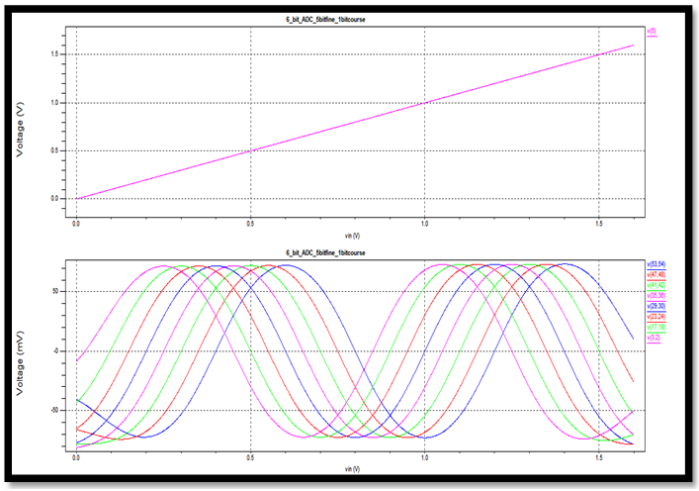


Fig.17: Generation of 32 Zero Crossing Points using eight folding amplifier

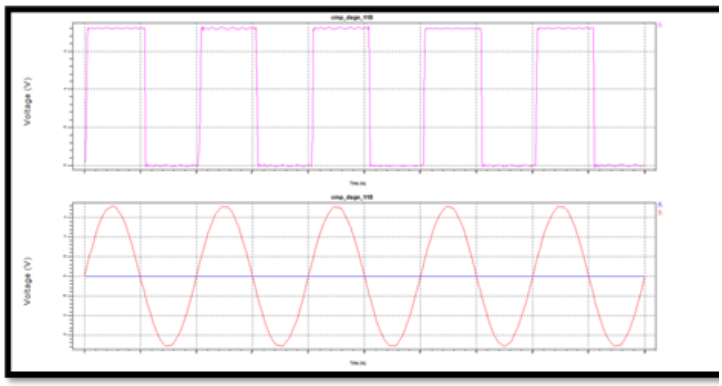


Fig.18: Transient Analysis of Comparator with Differential Input Signals Vin=±1.8V sinusoidal, Fin=50MHz

c. Simulation Results of CombinedBlocks

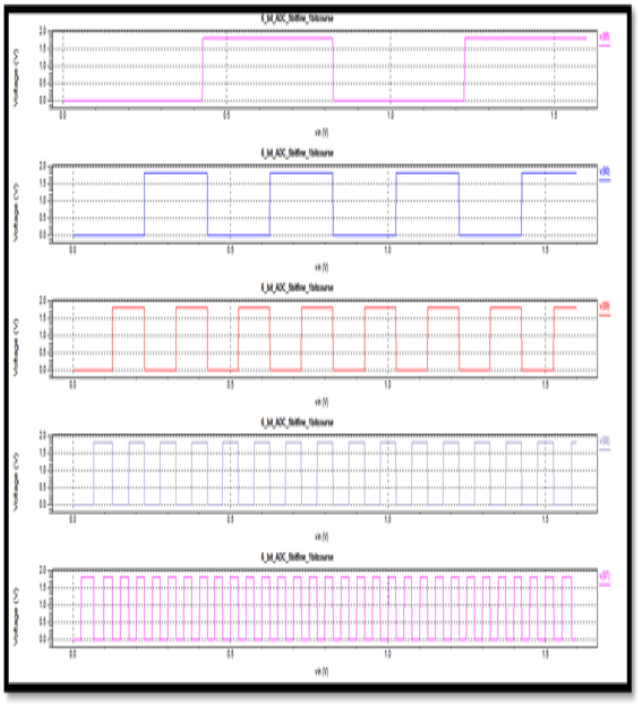


Fig.19: Simulation result of the Fine converter

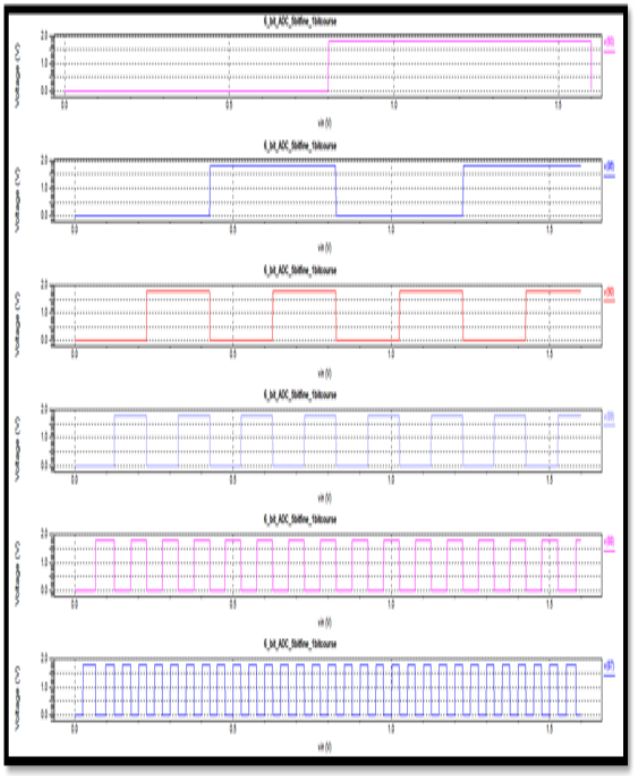


Fig.20: Simulation result of the whole ADC design (6 bit)

Table1. The comparative table for the folding-interpolating ADC

Reference	Technology (um)	Resolution (bits)	Power Dissipation(mW)
Nabavi [10]	1.2	10	22
Yihui Chen [7]	0.13	10	195
Nauta[16]	0.8	8	45
Wan Ahmad [1]	0.18	8	497.02
Xubin Zhu[6]	0.18	8	290
This work	0.18	6	7.07

V. CONCLUSION

High speed-medium resolution analog to digital conversion can be achieved using folding and interpolating ADC architecture. Due to the folding and interpolating operation on input signal, the required number of comparators can be reduced significantly with compared to flash ADC. In this work, 6 bit folding and interpolating ADC is implemented and simulated using standard TSMC 0.18um CMOS Technology. The folding factor of folding amplifier is four (F=4). The architecture uses folding amplifier for both coarse and fine ADC. The simulation and analysis of folding amplifier, interpolation, comparator and encoder are carried out at the input frequency of 50MHz. It is found that they are working in a proper condition and implement their basic function. The design achieves low power operation.

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