A Review of Various Full Adders Designs for High Performance Applications

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Abstract- Adders are the key components in building of any digital circuits. In this survey paper, we will present a review on the study of different logic style of full adders and taking positive aspects of these design style to form a hybrid for low power consumption and minimum propagation delay. Different logic styles have been compared taking full adder design as a reference & power dissipation and delay as a reference parameter.

Keywords- Full adder, Hybrid adder, CMOS, Power Dissipation.

I. INTRODUCTION

Increased usage of the battery-operated portable devices, like cellular phones, personal digital assistants (PDAs), and notebooks demand VLSI, and ultra large-scale integration designs with an improved power delay characteristics. Full adders, being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years . As growing importance of low power, small area & high speed circuitry design methodologies it become popular for wide application in VLSI like in design of microprocessor & system mechanism.

Need of Low Power VLSI Design

First of all, it is very important to understand what actually power dissipation is. It is actually the rate through which energy is being transferred from certain source to the device in use. Power dissipation [4] acts as an actual hurdle in designing any device. There are many reasons why this issue is emerging these days. Some of the major issues are being discussed over here The devices such as notebook computers, laptops etc have a must need of long lasting battery. Most of the applications that are portable use the Nickel Cadmium(NiCd) batteries which are rechargeable. The battery industry has been working over the life of batteries from over the decade to extend the hours a battery can work without being recharged. There are continuous efforts to develop batteries which are much more efficient than the NiCd and have higher capacity in terms of energy but still not much growth has been noticed. Till the turn of century, only about 40% of the energy density has been improved. There are some better and advanced technologies like the Nickel-Metal Hydride (Ni-MH) batteries which have good characteristics of energy density, but still their lifetime is also low. Thus, it is clearly visible that we can have only limited improvement and gains with the advent of battery technology. Therefore, it is important to develop low power design techniques so as to increase the working efficiency of the portable devices [8].

II. LITERATURE SURVEY

Parth Bhattacharyya (2014) [1] In this article a hybrid 1-bit full adder configuration utilizing both corresponding metal-oxide- semiconductor (CMOS) rationale and transmission gate rationale is accounted for. The outline was executed firstly for 1 bit and after that reached out having 32 bit too. This circuit implementation was executed utilizing Cadence Virtuoso instruments in 180nm and 90-nm innovation.

Basant kumar and sujit kumar patel (2013) [2] In this paper made an analysis on the logic operations involved in conventional CSLA and BEC-based CSLA to identify both the data dependency, redundant logic operations. They have eliminated all the redundant logic operations of conventional CSLA.SQRT-CSLA on average for different Bit-width due to small carry output Delay.

Pakkiraiah chakali et al (2012) [3] In this paper adopted gate diffusion input technique which is a low power technique to design any digital combinational system to reducing the transistor count with full swing. Dynamic power can be reduced in GDI technique and also it reduces the latency of the circuit which helps the carry look ahead adder design consuming low power and gives high speed with less delay.

Balakrishna Batta et al (2012)[4] In this paper introduced that the GDI technique was a novel technique for low power digital circuit design which allows reduction in power consumption, propagation delay and transistor count of the digital circuit. The performance of GDI was compared with cmos and different other design logic for digital circuit. Comparison are made among Full adder with GDI, standard cmos and some pass transistor logics. They found that the GDI technique will effectively reduce the size of the chip and allows high density of fabrication. **Pooja varma and Rachana Manchanda (2014) [5]** In this paper analyzed that the basic GDI logic suffers from swing degradation, fabrication complexity and bulk connection. This can be overcome by modified GDI with full swing logic. Basic building blocks of digital systems are analyzed and made

comparison on cmos and GDI logic with respect to area, power consumption and propagation delay. They suggested that the digital circuits implemented using full swing gates have better performance and less static power dissipation than static cmos technique.

B. Ram Kumar and H.M.Kittur (2012) [6] In this paper proposed gate level modification to effectively reduce the area and power of carry select adder. Higher bit width as 16, 32 and 10 64 bit SQRT-CSLA can develop based on this modification and made comparison with conventional CSLA architecture. The proposed CSLA design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. The power delay product (PDP) as wells the area delay product (ADP) of proposed design results analysis shows that the proposed CSLA architecture design is better than the regular SQRT CSLA design.

Hybrid Full Adder:-

Nowadays, battery operated portable devices like laptops, notebooks, cellular phones etc are widely used in the market. These devices have demand of the VLSI with the designs that are ultra large scale integrated and also where the power delay is very low. Full adder being the basic building block of all the circuits and it is important to reduce its power and delay. Over the years researchers have been focusing over the full adder only as it is the basic and the fundamental unit behind the building of all the circuit applications.

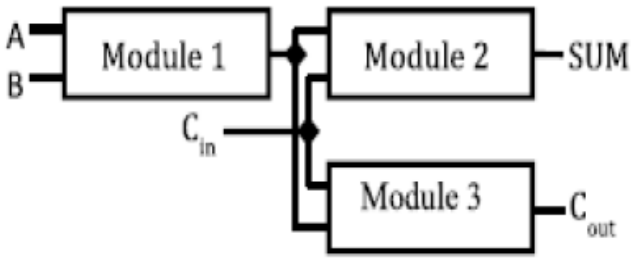

Fig.1: Block Diagram of Full Adder

To implement out the 1-bit full adder, different logical methods were being researched out where each method has its own benefits and issues. There have been two designs that have been investigated out so far.

They are Static style and Dynamic style.

The static adders are the one which are efficient with simple design and less requirement of power along with more reliability. But the area required for the chip is very large as compared to the dynamic adders.

Existing Full Adder Module

The proposed circuit of full adder is represented by three modules as shown in Fig.1 Module 1 and Module 2 are the XNOR modules. These two modules are responsible for generating the SUM(sum signal) and Module 3 generates the Cout(output carry signal). Each and every module is designed in such a way that whole circuit of adder works in an optimized manner. The delay, power and the area results are always in the favor.

Each module is discussed in details below:

A) XNOR Block

In our proposed circuit of full adder, the function of the XNOR module is to consume the power required for the operation of entire circuit. Thus this block is designed in such a way that power is being consumed in the most optimized way and of course without the degradation of the voltage. Presented below is the Fig.2 which clearly shows the modified version of the XNOR circuit. This circuit consumes reduced power with the help of the use of weak inverter. In these inverters the channel width of the transistors tends to be small. The transistors here are Mp and Mn1 [1].

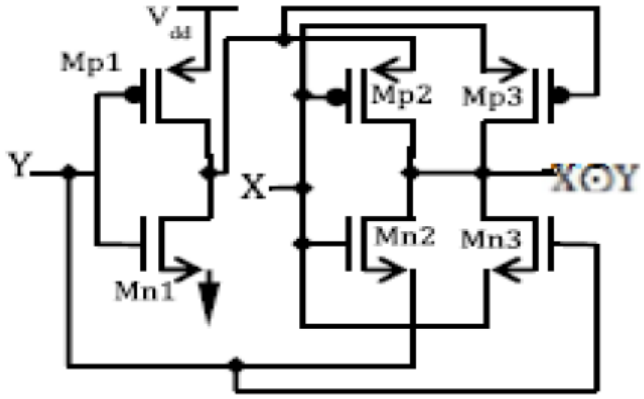

Fig.2: XNOR block

In our design, the XNOR block has employed 6 transistors but the arrangement of the transistors is done in a different manner. This XNOR offers very low power and in return high speed when compared with the conventional 6T XOR-XNOR implementation

B) Carry Generation Block

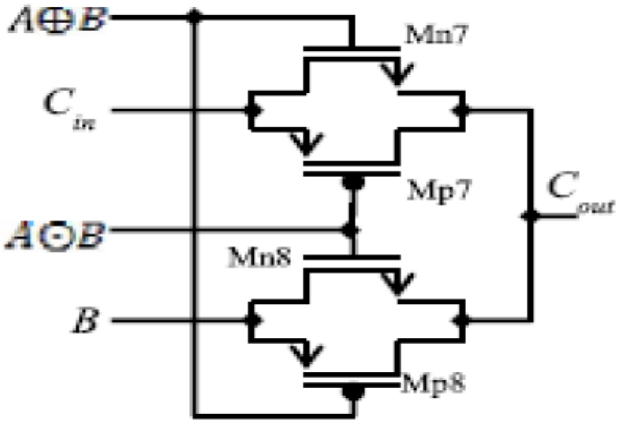

Fig.3: Carry Generation Block

In the existing circuit, the transistors Mn8, Mp8, Mp7, and Mn7 are used for the output carry signal. There is a single transmission gate Mp7 and the Mn7 through which the input carry signal i.e. the Cin propagates out. This way the complete carry propagation path is reduced significantly. Then, the stronger transmission gates being used which are having larger width of the channel are used to further reduce the delay in the propagation of the carry signal. These transistors are Mn7, Mp7, Mn8, and Mp8.

III. CONCLUSION

We have discussed various logical techniques of full adder and parameters like power delay and power delay product for its improved performance further work can be done on reducing power consumption and delay for high speed so it can be more efficient to work on various applications.

IV. REFERENCES

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