LOW POWER AND LOW PDP TERNARY ADDER DESIGN BASED ON CNTFET TECHNOLOGY

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Abstract: Electronic devices portability requires major low power requirements and also high-speed requirements so there is high necessity for improving the circuits. Ternary logic these days is in high demand as most special algorithms such as fuzzy logic works on ternary logic so there is necessity of improving the performance of the ternary adder. In this thesis, we have proposed a new approach for Ternary Adder, in which tri-mode technique is used to improve the performance of the circuit and compared with a sleep transistor-based technique and the simple ternary adder(TA). With this improvement it is seen that the proposed circuits give better performance in terms of Average Power, Delay, PDP and EDP. So, tri-mode technique and sleep mode technique have higher advantages in terms of performance metrics calculated. CNTFET has a high performance in terms of performances and is a better substitute for MOSFET in 32nm technology.

Keywords- *Ternary Adder, HSPICE, CNTFET, Power Gating*

I. INTRODUCTION

The scaling of current CMOS technology to nanoscale range causes various critical challenges and reliability issues such as direct electron tunnelling through short channels and thin insulator films, variations in device structure and doping, larger process variations, reduced gate control and high leakage current etc. As indicated by Moore's law the elements of individual devices in a coordinated circuit have been diminished by a factor of around two at regular intervals. This downsizing of devices has been the main impetus in innovative advances since the late twentieth century. In any case, as substantiated by ITRS 2009 release, further downsizing has confronted genuine limits identified with manufacture innovation and device exhibitions as the basic measurement contracted down to sub-22 nm range. The points of confinement include electron burrowing through short channels and slight protector films, the related leakage currents, aloof power dissipation, short channel effects, and varieties in device structure and doping. These breaking points can be defeated to some degree and encourage further downsizing of device measurements by altering the channel material in the conventional mass MOSFET structure with a solitary carbon nanotube or a variety of carbon nanotubes. Electronic device, innovation and circuit specialists are investigating conceivable options for the fate of semiconductor industry to improve execution of electronic framework. Research is being completed in growing high-portability transistor channel materials, for example, compound semiconductors, stressing the channel material to improve bearer versatility just as in utilizing nonplanar transistor structures in particular CNTFETs and multigate structures.

II. IMPLEMENTATION

In this section, we propose to types of ternary adders in tri-mode and sleep mode techniques.

Waveform of CNTFET based Ternary Adder:

In Figure 1 Ternary Adder waveform is given for CNTFET based Ternary Adder in 32nm technology.

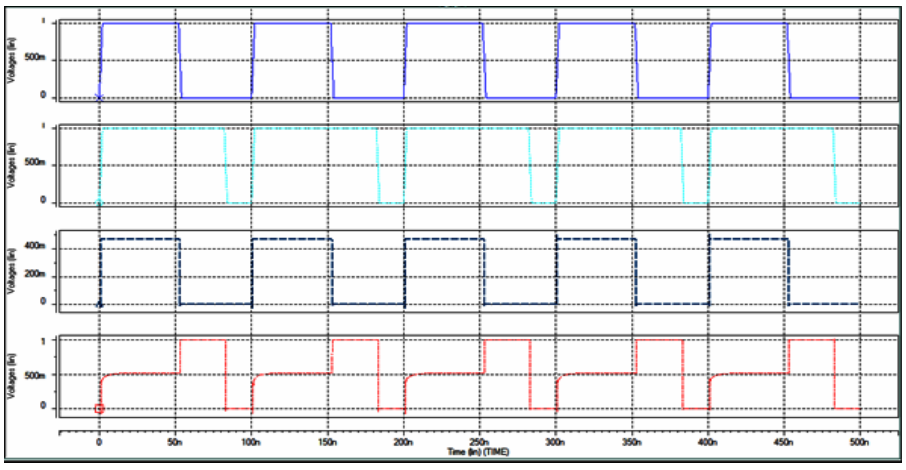

Figure 1: Waveform of CNTFET based Ternary Adder

Proposed Tri mode Ternary Half Adder(THA) using CNTFET:

In figure 2, the circuit for ternary half adder using tri mode technique is presented. In this circuit, in the ground network, two transistors are added as seen in the figure. And the gate of two transistors is connected to sleep and hold signals. Hence, its requirement is to save power with keeping it up to output expectations even when the circuit is in sleep mode. Another signal here is hold. Sleep and hold controls when the circuit is in sleep mode or hold mode.

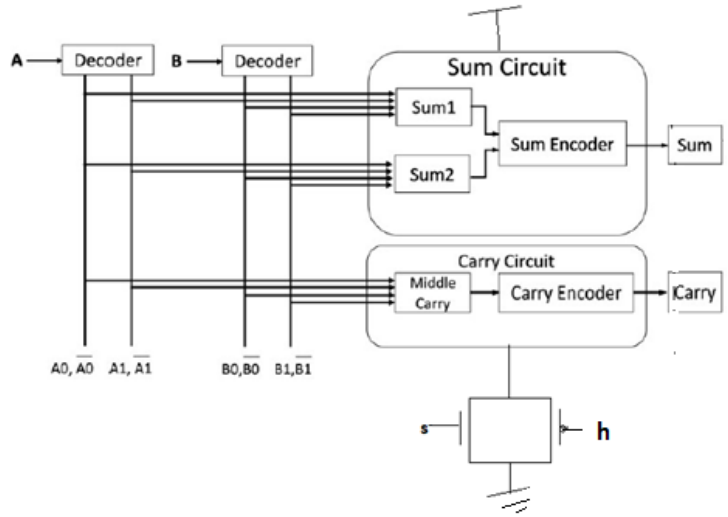

Figure 2: Proposed TMTHA using CNTFET

Proposed Sleep Transistor Ternary Half Adder using CNTFET:

This technique is shown in Figure 3. it has two transistors when connected to Vdd and other NCNTFET to ground. The signal sleep and sleep bar control the outputs of the circuit.

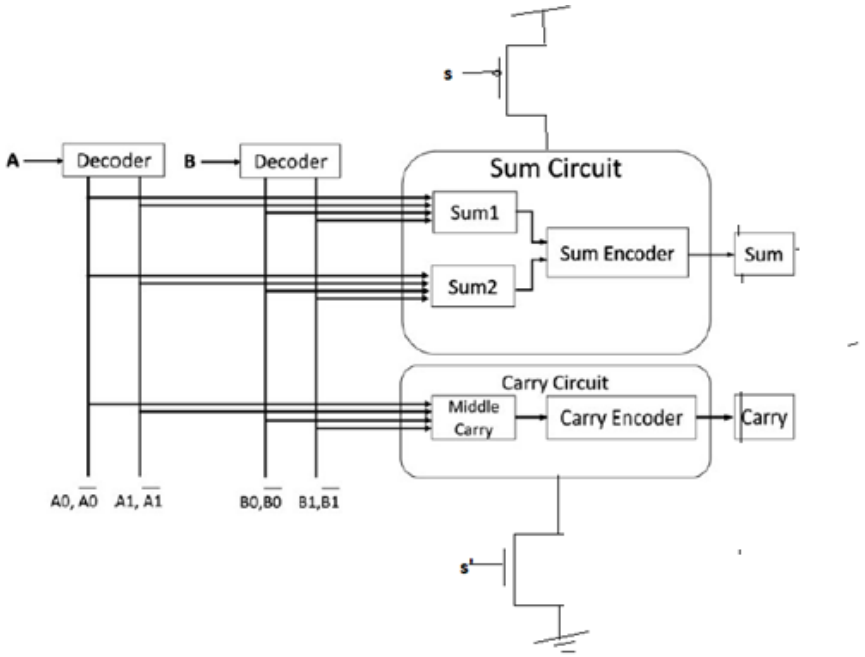

Figure 3: Sleepy Ternary Adder Technique

Simulation Results for Proposed Circuits with Ternary Adder:

Table 1: Simulation output parameters

	Ternary Adder	Tri Mode	Sleep Mode
Average Power	3.27E-05	1.09E-05	4.01E-06
Delay	3.00E-08	3.04E-08	3.02E-08
PDP	9.83E-13	3.33E-13	1.21E-13
EDP	2.95E-20	1.01E-20	3.66E-21

In figure 4 to figure 7 charts for Average Power, Delay, PDP and EDP are shown.

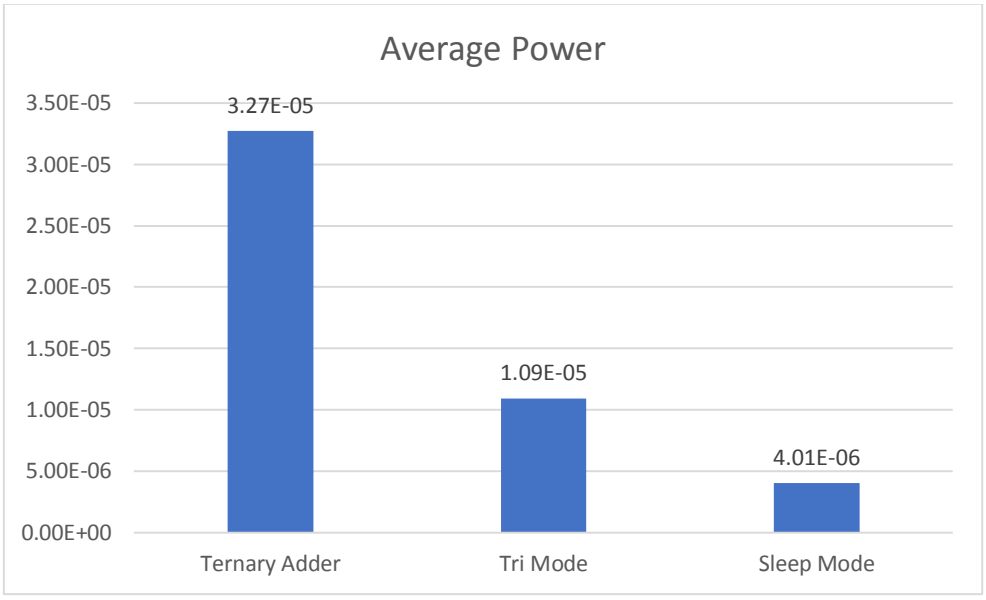

Figure 4: Average Power for Tri-mode, Sleep Mode and Base TA

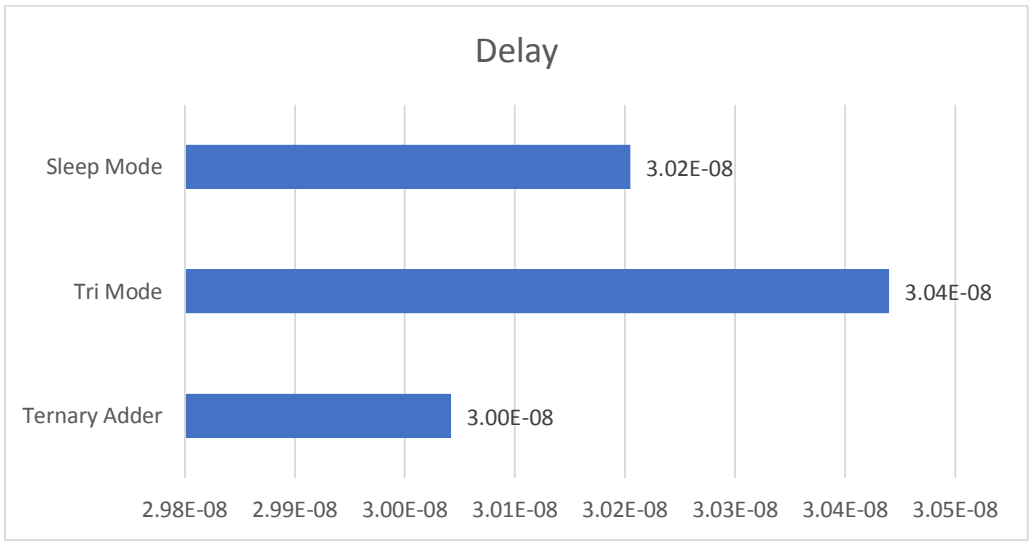

Figure 5: Delay for Tri-mode, Sleep Mode and Base TA

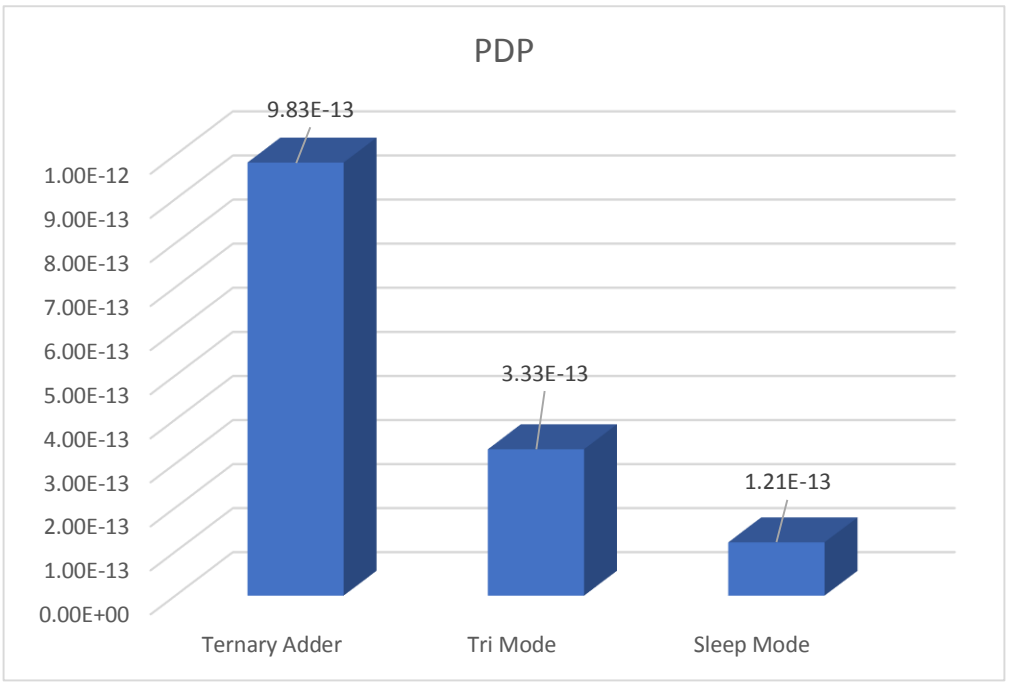

Figure 6: PDP for Tri-mode, Sleep Mode and Base TA

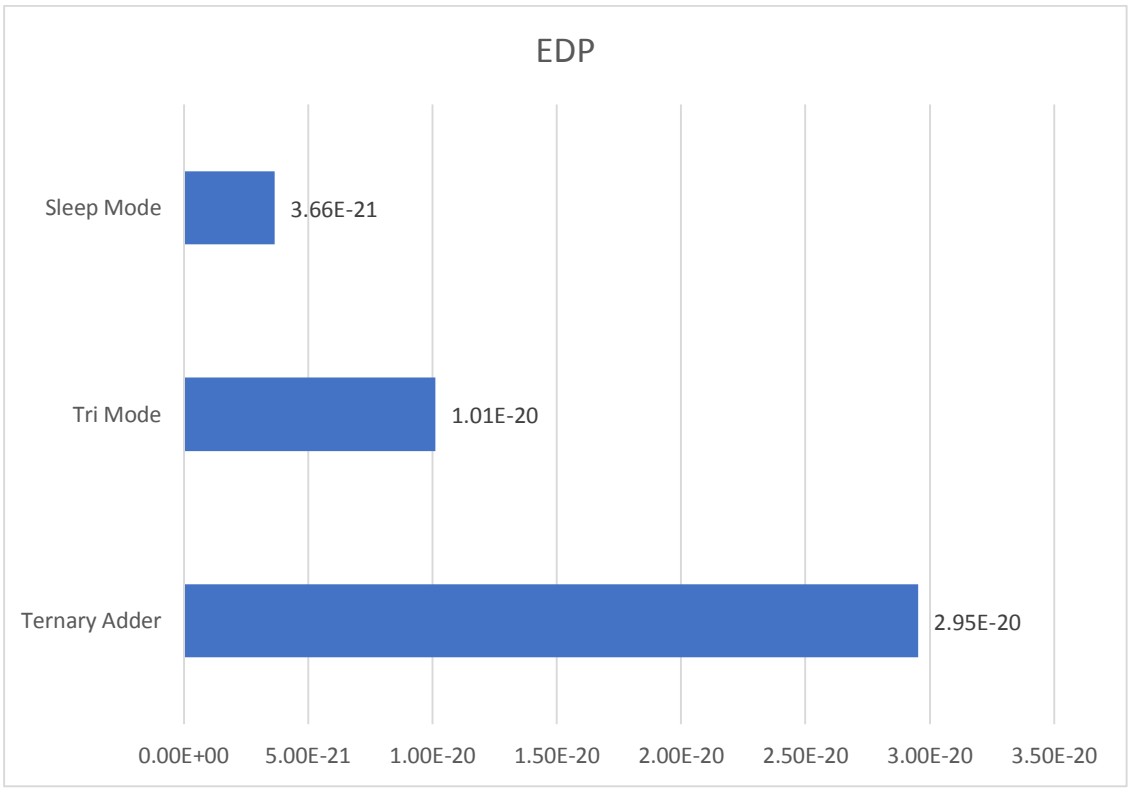

Figure 7: EDP for Tri-mode, Sleep Mode and Base TA

Waveform of Tri mode THA and Sleep THA:

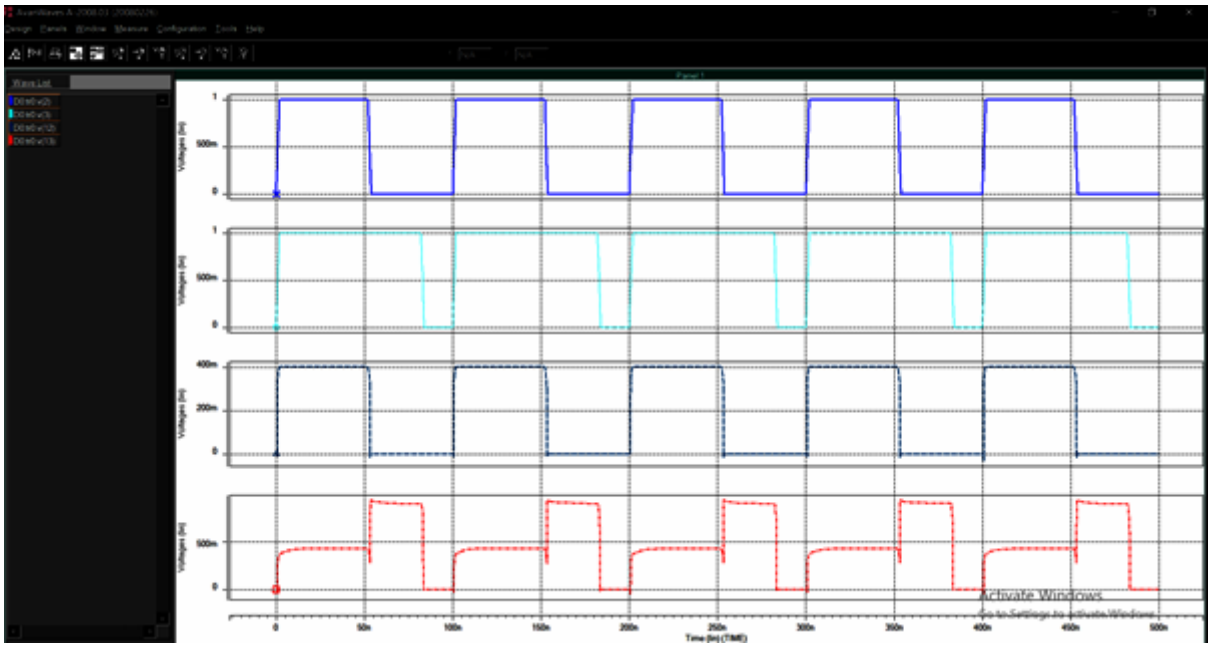

Figure 8: Tri mode THA waveform

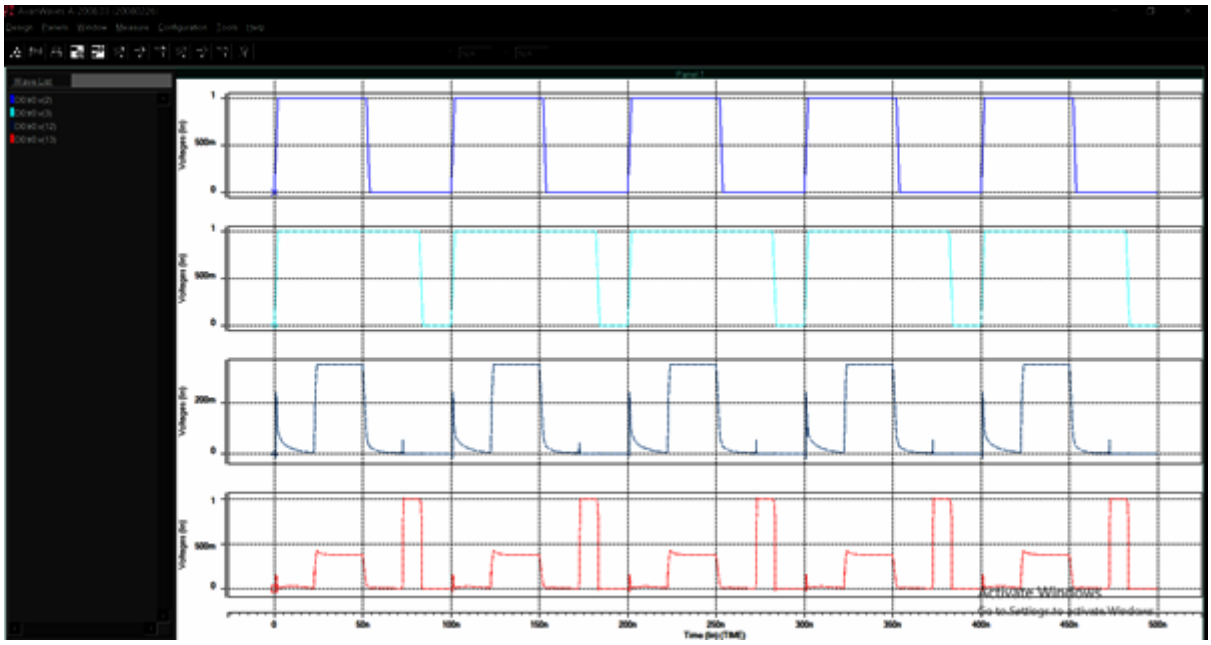

Figure 9: Sleep THA waveform

In figure 8 and figure 9, waveform is represented for Tri mode proposed work and for Sleep based Ternary Half Adder.

III. CONCLUSION

Hence, we conclude in this section, that tri-mode and sleep techniques work well with ternary adder circuit. The Average Power is improved by 66.6% in tri-mode and 88.7% in sleep mode, delay is nearly same in all circuits, PDP is improved by 66.1% in tri-mode and 87.6% in sleep mode. Also, energy is improved by 65.7% in tri-mode and 87.5% in sleep mode technique. Hence both the new techniques are performing good. Also, tri-mode is generally used for low noise applications.

IV. REFERENCE

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