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Research Article

Reduction of Process Variation in Sub-threshold Logic Circuit using Adaptive Feedback Equalization

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Abstract

Low energy or low powers are the primary constraint in the design of digital VLSI circuits in recent years. Minimum energy consumption can be achieved in digital circuits by operating it in the sub-threshold region. However this regime can only be achieved by proper body-biasing and transistor upsizing. Slow speed is the main drawback which can have a detrimental impact on the functionality of the circuits operating under low supply voltage. This becomes more frequent in scaled technology node where process variations are highly prevalent. Therefore mechanism to mitigate these timing errors in circuits is required. The proposal in this paper is to use variable threshold feedback equalizer circuit with combinational logic block to mitigate the timing constraint which can then be leveraged to reduce the propagation delay. As the part of analysis, a conventional D flip-flop is compared with a proposed equalized flip-flop using tanner EDA. The power and delay analysis of this feedback circuit is done using Xilinx software.

Keywords: Feedback equalizer; Leakage energy component; Propagation delay; Sub-threshold.

Introduction

The use of sub-threshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduce the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below the threshold voltage of the transistors for digital logic circuits [1].

However, digital logic circuits operating in the sub-threshold region suffer from process variations that directly affect the threshold voltage (*VT*). This in turn has a significant impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the sub-threshold regime. Moreover, sub-threshold digital circuits suffer from the degraded *I*ON/*I*OFF ratios resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded *I*ON/*I*OFF ratios [2] and process-related variations make sub-threshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of *VT* varies inversely with the square root of the channel area [3], one approach to overcome the process variation is to upsize the transistors [2].

Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates [4] to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption. In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the sub-threshold region while achieving robustness equivalent to that provided by [2]. Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the

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output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy.

In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the sub-threshold digital logic. In general, our approach of using feedback equalizer to lower energy consumption and improve robustness is independent of the methodology used for designing a combinational logic block operating in the sub-threshold regime. We propose using an adaptive feedback equalizer circuit in the design of tunable sub-threshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the sub-threshold digital logic circuits.

The major constraint in the design of a VLSI circuit is low energy or low power. The performance of a circuit in terms of power and speed are of particular interest. As the technology gets scaled down, it affects the voltage being supplied and size of the transistor used [2]. And supply voltage is scaling down in such a way that the circuit is forced to work in sub threshold regime [3]. Sub-threshold conduction occurs for gate to source voltages (Vgs) below the threshold voltage (Vth).

Fig. 1 shows the schematic of an inverter in 180 nm. Supply voltage is scaled down from 1.8 V to 500 mV. Upto 600 mV perfect inverted output was obtained. But for 500 mV supply, that was not the result. In order to obtain perfect operation as an inverter, it required various techniques viz., body biasing [6] and upsizing the transistor. Standard configuration has the bulk of the NMOS tied to the ground terminal, while that of the PMOS is tied to the power supply (VDD) for an inverter. If the bulk terminal [7] of the NMOS device is raised above ground and the power supply voltage is below the threshold, there is increase of the drain current (ID).Lowering the bulk voltage of pmos device leads to increased ID. In this case transistor Vgs is found out to be less than it's Vth which is the threshold voltage. And thus circuit operates in sub-threshold region [1].

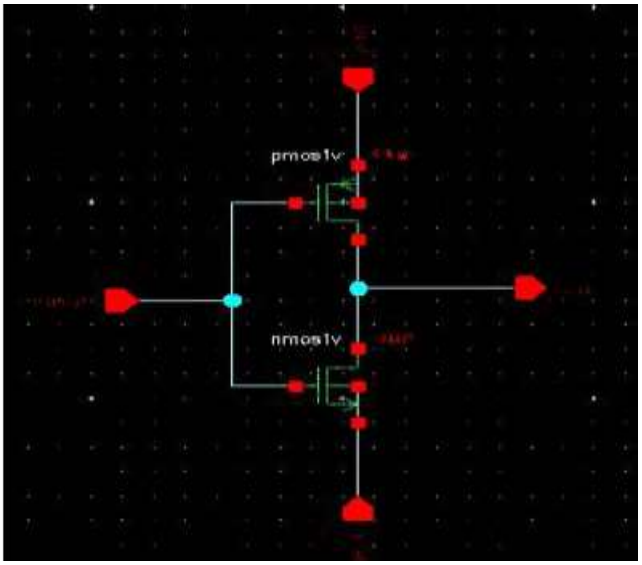

Fig. 1. Schematic of an Inverter

In all these cases, the dynamic power and propagation delay [9] were found out. From Table 1, we can observe that as voltage gets scaled down [3], the power is reducing, as dynamic power is proportional to the square of supply voltage. But propagation delay is increasing when voltage scales down. So in order to operate my device in scaled [8] technology nodes the main problem is higher propagation delay or slow speed [4].This paper mainly deals with a feedback equalization circuit using variable threshold inverter to improve speed than non-equalized one.

Table 1. Voltage Scaling Effects

VDD	Power (Mw)	Delay (ns)	Wp:Wn	Body-bias
1.8 V	46.4	9.865	2:1	NO
900 mV	0.5	10.027	2:1	NO
600 mV	0.267	10.264	2:1	NO
500 mV	0.204	11.581	5:1	YES

Research methodology

Variable Threshold Inverter

Variable threshold inverter [12] is a circuit that adjusts the switching thresholds and mitigates timing errors. The VTI [10] circuit shown in Fig. 2 is analyzed in 180 nm process. Switching threshold voltage is found out to be greater than or less than nominal threshold voltage. Table 2 shows the values obtained for

various values of P and N control signals. Variable threshold inverter fastens the transition from low-to high and high-to-low. The threshold voltage of the inverter is controlled by using signals P and N. When P is grounded and N is connected to VDD, the threshold voltage is V th0, which is the nominal threshold voltage of the inverter. When both P and N are grounded, the pull down path is off and the threshold voltage increases to Vth+. Similarly, when both P and N are connected to VDD, the pull up path is off and threshold voltage decreases to Vth-. A weak inverter is required in this case, to ensure that the output of the inverter is never floating.

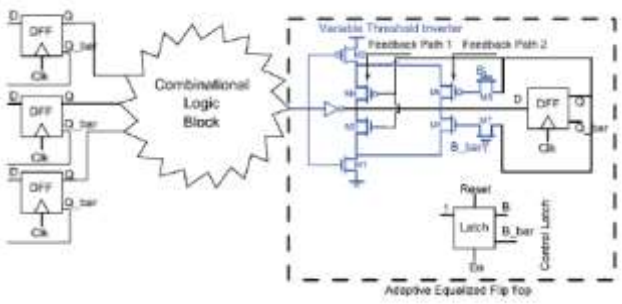

Fig. 2. Adaptive feedback equalizer circuit with multiple feedback paths (designed using a variable threshold inverter can be combined with a traditional master–slave flip-flop to design an adaptive E-flip-flop)

Table 2. Switching Threshold of VTI

P	N	VM (Mv)	Vth
VDD	VDD	734.198	Vth-
GND	VDD	826.047	Vth0
GND	GND	938.476	Vth+

Conventional D Flip-Flop

The working of D flip flop is similar to the D latch with one exception. The exception is that the output of D Flip Flop (D-FF) takes the state of the D input at the moment of a positive edge at the clock and delays it by exactly one clock cycle. That's why, it is commonly known as delay flip flop. D-FF can be interpreted as a delay line or zero order hold. The advantage of the D-FF over the D type "transparent latch" is that the signal on the D input pin is captured the moment the flip flop is clocked, and subsequent changes on the D input will be ignored until the next clock event.

Transmission gates are used in the construction of Master Slave flip flop shown in Fig. 3. Transmission gate is constructed using PMOS and NMOS which are actually tiled face to face. The Master Slave (MS) flip flop consists of cascading a master stage with a slave stage. When clock is low, the master stage is transparent and the D input is passed to the master stage output, QM and the slave stage is in the hold mode, which keeps its previous value using feedback circuit.

On the rising edge of the clock, the slave stage starts sampling whereas master slave stops sampling. During high phase of the clock, the master stage remains in hold mode, while the slave stage samples the output of the master stage (QM). Since QM is constant during the high phase of the clock, Q makes only one transition per cycle. The value of Q is the value of D right before the rising edge of the clock, achieving the positive edge-triggered effect. A negative edge triggered register can be constructed with same principle as that of a positive edge-triggered flip flop, but by switching the order of the positive and negative latch (i.e., by placing the positive latch first).

Proposed Equalized Flip-Flop

The proposal is to use a feedback equalizer circuit in the design of logic circuits operating in lower supply voltages. This feedback equalizer circuit takes the advantage of fast charging/ discharging of the load capacitance in the critical path, which creates opportunities for voltage scaling. The use of the feedback equalizer circuit in the design of an equalized flip flop and then provide a detailed comparison of the equalized flip flop with a conventional flip flop in terms of area, power and performance.

We propose the application of a feedback equalizer (designed using a variable threshold inverter) along with the classic master-slave positive edge triggered flip flop to implement an equalized flip flop. The equalized flip flop dynamically modifies the switching threshold of the gate before the flip flop based on the previous sampled data. If the previous output of the gate is a zero, the equalized flip flop lowers down the switching threshold which speeds up the transition to one. Similarly, if the previous output is one, the equalized flip flop increases the switching threshold which speeds up the transition to zero. In this configuration, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions. The switching of the variable threshold inverter is dynamically adjusted based on the previous sampled output data.

Adaptive Equalized Flip-Flop versus Conventional Flip-Flop

In this section, we first explain the use of the adaptive feedback equalizer circuit in the design of an adaptive equalized flip-flop (E-flip-flop) and then provide a detailed comparison of the E-flip-flop with the conventional flip-flop in terms of area, setup time, and performance. We propose the use of a variable threshold inverter as an adaptive feedback equalizer along with the classic master–slave positive edge-triggered flip-flop design an adaptive E-flip-flop.

This adaptive feedback equalizer circuit consists of two feed forward transistors (M1 and M2 in Fig. 3) and four control transistors (M3 and M4 for feedback path 1 that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON post-fabrication in Fig. 3) that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip- Flop input capacitance. The extra pull-up/pull-down paths are enabled whenever the output of the critical path in the combinational logic changes. The control transistors M5 and M6 are enabled/ disabled through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip bootup. After bootup, if required a square pulse is sent to the En terminal to set the output of the latch to 1 to switch ON M7 and M8, which enables feedback path 2.

The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of flip-flop in the previous cycle. If the previous output of the flip-flop is a 0, the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1. Similarly if the previous output is 1, the switching threshold is increased, which speeds up the transition to 0. Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic. The dc response of the adaptive feedback equalizer circuit with two different feedback paths in the sub-threshold regime is shown in Fig. 3.

The adaptive E-flip-flop has eight more transistors than the conventional master–slave flip-flop. Compared with a classic master–slave flip-flop with 22 transistors, the area overhead of the adaptive E-flip-flop is 36% and control latch with ten transistors (three inverters and two TGs) is 45%. This area overhead gets amortized across the entire sequential logic block. The total energy consumed by a digital circuit in the sub-threshold regime can be calculated using eq. 1.

$$ET = E\text{DYN} + EL = C\text{eff}V\,2\text{DD} + I\text{leak}V\text{DD}TD \quad \ldots\ldots(1)$$

In (1), EDYN and EL are the dynamic and leakage energy components, respectively. Ceff is the total capacitance of the entire circuit, VDD is the supply voltage, and $TD = 1/f$ is the total delay along the path of the digital logic block. Feedback equalization enables us to reduce the delay of the path in the digital logic block, which in turn reduces the leakage energy. In (1), Ileak is the leakage current and can be written as eq. 2.

$$I\text{leak} = \mu 0C\text{ox}WL(n-1)V2\ \text{th}e^{\eta V\text{DS}-VT\ nV\text{th}} \quad \ldots..(2)$$

In (2), VT is the transistor threshold voltage, Vth is the thermal voltage, n is the sub-threshold slope factor, and η is the DIBL coefficient. There is an exponential relationship between the leakage current and the supply voltage (due to the DIBL effect and because $V\text{DS} \approx V\text{DD}$). Using the E-flip-flop, we can scale down the supply voltage while maintaining the zero-error rate at a given operating frequency and achieve lower dynamic energy consumption (due to the quadratic relationship between the dynamic energy and the supply voltage) as well as lower leakage energy (due to smaller DIBL effect that exponentially decreases the leakage current).

Similar to the area overhead, the dynamic energy as well as the leakage energy overhead of the variable threshold inverter gets amortized across the entire sequential logic block. The setup time of the conventional master–slave positive edge-triggered flip-flop is $ts{-}t = 3t\text{inv} + t\text{TG}$. Since the adaptive E-flip-flop uses an extra variable-threshold inverter at its input, the setup time of the adaptive E-flip-flop will be larger $ts{-}t{-}\text{equ} \approx 4t\text{inv} + t\text{TG}$. The clk-to-$q$ delay of the conventional flip-flop is $tc{-}q = t\text{inv} + t\text{TG}$. Since the E-flip-flop has the variable threshold inverter as extra load at the output, the $tc{-}q$ delay of the

E-flip-flop is *tc−q*−equ = *t*inv+*t*TG +_*tc−q*, which is slightly larger than the *tc−q* delay of the conventional flip-flop. Here, _*tc−q* is the increase in inverter delay due to the extra load of the adaptive feedback equalizer circuit. However, the adaptive feedback equalizer circuit can significantly lower down the propagation delay of the critical path because the small input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic.

The hold time of the classic master–slave positive edge-triggered flip-flop is zero. Therefore, the adaptive feedback equalizer circuit does not impact the hold time violations. Table I compares the propagation delay, setup time, and the *tc−q* delay of the two 8- bit adders designed with the conventional flip-flop and E-flipflop in XIlinx software. Where *t*cdFF is the minimum propagation delay of the flip-flop and *t*cdlogic is the minimum propagation delay of logic.The hold time of the E-flip-flop is zero.

So, the hold time constraint is also fulfilled, which insures the stability of feedback equalizer circuit in the subthreshold regime.

$$t\text{hold} < t\text{cdFF} + t\text{cdlogic} \quad \ldots..3$$

To avoid the metastability problem in the E-flip-flop, both the setup time and hold time constraints should be satisfied.

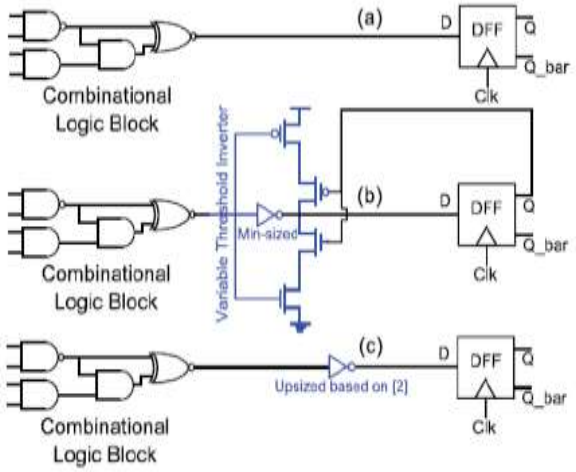

Fig. 3. Block diagrams of (a) original nonequalized design, (b) equalized design with onefeedback path ON, (c) buffer-inserted nonequalized design

Results and discussion

The analyses of equalized flip flop and non-equalized flip flop in 180 nm process are compared. For the same combinational logic output, which is here taken as a pulse input both the circuits exhibits different results. On an average, the equalization technique has 10.97% lower propagation delay than the non-equalized logic design. But the power dissipation of an equalized circuit is 5.06% more than that of its non-equalized version. This extra power is caused by the extra circuitry used for feedback equalization. Power delay product of an equalized circuit is 7.81% less than non-equalized one.

We compare different techniques proposed with our adaptive feedback equalizer circuit to mitigate process variations in digital sub-threshold logic circuits. Feedback equalization complements these existing techniques and can be used along with these techniques for the sub-threshold circuit design. The upsizing design methodology proposed increases the device parasitics, which in turn increases the dynamic and leakage energy components of the entire digital sub-threshold logic block.

For the 8-bit adder, the proposed feedback equalization technique has 10.8% lower total energy and 8.9% lower delay variation compared with the upsizing methodology proposed. Increasing the logic path depth requires inserting of additional buffers in the critical path of the sub-threshold design to reduce the normalized (σ/μ) The proposed adaptive feedback equalization technique reduces the normalized delay variation by 8.9% with 0.56% area overhead in the entire 8-bit adder.

The proposed adaptive feedback equalizer circuit has simple topology, negligible area, and energy overhead and the capability to reduce the normalized delay variations post fabrication. Here the circuit operated in three mode (i) Non equalized adder,(ii) buffer inserted adder and (iii)equalized adder circuit as mode 01, mode 10 and mode 11 respectively and its corresponding output are shown in fig. 6, 7 and 8.

Delay comparison of equalized adder along with control latch. The resulted analysis shows the equalized adder with control latch having minimum delay when compared to equalized adder. The comparisons are shown in table 3 and 4. Power analysis of equalized adder and non-equalized adder are compared. Comparing to non-equalized, the equalized circuit take more power because of large circuitry, but performance of equalized circuit is high.

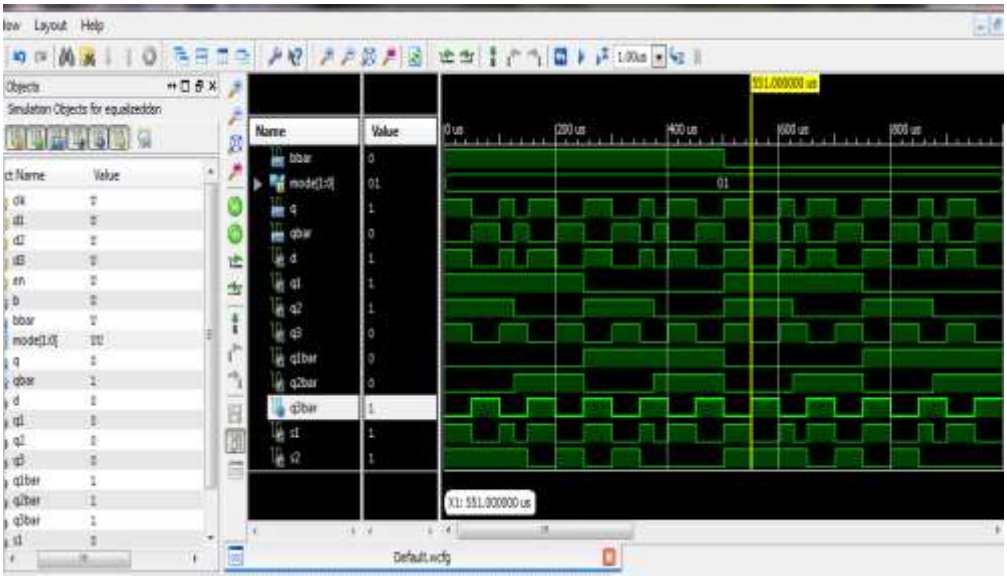

Fig. 6. Non equalized adder output

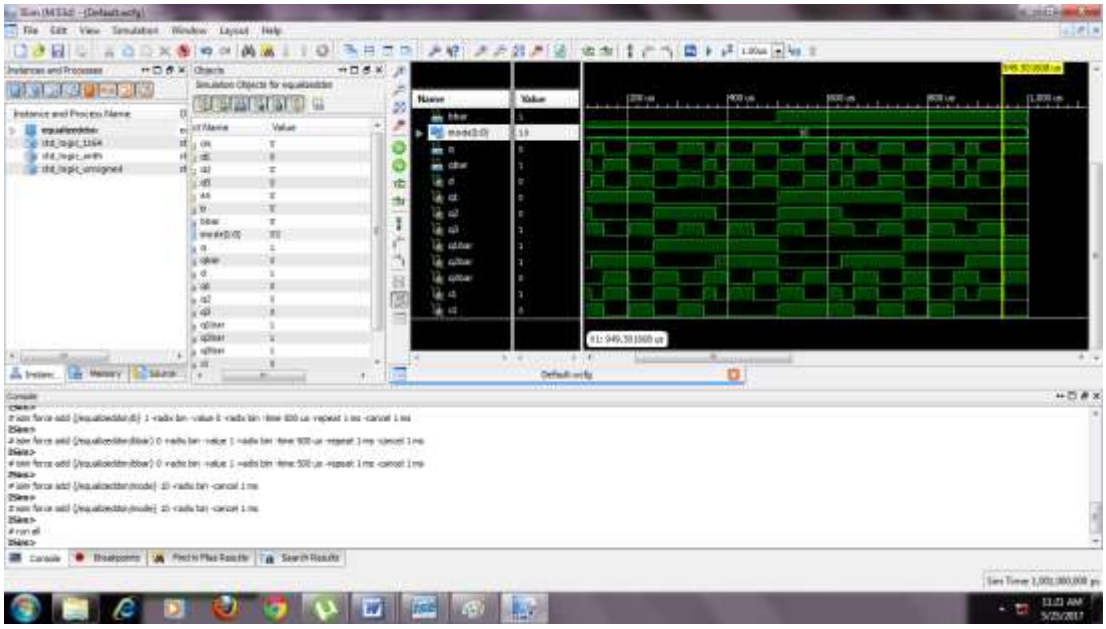

Fig. 7. Buffer inserted adder output

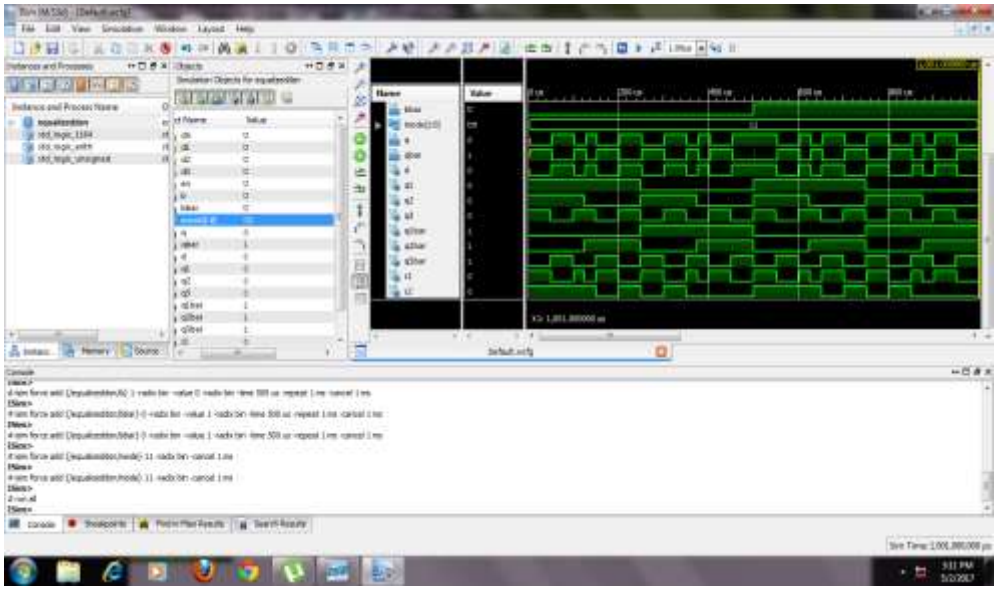

Fig. 8. Equalized adder output

Table 3. Delay comparison of adder circuit

Design	Delay ns
Equalized circuit	0.04
Equalized circuit with control latch	0.16

Table 4. Power comparison of adder circuit

Design	Power Watt
Equalized circuit	0.00047
Non equalized circuit	0.00046

Conclusions

The analyses done on the conventional D flip-flop and Equalized flip-flop and compared. It is found that there is a noticeable decrement in the propagation delay of the equalized flip-flop than its non-equalized version. The power of equalized flip-flop is more than that of non-equalized flip-flop. This is due to the fact that feedback equalization circuits consist of a variable threshold inverter is having an area overhead. We proposed the application of a tunable adaptive feedback equalizer circuit to reduce the normalized variation of total delay along the critical path and the dominant leakage energy of the digital CMOS logic operating in the sub-threshold regime. Adjusting the switching thresholds of the gates before the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage energy of digital logic in weak inversion region.

Conflicts of Interest

Authors declare no conflict of interest.

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