# Design and Performance analysis of CMOS based D Flip-Flop using Low power Techniques

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***Abstract*—** In today's world, the VLSI designer totally dependent on Flip-flops as it has wide range of applications in various field of electronics. Flip-flops are widely used in spacecraft for numerous processes; these are also used in telecommunication sector for exchange the information and storage the data [1]. The functionality of the integrated circuit is controlled by the using flip-flops [2]. In VLSI Technology, the high-performance parameters like power dissipation, leakage, area, speed have the significant appearance in designing clock storage element, these elements are used in portable devices (for example batteries, microprocessors etc). To brought down power consumption in these devices upgrades battery. The size of chips is major problem in digital integrated circuit because millions of transistors consume more energy. For reducing the size of chips in integrated circuit, scale down the VLSI Technology (180nm, 90nm, 45nm, etc) [3]. A lot of problems are associated with the using of these transistors among which power dissipation is one of the vital design concern. More power consumption decrease more current from the power supply and temperature of devices is raised as heat dissipated is directly proportional to the temperature. So more complicated techniques for cooling and packaging of devices is required for better circuit operation and reliability. Many low power techniques is used in this paper to reduce these problems. In term of power consumption, MTCMOS based D flip-flop is reduced by 8.2 %, power gating-based D flip-flop is decreased by 7.42% while more reduction in SVL based D flip-flop is brought down by 10% as compared to conventional CMOS based D flip-flop at 45nm technology.

***Keywords*—***Flip-Flop, CMOS, MTCMOS, Power Gating, SVL, Power Dissipation, Delay, Power Delay Product, Leakage Current, Layouts*.

## I. INTRODUCTION

The current trends in the enlargements and improvements in the domain of low power VLSI design does examined in this paper. This paper focuses to expand on the modern aims in the low power design. Multi-threshold CMOS is an efficient standby leakage control low power method. Multi-threshold logic makes use of low $V_{th}$ and high $V_{th}$ MOS transistors to satisfy both low power and high-performance requirements. Minimizing supply voltages devoid compromise of speed are mainly useful mode to diminish power consumption. To achieve this aim, numerous low voltage circuits with low-threshold MOSFET's, power gating and SVL has been proposed. High performance D Flip Flop design using standard CMOS logic gates is proposed at 45nm Technology. In this paper, proposed D flip-flop design is negative edge-triggered D flip-flop. Power is one of the main resources; hence the designers are attempting to reduce it while designing a system. The crucial challenge in portable electronics devices is brought down their power dissipation. Variation of the process parameters due to rapid scaling of technology arise many issues in yield, reliability and testing. Usually it is considered that with every 10°C rise in temperature the failure rate of a VLSI chip doubles. Heavy power dissipation proceeds to the increased cost of cooling and packaging. This paper is used different low power techniques to reduce leakage current and increase the performance.

### *A. CMOS Technique*

CMOS is called as "Complementary Metal Oxide Semiconductor" [4]. CMOS technique is one of the most well-known technique in the computer chip design industry and widely used today to compose integrated circuits in several miscellaneous applications. CMOS technology uses of both PMOS and NMOS transistors i.e. pull up and pull-down network that's why it is called as complementary Metal Oxide Semiconductor. CMOS is quite suitable technique for various components such as microprocessors, microcontrollers, and memories- RAM, ROM and ASICs. A Complementary MOS circuits has negligible static power dissipation like NMOS or BIPOLAR circuits.

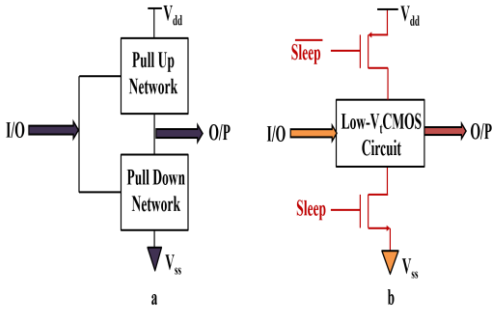


Fig.1: a) CMOS b) MTCMOS basic Circuit

Most of the time, power is exhausted when switching takes place in the circuit. More number of gates can be integrated on an IC by CMOS technology than NMOS or bipolar technology,

so lowering the power consumption. Power consumption is a critical concern in the VLSI circuits due to regular decrease in feature size of CMOS circuits and a subsequent increase in chip density and operating frequency.

### B. *MTCMOS Technique*

MTCMOS is called as "Multi-threshold Complementary Metal Oxide Semiconductor" [4]. Scaling the supply voltage is an effective way to handle power dissipation. MTCMOS is a robust circuit-level technique which gives high-performance and low-power consumption by using sleep transistors as shown in Fig.1. Basically, these low-power techniques help in maintaining the circuit performance while reducing the sub-threshold currents in standby mode. Power management is unavoidable especially as technology scales down, so low-power techniques must be devised to reduce power dissipation and accurately estimate the power consumption [5-6]. Normally, there are three sources of power dissipation in digital CMOS circuits, first is switching activities i.e. signal transition, second comes from short circuit current and the last is due to leakage currents. Besides, leakage power is also the critical concern. As high leakage current is also transformed into an important contributor to power dissipation of CMOS circuits. Basically, MTCMOS is the low power technique i.e. is used to minimize power consumption. To reduce the power dissipation in CMOS circuit, numerous sources must be identified. Standby currents, an important cause of power dissipation can be reduced by using CMOS and MTCMOS technique. It can be used to improve speed at low supply voltage and low power consumption. More power consumption in VLSI circuits requires more costly packaging and cooling technologies that enhance the cost and decrease system reliability. This is one of the main reasons for low power cell design. The most important reason for low power research and design is our convergence to a mobile society for that we require long battery life and this can be done by using low power cells.

### C. *Power gating technique*

Transistor based power gating is a technique used to reduce power consumption in integrated circuit. This technique uses the sleep transistors which work as a headers and footers is shown in fig 2. In this technique when numerous power areas or an independent modifiable voltage regulator is used, Headers find their applications in most commercial designs as they are easy to design and analyze. On the other hand, less number of footers is needed due to their high n-type mobility, thus making them more area efficient. Leakage problem in header is slightly reduced during standby mode. The width of the headers act as controlling factors, which is responsible for leakage reduction and increasing delay on power network.

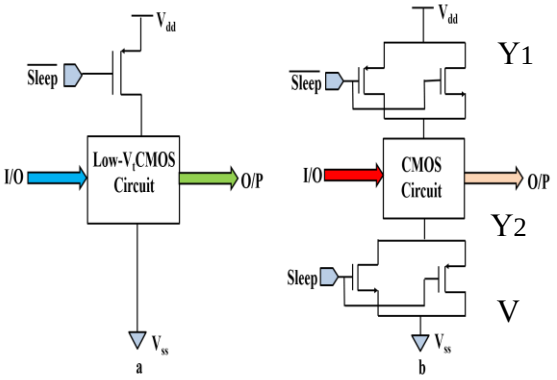


Fig.2: a) Power gating b) SVL Basic Circuit

Due to large variations in the size of header, the leakage power during active mode is reduced but not increased during large ideal mode remaining leakage power encourages energy consumption. The additional capability of power getting technique is to enable $I_{ddq}$ testing which enhances the testing speed in CMOS circuits. The selected ideal period can be controlled by Temporal Granularity and the number of distinct power gating regions is controlled by Regional Granularity. The most granular approach can be achieved by an independent modifiable regulator. On chip leakage will be completely removed by switching off the voltage regulator. But it achieves high granularity in both ways. First, the distinct power supply pins will be required by every power gated area. Second, the high capacitance of switched power network would consume considerable amount of energy and time to energize. As compared to coarse-grained approach, the fine-grained approach is achieved by advanced low-power microprocessors.

### D. *Self-controllable voltage technique*

Most common application of low power techniques now a-days in telecommunication i.e. in mobile phones, it has a logic circuit (multiplier and adder) and storage circuit (flip-flop, memories) which needed the low power techniques. Many low power techniques were proposed out of which MTCMOS technique is one of them. In this technique, it reduce the leakage current, standby power $P_{st}$ by using the PMOS and NMOS with high threshold voltages ($V_{thp}$,$V_{thn}$). But due to certain limitations, it is not able to maintain the output of the digital circuits. To overwhelm this pitfall, Self-Controllable voltage technique is one of the most effective techniques in all low power techniques to reduce the leakage current, standby power and maintain the high-speed performance. In this technique, PUN and PDN are connected with basic structure. The connection of PUN and PDN are shown in Fig. 2. The differences between PUN and PDN are that it places the transistors opposite site to the other network. By using this technique, it reduces the sufficient amount of leakage current, PDP and average power.

This technique is most useful technique in digital electronics and telecommunication sector as it gives high performance of the digital design. The aim of this technique in this thesis is to reduce the leakage current during the standby mode and average power during the active mode in clocked system like flip-flops. By controlling the clock signal, this technique maintains the performance of clocked system [7].

## II. DESIGN D FLIP-FLOP USING LOW POWER TECHNIQUES

### *A. Design D Flip-flop Using CMOS technique*

In conventional CMOS technique, circuit consists of pull-up network and pull-down network i.e. it comprises of both PMOS and NMOS transistors [8-9]. Hence, both PMOS and NMOS transistors contributed equally to the whole circuit operation. Basically, supply voltages ($V_{dd}$) has been scaled to achieve the aim of low power consumption. The proposed D Flip-flop by CMOS technique is designed using 44 transistors (22 PMOS and 22 NMOS). In this proposed design, the average power consumption and delay of the circuit is reduced. In this design 2 inputs and 2 outputs are as shown in Fig. 3, where 'X' represents the output of the circuit and Y represent the bar of output, D and CLK are the inputs of the circuit designed.

### *B. Design D Flip-flop Using MTCMOS technique*

The proposed D flip-flop by MTCMOS technique is designed using 46 transistors (23 PMOS and 23 NMOS) as shown in Fig. 3. In proposed design by using MTCMOS technique the delay, power delay product, leakage current and average power consumption of the circuit is reduced as compared to conventional circuit [10]. Sleep transistors are also added in this circuit which is used to reduce the leakage and average power consumption of the circuit. These sleep transistors are enabled through sleep signals. High threshold transistors are used as sleep transistors to reduce power consumption in standby mode [10-11]. Low $V_{th}$ transistors are used in the logic circuit to increase the performance during the active mode. High $V_{th}$ PMOS and NMOS transistors connected between the logic circuit and supply rails. Sleep signal activates high threshold transistors during an active mode for actual logic operation. High $V_{th}$ transistors are under turn-off state during standby mode to cut off the logic circuit from supply rails. This minimizes the subthreshold leakages to flow during standby mode. MTCMOS can be an effective technique for low power and high-speed applications.

### *C. Design D Flip-flop Using power gating technique*

The proposed D flip-flop by power gating technique is designed using 45 transistors (23 PMOS and 22 NMOS). In proposed design by using power gating technique the delay power product, leakage current and average power consumption of the circuit is reduced as compared to conventional circuit [10].This technique uses the sleep transistors which work as a headers and footers. In the proposed design header is used to increase the performance of the circuit and reduce the sub threshold leakage.

### *D. Design D Flip-flop Using SVL technique*

The proposed D flip-flop by SVL technique is designed using 48 transistors (24 PMOS and 24 NMOS) as shown in Fig. 3. In proposed design by using SVL technique the leakage current and average power consumption of the circuit is reduced as compared to conventional, MTCMOS and power gating circuits. In this technique, PUN and PDN are connected with basic structure. The differences between PUN and PDN are that it places the transistors opposite site to the other network. SVL is most beneficial technique as compared to the other low power techniques.

## III. FUNCTIONAL DESCRIPTION OF PROPOSED D FLIP-FLOP USING LOW POWER TECHNIQUES

### *A. Functional description of proposed D Flip-flop using CMOS technique*

The Proposed Design of D flip-flop using Conventional CMOS technique has 44 transistors. It has two input first is D and second is CLK and two output X and Y where Y is complementary of X. This flip-flop is an edge triggered D flip-flop which operates at 1 V power supply and stop time is 50ns. This schematic is designed by Cadence virtuoso tool at 45nm technology. This schematic is depending on the clock signal because clock signal works as controller for the flip-flops. CMOS technique is conventional technique which is used to compare other low power techniques. CMOS technique consumes more average power and decrease the performance of D Flip-flop. This is a drawback of CMOS technique. According to the truth table of D flip-flop, it changes the state when clock pulse change states as shown in Fig. 4. This technique was commercially used techniques before the using the low power techniques.

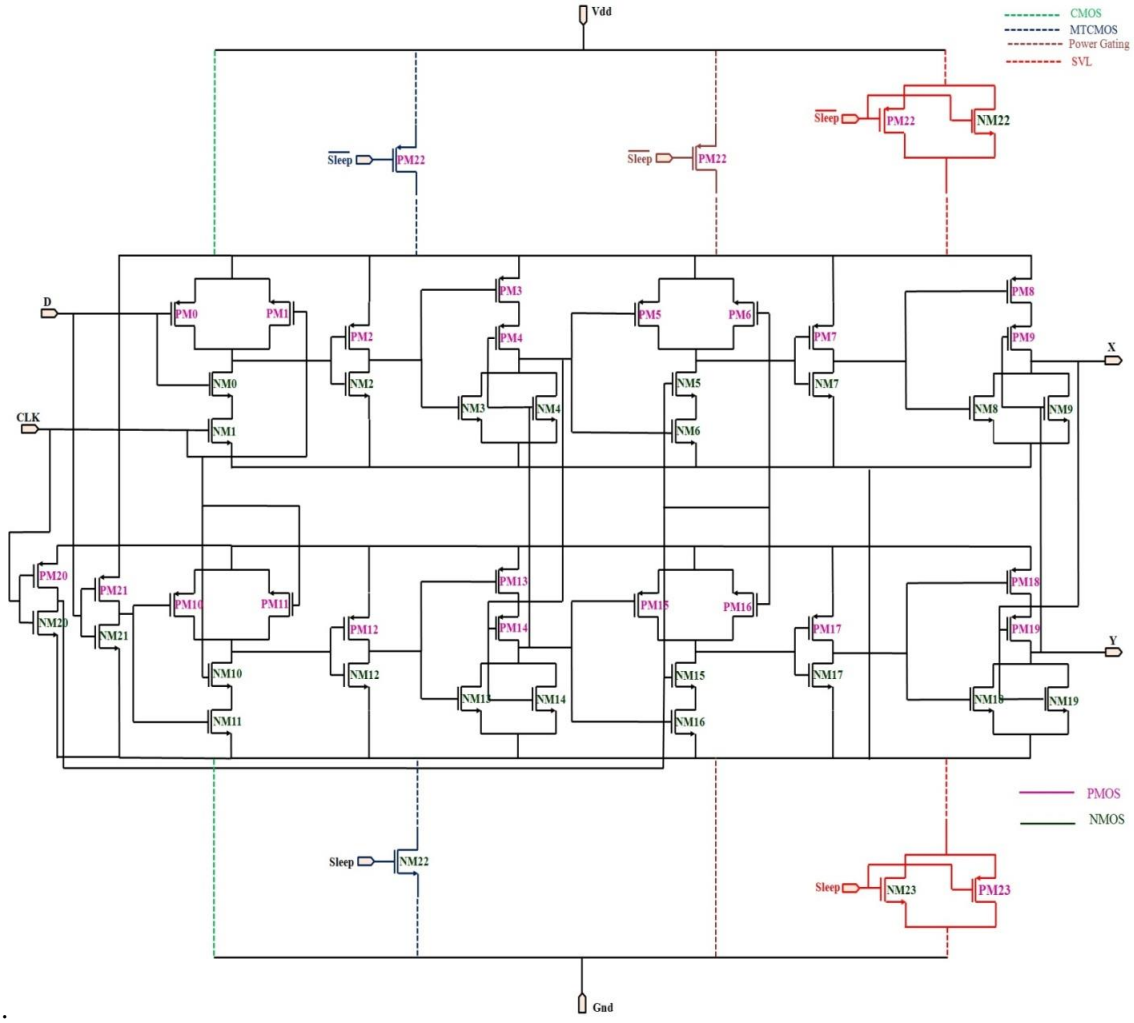


Fig.3: Design D flip-flop using CMOS MTCMOS, power gating and SVL technique at 45nm

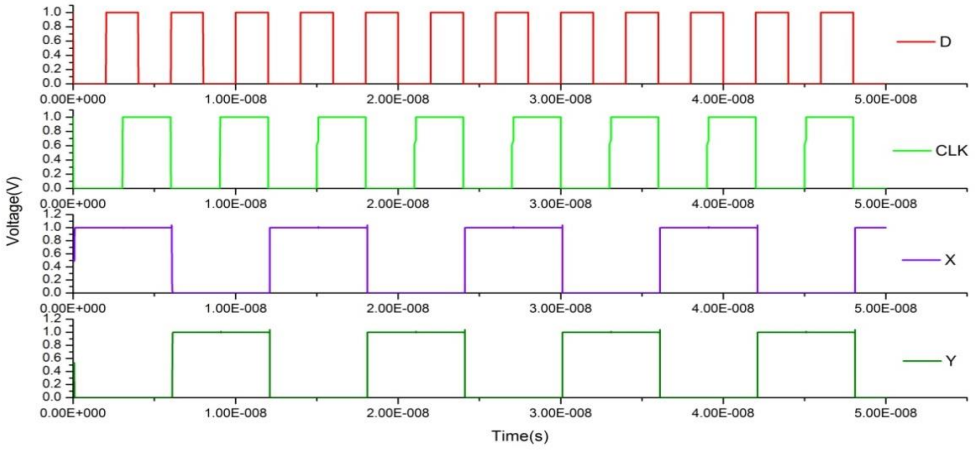


Fig. 4: Transition response of D flip-flop using CMOS

*B. Functional description of proposed D Flip-flop using MTCMOS technique*

The proposed design of D flip-flop using MTCMOS technique has 46 transistors. It has two inputs first is D and second is CLK and two output X and Y where Y is complementary of X. This flip-flop is an edge triggered D flip-flop which operates at 1 V power supply. This schematic is designed by Cadence virtuoso tool at 45nm technology. This schematic is depending on the clock signal because clock signal works as controller for the flip-flops. In a MTCMOS technique, it has two sleep transistors first is PMOS and second is NMOS. Threshold voltage plays a very vital role in CMOS circuits. Threshold voltage is directly related to the leakage current. In low power MTCMOS technique low $V_{th}$ and high $V_{th}$ transistors are used. In the MTCMOS transistors $V_{sb}$ is directly connected to the threshold voltage of MOS transistor. According to DC analysis, threshold voltages of different transistors were analyzed it was observed that threshold voltages of PMOS transistors either at high or low $V_{th}$ was negative values and that of NMOS was positive values. High threshold transistors are used as sleep transistors to reduce power consumption in standby mode [10-11]. Low $V_{th}$ transistors are used in the logic circuit to increase the performance during the active mode. High $V_{th}$ PMOS and NMOS transistors connected between the logic circuit and supply rails. Fig. 5 shows the transition response of the MTCMOS based D flip-flop. The transition response is analyzed that it is a negative edge triggered D flip-flop, it changes the state on the falling edge of clock signal.

*C. Functional description of proposed D Flip-flop using power gating technique*

The proposed design of D flip-flop using power gating technique has 45 transistors. It has two inputs first is D and second is CLK and two output X and Y where Y is complementary of X. This flip-flop is an edge triggered D flip-flop which operates at 1 V power supply. This schematic is designed by Cadence virtuoso tool at 45nm technology. This schematic depends on the clock signal because clock signal works as controller for the flip-flops. This technique is used header or footer that means PMOS is used as a header or NMOS is worked as footer**.**

In this schematic, header is used to reduce power and leakage. This Footer i.e.PM22 is connected to $V_{dd}$ and logic circuit. When sleep is high PM22 is turned off and when sleep is low, this transistor is turned on. When it is turned off it reduce the leakage current and it is turned on connect to the logic circuit provide the output according to the circuit. This technique is consuming huge average power as compare to MTCMOS and less average power as compare to CMOS technique. The performance of the circuit is degrading as compare to MTCMOS. The schematic of power gating-based D flip-flop is shown in Fig. 3. The waveform is simulated at 45nm technology with supply voltage is 1 V as shown in Fig. 6. The output waveform is changing the states when the clock pulse of D flip-flop is falling edge as shown in Fig. 6.

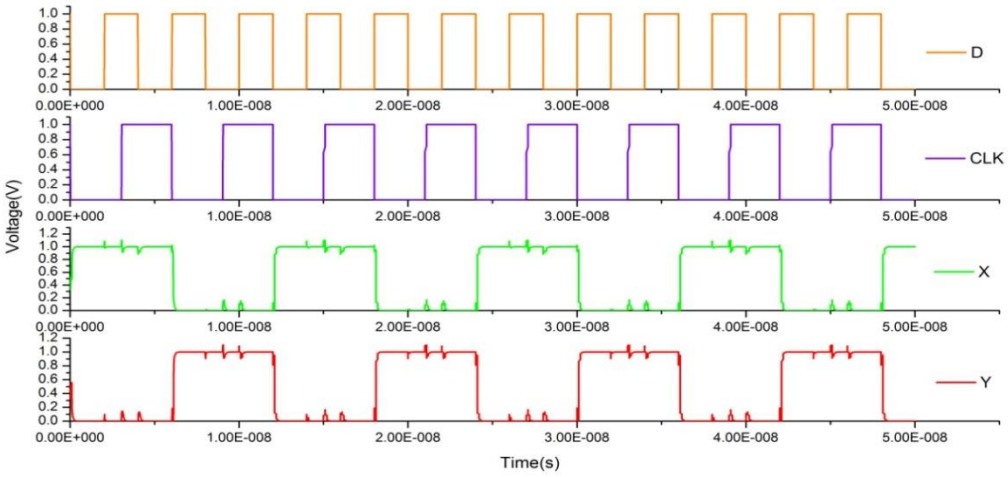


Fig.5: Transition response of D flip-flop using MTCMOS technique

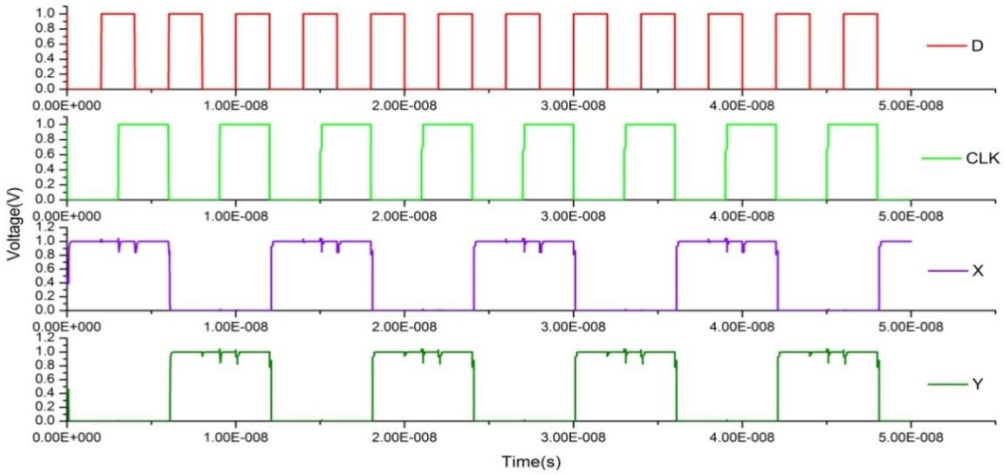


Fig.6: Transition response of D flip-flop using power gating technique

*D. Functional description of proposed D Flip-flop using SVL technique*

The proposed D flip-flop by SVL technique is designed using 48 transistors (24 PMOS and 24 NMOS). PUN and PDN are connected with basic structure. The differences between PUN and PDN are that it places the transistors opposite site to the other network. When sleep is high and sleep bar is turned low NM22 is turned off logic circuit will be connect to $V_{dd}$, When sleep is turned low the circuit will work in standby mode so no more power supply will require to keep in standby mode. When sleep is low, NM23 is turned to off then output will depend on PMOS and it provides bad logic that means $V_{th}$ at output node.

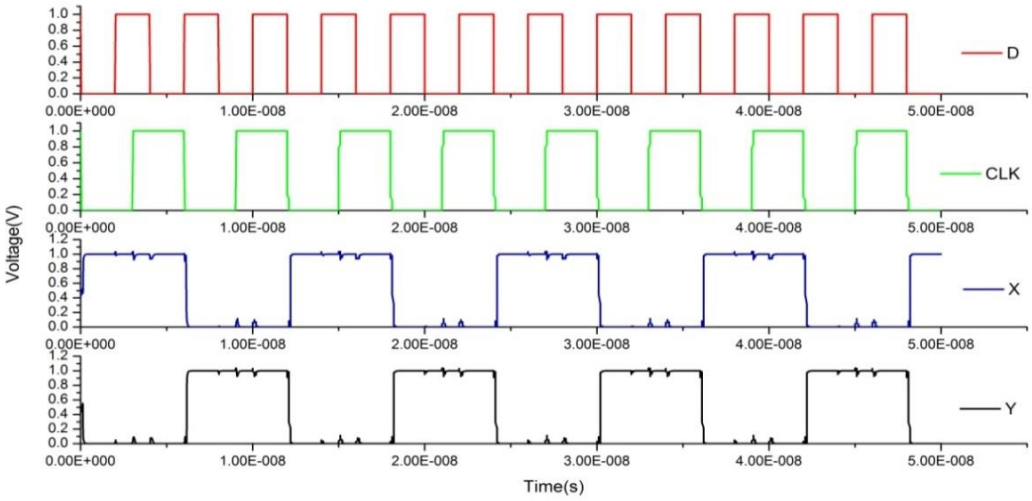


Fig.7: Transition response of D flip-flop using SVL technique

This technique is reduced huge power as compared to other techniques. This schematic is designed by Cadence virtuoso tool at 45nm technology. The waveform is also simulated at 45nm technology with supply voltage is 1 V and stop time is 50ns as shown in fig 7. The output waveform is changing the states when the clock pulse of D flip-flop is low as shown in fig 7.

## IV. PHYSICAL DESIGN METHODOLOGY OF PROPOSED D FLIP-FLOP

The physical designs of D flip-flop are shown with different techniques in figures. The designs demonstrated with zero design rule checker error and also with successful layout versus schematic match. The design has a P & R boundary of 200 $\mu$m × 132 $\mu$m with about 44 transistors used in CMOS technique which shown in fig.8, 46 transistors are used MTCMOS technique which shown in Fig. 9, 45 transistors are used in power gating technique as shown in Fig. in fig. 10 and 48 transistors are used in SVL technique shown in fig 11. These layouts are used to reduce the area of the designs and these are verified by the DRC and LVS. The DRC is known as the Design Rule Check which is verify the parameter specification and LVS is known as the Layout Versus Schematic which is used to remove the mismatching with the schematic.

In these designs, there were three metal layers has been implemented. The circuits were designed at 1 V and at 27 ℃ junction temperature at 45nm. The designed layouts can represented the negative edge triggered D flip-flop.

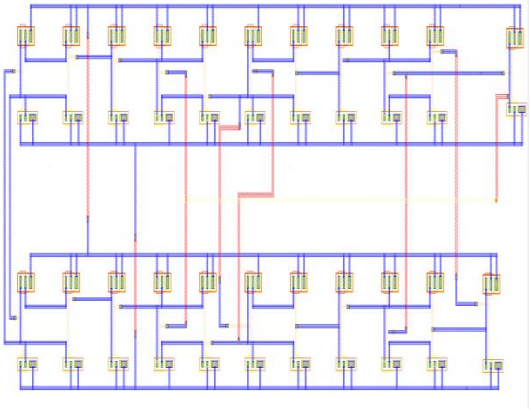

Fig.8: Layout design of D flip-flop using CMOS technique

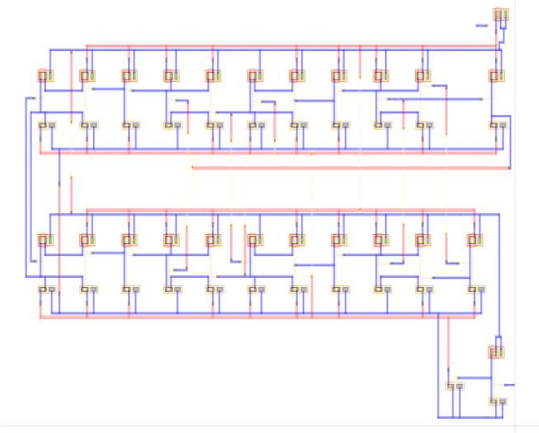

Fig.9: Layout design of D flip-flop using MTCMOS technique

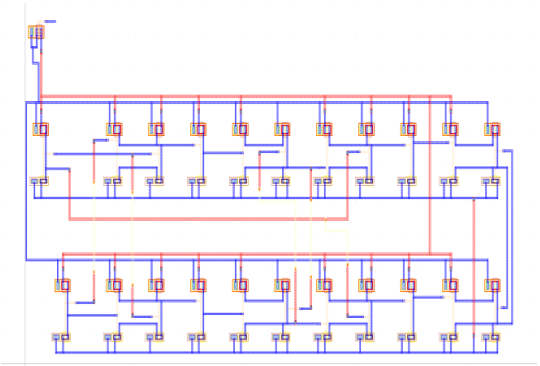

Fig.10: Layout design of D flip-flop using power gating technique

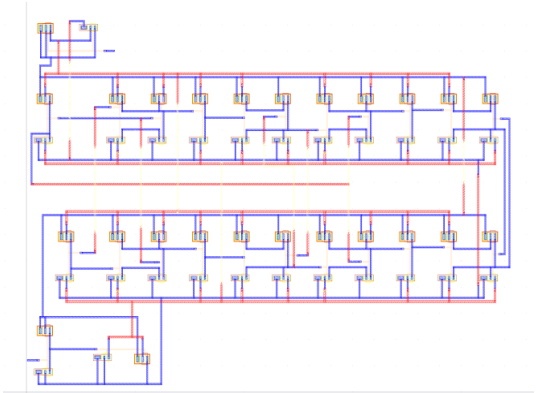

Fig.11: Layout design of D flip-flop using SVL technique

## V. GRAPHS OF POWER CALCULATION FOR LOW POWER TECHNIQUES AT 45NM

Graphs of average power calculation are shown the power consumed by the circuit designed using CMOS, MTCMOS, SVL and power gating technique at 45nm as shown in fig 12-15. Hence, power consumption can be reduced to great extent using SVL technique as compared to the CMOS, Power gating and MTCMOS technique.

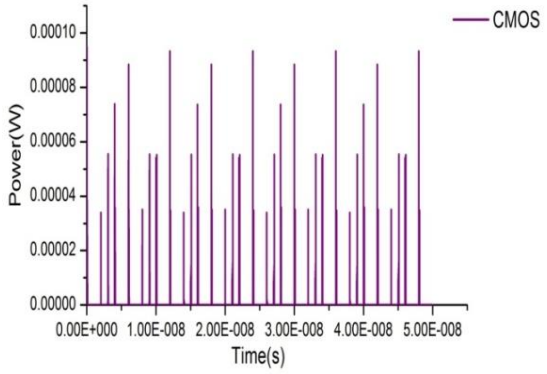


Fig.12: Simulation waveform of power consumption using CMOS technique

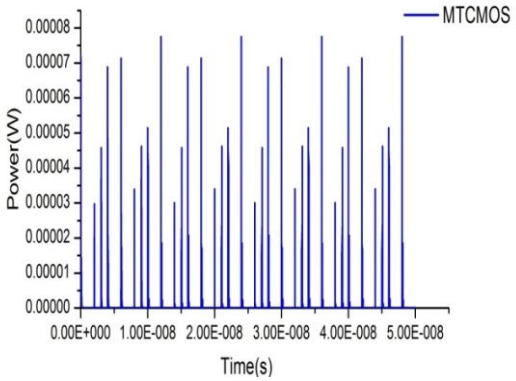


Fig.13: Simulation waveform of power consumption using MTCMOS technique

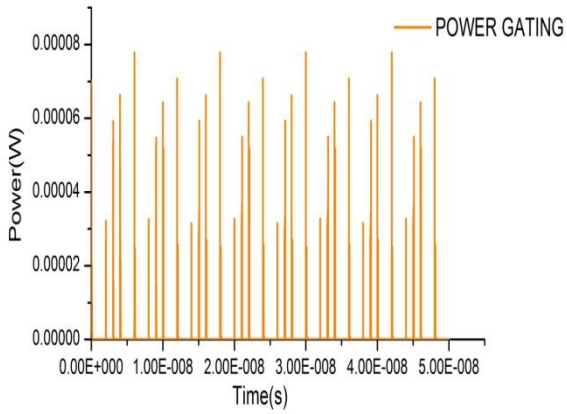


Fig.14: Simulation waveform of power consumption using power gating technique

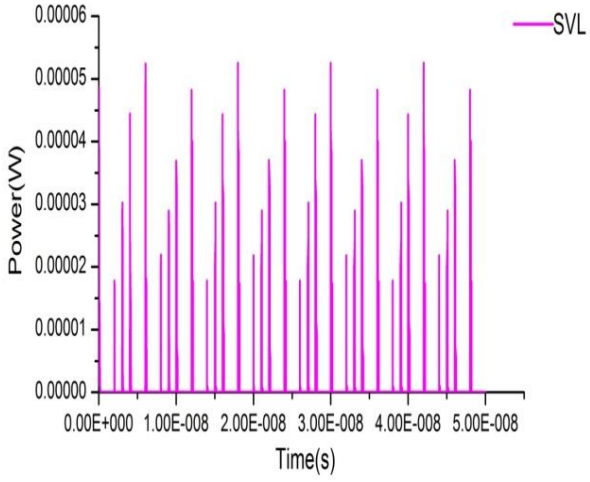


Fig.15: Simulation waveform of power consumption using SVL technique

## VI. GRAPHS OF LEAKAGE CURRENT CALCULATION FOR LOW POWER TECHNIQUES AT 45NM

Graphs of leakage current calculation are shown the circuit designed using CMOS, MTCMOS, SVL and power gating techniques at 45nm.

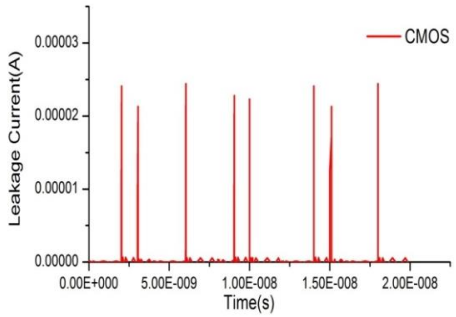


Fig.16: Simulation waveform of leakage current using CMOS technique

Hence, leakage current can be reduced to great extent using SVL technique as compared to the CMOS, Power gating and MTCMOS technique.

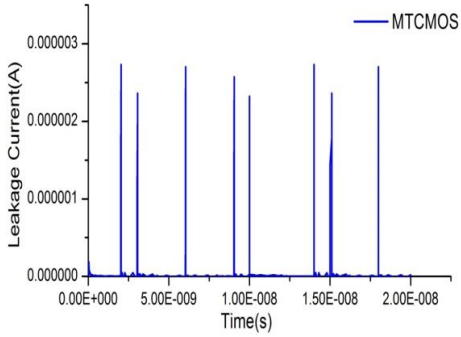


Fig.17: Simulation waveform of leakage current using MTCMOS technique

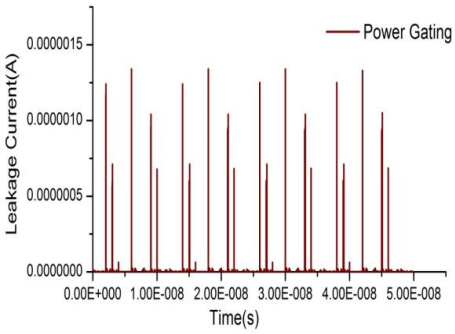


Fig.18: Simulation waveform of leakage current using power gating technique

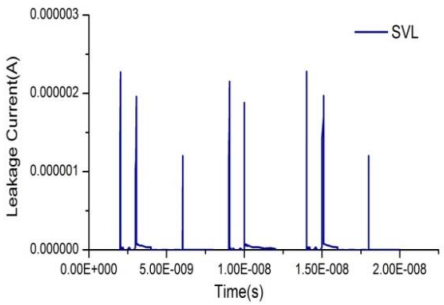


Fig.19: Simulation waveform of leakage current using SVL technique

## VII. CONCLUSION

The table of different parameters are shown in table 1. This table has explained the performance of parameters in different techniques. In this comparison SVL technique consume less power as compared to other techniques. SVL technique also reduces the delay as compared to other techniques that means increase the overall performance of circuit. Leakage current can also be reduced by SVL technique as compare to others techniques.

**TABLE .1.** Comparison of different parameters in different techniques-based D Flip-flop

| PARAMETER | CMOS | MTCMOS | Power Gating | SVL |
|---|---|---|---|---|
| Average Power Consumption (uW) | 1.34 | 1.23 | 1.24 | 1.21 |
| Propagation Delay (D-X) (ns) | 32.97 | 1 | 2.07 | 0.98 |
| Power Delay Product (D-X)(fJ) | 44.18 | 1.23 | 2.57 | 1.19 |
| Propagation Delay (CLK-X)(ns) | 4.56 | 1.59 | 4.57 | 4.63 |
| PDP (CLK-X) (fJ) | 6.11 | 1.95 | 5.68 | 5.60 |
| Leakage Current (nA) | 19.04 | 1.38 | 15.0 | 0.61 |

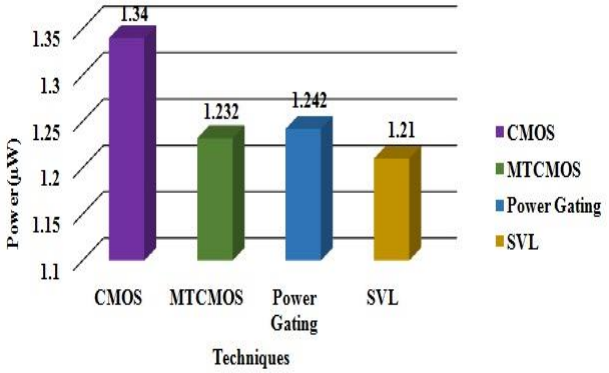


Fig.20: Comparison in average power for techniques-based D flip-flop

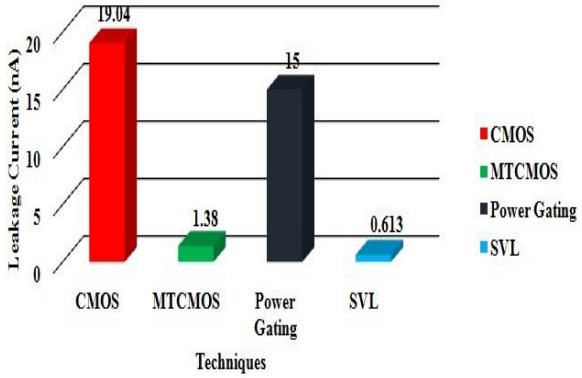


Fig. 21: Comparison in leakage current for techniques-based D flip-flop

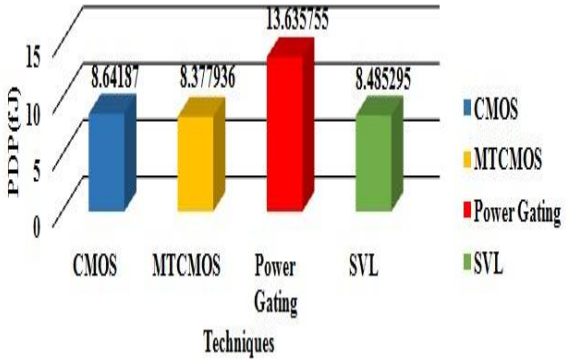


Fig. 22: Comparison in power delay product for techniques-based D flip-flop

The bar graphs of average power, leakage current and power delay product are shown fig 20, fig 21 and fig 22. These bar graphs explained the comparison of different parameters of D flip-flop with different techniques. The bar graph of average power shows that SVL technique is better than other techniques. The bar graph of leakage current shows that SVL technique is better than other techniques. MTCMOS technique is also reduced leakage current as compared power gating and CMOS techniques. The bar graph of power delay product shows that MTCMOS technique is increase the performance as compared to the others techniques. In term of power consumption, MTCMOS based D flip-flop is reduced by 8.2 %, power gating based D flip-flop is decreased by 7.42% while more reduction in SVL based D flip-flop is brought down by 10% as compared to conventional CMOS based D flip-flop at 45nm technology.

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