Single-Phase Rectifier is Composed of Two Parallel Single-Phase Half-Bridge Rectifiers

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Abstract **-** Commercial and industrial electrical equipment requires three-phase power. Electric utilities do not install three-phase power as a matter of course because it cost significantly more than single-phase installation. Hence we need to conversion from single-phase to three-phase. Parallel converters have been used to improve the power capability, reliability, efficiency, and redundancy. Usually the operation of converters in parallel requires a transformer for isolation. This paper presents two single-phase to three-phase conversion systems for a three-phase load application. The load is connected to a single-phase grid through an ac–dc–ac single-phase to three-phase converter. The single-phase rectifier is composed of two parallel single-phase half-bridge rectifiers. The first proposed topology is composed of a full-bridge three-phase inverter, i.e., three-leg inverter, while the other topology is composed of a two-leg inverter. Suitable modeling, including the circulation current, and control strategy are presented. A pulse width modulation (PWM) technique using a single or double carriers PWM implementation is presented. Proposed topologies permit to improve the harmonic distortion. In addition, the P5L converter can reduce the converter power losses.

Keywords – Ac-dc-ac power converter, 3- phase three-phase power, parallel converter, full-bridge three-phase inverter.

I. INTRODUCTION

Parallel converters can be used to improve the power capability, reliability, efficiency and redundancy. Parallel converter techniques can be employed to improve the performance of active power filters, uninterruptable power supplies, fault tolerance of doubly fed induction generators and three phase drives. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design. This work proposes a single phase to three phase drive system composed of two parallel single phase rectifiers, an induction motor and three phase inverter. The proposed system permits to reduce the rectifier switch currents, the total harmonic distortion (THD) of the grid current with same switching frequency and to increase the fault tolerance characteristics. Even with the increase in the number switches, the total energy loss of the proposed system is lower than that of conventional system. The model of the system will be derived. A suitable control strategy and pulse width modulation technique (PWM) will be developed. The complete comparison between the proposed and standard configurations will be carried out in this work. Simulation of this project will be carried out by using MATLAB/ Simulink. The rectifier side uses two parallel legs (each leg represents a half-bridge rectifier), as shown in Fig. 3. The first topology presents five legs, i.e., P5L converter [see Fig. 3(a)] and the second one uses four legs, i.e., P4L converter [see Fig. 3(b)]. The topology P5Lwas proposed in [23]. In fact, the proposed topologies are obtained by the addition of two parallel half-bridge rectifier with two known inverter circuits. However, these topologies can improve the overall performance of ac–dc–ac converter, such as the harmonic distortion and efficiency, when compared to topologies with a close number of switches (conventional 5L and 3L converter). These topologies improve the division of power flow between the inverter and rectifier switches, which can reduce the power losses at the rectifier circuits. They are also more economically attractive, with lower cost, because they use a smaller amount of power devices in comparison with the 7L converter. Suitable modeling, control strategy, and circulation current control are presented for the validation purposes.

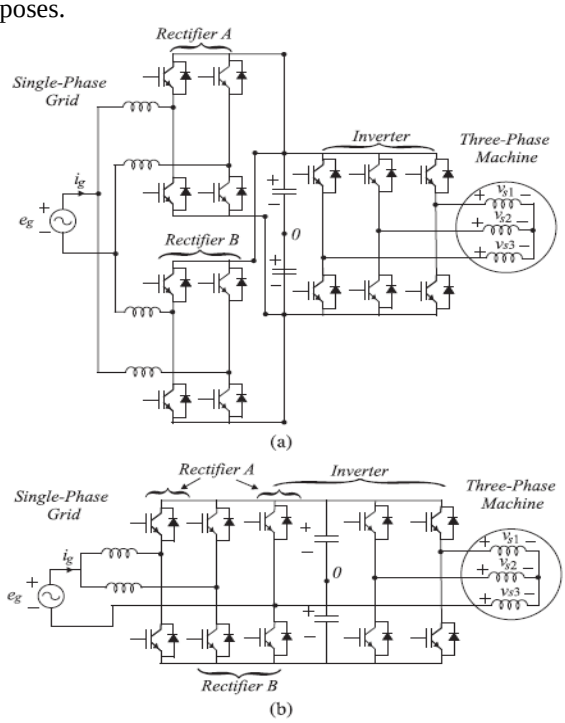

Figure 1: Parallel 1ph-to-3ph converter (a) With parallel full-bridge rectifiers (seven legs denominated as 7L) (b) Parallel rectifier with a shared leg (five leg denominated as 5La)

Among topologies addressed in this paper, the P5L topology presents the best performance, because it can reduce: 1) power losses in switches, due to a reduction of the current in rectifier circuit and 2) the harmonic distortion on the utility grid, when the interleaved technique is applied. The P4L topology reduces the harmonic distortion compared by the 3L converter and provides the same harmonic distortion of the conventional 5L counterpart in the single-phase grid, when the interleaved technique is also adopted. The output three-phase ac voltages of the proposed systems can be variable, to supply a motor with variable voltages for achieving its speed and torque control, or with constant amplitude and frequency, to supply constant three-phase load type.

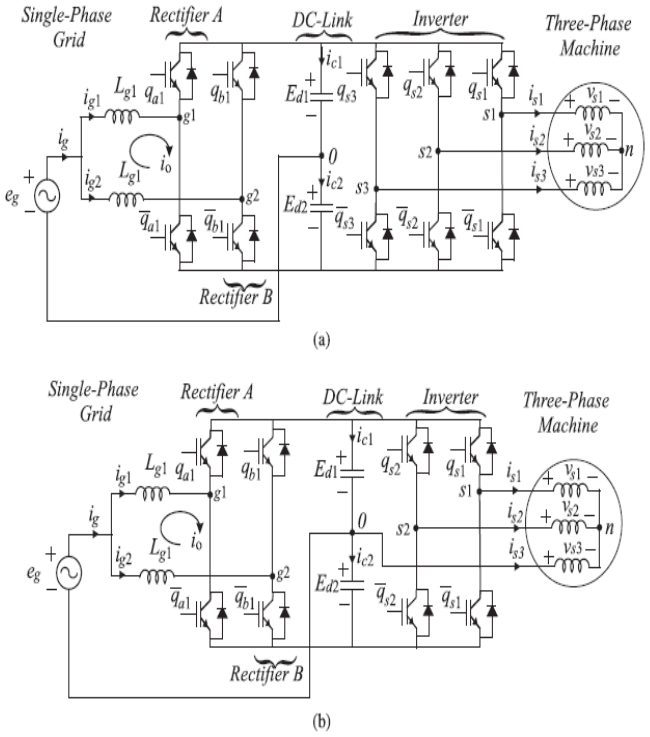

Figure 2: Proposed 1ph-to-3ph converter using a half-bridge rectifier circuit (a) Parallel five-leg (P5L) converter (b) Parallel four-leg (P4L) converter

II. PWM CONTROLLER

This controller offers a basic "Hi Speed" and "Low Speed" setting and has the option to use a "Progressive" increase between Low and Hi speed. Low Speed is set with a trim pot inside the controller box. Normally when installing the controller, this speed will be set depending on the minimum speed/load needed for the motor. Normally the controller keeps the motor at this Lo Speed except when Progressive is used and when Hi Speed is commanded (see below). Low Speed can vary anywhere from 0% PWM to 100%.

Progressive control is commanded by a 0-5 volt input signal. This starts to increase PWM% from the low speed setting as the 0-5 volt signal climbs. This signal can be generated from a throttle position sensor, a Mass Air Flow sensor, a Manifold Absolute Pressure sensor or any other way the user wants to create a 0-5 volt signal. This function could be set to increase fuel pump power as turbo boost starts to climb (MAP sensor). Or, if controlling a water injection pump, Low Speed could be set at zero PWM% and as the TPS signal climbs it could increase PWM%, effectively increasing water flow to the engine as engine load increases. This controller could even be used as a secondary injector driver (several injectors could be driven in a batch mode, hi impedance only), with Progressive control (0-100%) you could control their output for fuel or water with the 0-5 volt signal.

Progressive control adds enormous flexibility to the use of this controller. Hi Speed is that same as hard wiring the motor to a steady 12 volt DC source. The controller is providing 100% PWM, steady 12 volt DC power. Hi Speed is selected three different ways on this controller: 1) Hi Speed is automatically selected for about one second when power goes on. This gives the motor full torque at the start. If needed this time can be increased (the value of C1 would need to be increased). 2) High Speed can also be selected by applying 12 volts to the High Speed signal wire. This gives Hi Speed regardless of the Progressive signal.

When the Progressive signal gets to approximately 4.5 volts, the circuit achieves 100% PWM – Hi Speed.

How does this technology help?:

The benefits noted above are technology driven. The more important question is how the PWM technology Jumping from a 1970's technology into the new millennium offers:

A. Longer battery life:

- reducing the costs of the solar system
- reducing battery disposal problems

B. More battery reserve capacity:

- increasing the reliability of the solar system
- reducing load disconnects
- opportunity to reduce battery size to lower the system cost

C. Greater user satisfaction:

- get more power when you need it for less money!!

III. SYSTEM MODEL

The P5L configuration presented in Fig. 3(a) is composed of two single-phase half-bridge rectifiers (rectifiers A and B), a dc-link, a three-phase inverter and a three-phase motor or a three-phase load. On the other hand, the P4L configuration [see Fig. 3(b)] is composed of a two-leg inverter instead three-leg inverter of the P5L converter.

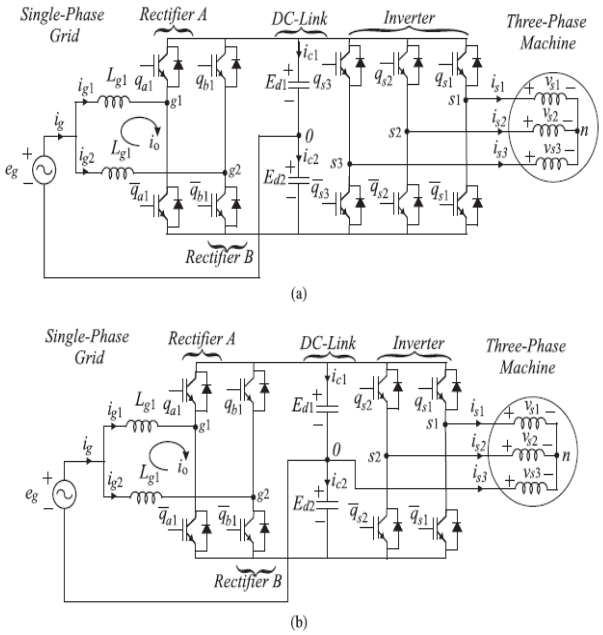

Figure 3: Proposed 1ph-to-3ph converter using a half-bridge rectifier circuit (a) Parallel five-leg (P5L) converter (b) Parallel four-leg (P4L) converter

A. Rectifier Model:

From Fig. 3, the following model is derived:

$$e_g = r_{g1} i_{g1} + l_{g1} \frac{di_{g1}}{dt} + v_{g10} \quad (1)$$

$$e_g = r_{g1} i_{g2} + l_{g1} \frac{di_{g2}}{dt} + v_{g20} \quad (2)$$

$$i_g = i_{g1} + i_{g2} \quad (3)$$

where *rg*1 represents the resistance of the inductor filter *Lg*1 , *lg*1 represents the inductance of the inductor filter *Lg*1 , *vg*10, and *vg*20 are the pole voltages of the rectifiers A and B, respectively, *ig* is the grid current and *ig*1 and *ig*2 are the input currents of the rectifiers A and B, respectively.

The previous model can also be expressed by using the circulating current *io* introduced by

$$i_{g1} = \frac{i_g}{2} + i_o \quad (4)$$

$$i_{g2} = \frac{i_g}{2} - i_o. \quad (5)$$

From (1) to (5), the complete system model is given by

$$e_g = \left(\frac{r_{g1}}{2}\right) i_g + \left(\frac{l_{g1}}{2}\right) \frac{di_g}{dt} + v_g \quad (6)$$

$$v_o = r_{g1} i_o + l_{g1} \frac{di_o}{dt} \quad (7)$$

With

$$i_o = \frac{i_{g1} - i_{g2}}{2} \quad (8)$$

$$v_g = \frac{v_{g10} + v_{g20}}{2} \quad (9)$$

$$v_o = \frac{-v_{g10} + v_{g20}}{2}. \quad (10)$$

From (6) to (10), it is clear that the grid and circulating currents depend on the voltages *vg* and *vo* , respectively. Then, the rectifier pole voltages can be calculated from desired voltages (*vg* and *vo*) to control these currents. Considering circulating current null and the equivalent inductor *Lg* = *Lg*1/2 equal to that of the conventional converter, the front-end model of the configurations presented in Fig. 3 is identical to that of the conventional 5L converter.

B. Inverter Model:

The inverter model for the P5L configuration is given by

$$v_{s1} = v_{s10} - v_{n0} \quad (11)$$

$$v_{s2} = v_{s20} - v_{n0} \quad (12)$$

$$v_{s3} = v_{s30} - v_{n0} \quad (13)$$

where *vs*10, *vs*20, and *vs*30 are the pole voltages of the inverter, *vs*1 , *vs*2 , and *vs*3 are the voltages of the three-phase load, and *vn*0 is the voltage between the point *n* and the dc-link midpoint 0. While the model of inverter of the P4L configuration is given by

$$v_{s13} = v_{s10} \quad (14)$$

$$v_{s23} = v_{s20} \quad (15)$$

where *vs*13 and *vs*23 are line voltages of the three-phase load.

C. Control Strategy:

The control system of the proposed converters has the same objectives of the conventional one, i.e., dc-link voltage and power factor control from rectifier circuit and load voltage control from inverter circuit. Additionally, the proposed control system needs to regulate the circulating current between the parallel half-bridge rectifiers. Fig. 4 shows the control block diagram of the P5L and P4L converters proposed in this paper.

The capacitor dc-link voltage *Ed* (*Ed*1 + *Ed*2) is adjusted to its reference value *E*∗*d* utilizing a proportional integral (PI) type controller. This controller provides the amplitude of the reference grid current *I*∗*g*. To control power factor and harmonics at the grid side, the instantaneous reference grid current *i*∗*gx* must be synchronized with the grid voltage *eg* based on phase locked loop scheme [24]. Control of the grid current is implemented using a synchronous controller (a resonant controller type) described in [25]. The block *Rg*

represents this controller. It defines the reference grid voltage $v*g$.

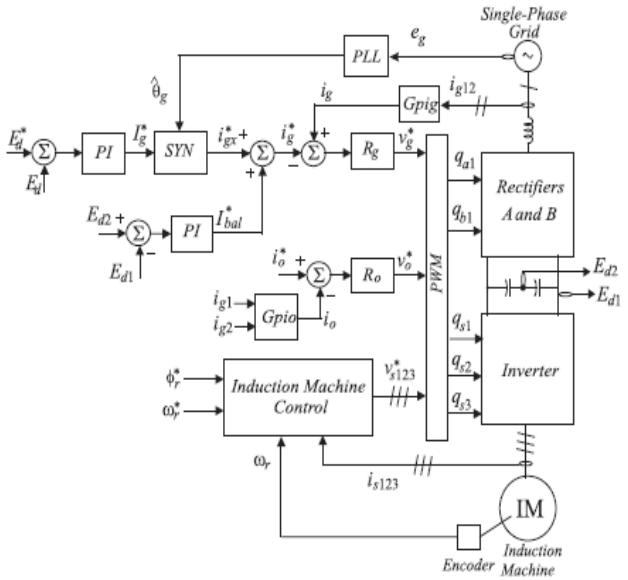

Figure 4: Control block diagram used for configurations P5L and P4L

The circulating current (*io*) is obtained by block *Gpio* from the measured rectifiers currents *ig*1 and *ig*2 . This block is based on (8). The circulating current is compared to its reference ($i*o = 0$). The error is the input of a synchronous controller (*Ro*), and gives in its output the voltage $v*o$.

Due to different dead-time switches, non-sinusoidal grid voltage or different capacitance, the voltage balance between the split capacitors obtained naturally may not be satisfactory. Some works have proposed solutions to voltage balance between the split capacitors of the half-bridge rectifier [26]–[29]. One way to minimize the voltage imbalance between split capacitors is to add a current balance value $i*$bal in the reference grid current. The difference in voltage between the split capacitors (*Ed*1 – *Ed*2) is input of the conventional PI controller. This controller provides the reference current balance value ($i*$bal). The reference grid current is achieved by adding $i*gx$ with $i*$bal ($i*g = i*gx + i*$bal), as discussed in [27]. The voltage balance between the split capacitors is carried out, but it is necessary to apply a small distortion in the reference grid current. When a three-phase motor is used, control can be performed by the field-oriented control (FOC) technique as shown in [30] or volt/hertz control.

D. DC-Link Capacitor Voltage:

Considering that all the voltages are purely sinusoidal, the voltage limit conditions of each configuration is shown in the Table I. Where *Vg* represents the amplitude of rectifier voltage, whereas *Vs* denotes the amplitude of the load phase voltage. If the input voltage is equal to output voltage (i.e., *Vg =Vs)*, the conventional 5L converter has the best dc-link voltage rating. The proposed P5L converter has the dc-link voltage 15% bigger than the conventional 5L one. While conventional 3L and proposed P4L converters require twice the dc-link voltage of the conventional 5L one.

On the other hand, when the output voltage is double the input voltage (i.e., *Vs* = 2*Vg*), the proposed P5L converter can operate with the same dc-link voltage of the conventional 5L converter.

Table 1: Dc-Link Voltage Limits

Configurations	Input Limit	Output Limit
5L	$E_d \geq V_g$	$E_d \geq \sqrt{3}V_s$
3L	$E_d \geq 2V_g$	$E_d \geq 2\sqrt{3}V_s$
P5L	$E_d \geq 2V_g$	$E_d \geq \sqrt{3}V_s$
P4L	$E_d \geq 2V_g$	$E_d \geq 2\sqrt{3}V_s$

IV. CONCLUSION

In this paper, two drive motor systems have been presented. These systems are composed of an ac–dc–ac single-phase to three-phase converter. The single-phase rectifier combines two parallel single-phase half-bridge converters without transformers. Suitable model and control strategy, including the PWM strategy have been developed. Table V summarizes the comparison between the conventional and proposed configurations for different figures of merit. In this table, the dc-link voltage, the WTHD and semiconductor power losses are normalized by the conventional 5L topology. The results for P5L and P4L configurations were obtained with double-carrier PWM, the condition that guarantees the lowest harmonic distortion.

V. REFERENCES

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