DESIGN, FABRICATION AND TESTING OF MONOLITHIC LOW-POWER PASSIVE SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTERS

by

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Bachelor of Science in Electrical Engineering

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2013

A thesis submitted in partial fulfillment of the requirements for the

Master of Science in Engineering – Electrical Engineering

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November 2015

ABSTRACT

Analog-to-digital converters are critically important in electronic systems. The difficulty in meeting high performance parameters increases as integrated circuit design process technologies advance into the deep nanometer region. Sigma-delta analog-to-digital converters are an attractive option to fulfill many data converter requirements. These data converters offer high performance while relaxing requirements on the precision of components within an integrated circuit. Despite this, the active integrators found within sigma-delta analog-to-digital converters present two main challenges. These challenges are the power consumption of the active amplifier and achieving gain-bandwidth necessary for sigma-delta data converters in deep nanometer process technologies. Both of these challenges can be resolved through the replacement of active integrators with passive integrators at the expense of resolution.

Three passive sigma-delta topologies were examined and characterized in detail. Two of these topologies were first-order and second-order noise shaping topologies. A new passive topology was developed which was determined to be optimal in resolution compared to the two traditional designs. This topology exhibits a first-order signal transfer function and a second-order noise transfer function. A method for increasing resolution of passive sigma-delta data converters despite inherent performance constraints was developed.

Three example circuits were designed, fabricated and tested using On Semiconductor's C5 500 nanometer CMOS process. These designs were optimized for low

power and utilized memory sense amplifiers as quantizing elements. The first circuit, using passive lumped on-chip elements for the noise shaping network achieved a power consumption of 100 micro-watts and an effective resolution of 8-bits. The second circuit replaced the lumped components with switched-capacitor elements and achieved a power consumption of 6.75 micro-watts and an effective resolution of 9.3 bits. The third circuit was designed as a case study for the application of the proposed topology to "K-delta-1-sigma" modulators. This circuit achieved a power consumption of 10 milli-watts and an effective resolution of 8.5 bits.

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. R. Jacob Baker for the extensive, untiring support provided to me as a student at UNLV. He has served not only as an academic advisor but as a role model for the rest of my life. I would like to thank my committee for all the guidance they have given to me over the years –Dr. Peter Stubberud, Dr. Yahia Baghzouz, and Dr. Evangelos Yfantis. My undergraduate research team consisting of Matthew Meza, Joey Yurgelon, Dane Gentry, Mario Verduzco, Michael Ghisilieri and Gerardo Gomez have been instrumental and critical to the completion of this research. I would like to thank Brandon Blackstone for providing the facility resources needed to complete this research as well as being a mentor to me. I would also like to thank Golf Nantanapramoth for providing electronic components at all hours of the night. Finally, I am grateful to my parents for providing a supportive environment that has facilitated my education. I am especially grateful for my father's encouragement in pursuing lifelong education.

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Chapter 1 Introduction

Analog to digital converters (ADC) are one of the most important types of electronic circuits today. They are found in any application where an analog signal needs to be converted into a digital value. Almost all quantifiable natural phenomena such as light and sound are analog in nature. However, most modern electronic components such as microcontrollers and processors require inputs in the form of digital values. The analog to digital converter bridges this divide. Due to the ubiquity of digital electronics, ADCs are found in almost all electronic circuits. There are many different topologies of ADC each with their strengths and weaknesses.

ADCs can be grouped into two broad categories, Nyquist-rate and oversampling. A Nyquist-rate ADC samples the signal at a frequency that is twice that of the maximum input signal frequency. Historically most ADCs have been Nyquist-rate ADCs. Topologies in this category include the flash ADC, the successive-approximation (SAR) ADC, pipeline ADCs and many others. These ADC topologies all suffer from the requirement that precision analog circuitry is needed to ensure accuracy. As semiconductor process technologies progress, it becomes increasingly difficult to fabricate precision analog components. Oversampling ADCs gain an increase in resolution by an increase in sampling rate. The sampling rate is set higher than the maximum input frequency by some multiple. This increases the resolution through averaging. Any Nyquist-rate ADC can be run as an oversampled ADC to increase resolution at the expense of bandwidth assuming that the

analog input signal is busy [1]. However, the true benefits of oversampling become apparent when combined with noise-shaping to create the sigma-delta (∑-Δ) ADC.

The key benefit of oversampling is that an ADC can have a higher effective resolution than its nominal value. For example an 8-bit ADC can have an effective 10-bit resolution with 16X oversampling. The problem with using Nyquist-rate ADCs in this manner is that any Nyquist-rate ADC will have significant constraints on analog precision regardless of oversampling. If the concept of oversampling is extended to its most basic implementation, it becomes possible to theoretically realize any resolution with just a 1-bit ADC. There are many benefits to using a 1-bit ADC. Precision requirements are relaxed on components since there are only two states of operation and thus the ADC is inherently linear [2]. Power consumption is decreased since only a single active quantizing element is required. Integration into nano-CMOS processes is facilitated by the simplicity of the design. Combined with noise-shaping, a 1-bit oversampling ADC forms the heart of the sigma-delta ADC. Due to all these benefits, ∑-Δ ADCs have become the topology of choice for low-cost high resolution data converters.

Sigma-delta ADCs can be further categorized as active or passive. While all ADCs use active components, the term refers to the active integrator when applied to sigma-delta ADCs. Most ∑-Δ ADCs use an active amplifier configured as an integrator to perform the integration function. A passive ∑-Δ ADC replaces the active integrator with a capacitor. This reduces the linearity but also decreases power consumption. Usually 1^{st} or 2^{nd} order noise-shaping is used in passive ∑-Δ ADCs. It is generally not practical to realize passive ∑-Δ ADCs with higher order noise-shaping. As a result of their poor linearity, passive ∑-Δ ADCs

have not been extensively investigated and other ADC topologies, particularly SAR, have been used for low power applications. A passive ∑-Δ ADC is a viable alternative choice for applications where minimum power consumption is the highest priority. A novel passive 2^{nd} order ∑-Δ has been developed that improves linearity while retaining low power consumption. This topology can be implemented in purely digital systems such as microcontrollers or FPGAs as well as integrated circuits.

Oversampling

The concept of oversampling is fundamentally important to the function of sigma-delta ADCs. Simple oversampling can be applied to any data converter topology. For a given analog signal bandwidth, a minimum frequency of twice that bandwidth is required to digitize the signal without aliasing. This concept is described formally as the *Nyquist Criterion* which is mathematically given by

$$f_{sampling=2f_{MAX}} \tag{1.1}$$

Where $f_{sampling}$ is the minimum sampling rate required to accurately digitize the analog signal without aliasing, and $f_{MAX}$is the bandwidth of the sampled signal. Oversampling involves running a data converter at a sampling rate that is higher than $2f_{max}$. For ease of signal processing and binary math operations usually this ratio is chosen to be a multiple of two. For example using a sampling rate of 32 MHz for a signal bandwidth of 1 MHz is oversampling by 16X. The required oversampling ratio (OSR) required to get n additional bits of precision is given by

$$OSR = 2^{2n} \tag{1.2}$$

Using this equation, if one desired to have 10-bit resolution from an 8-bit data converter, an OSR of 16X would be required. An important caveat to this is that this equation is valid only if the inherent linearity of the 8-bit data converter is at least equal to a 10-bit resolution. For a theoretical data converter perfect linearity is assumed. To understand why oversampling increases the resolution of an ADC, it is important to understand the concept of quantization noise.

Whenever an analog signal is sampled, there is an error between the quantized value and the actual value of the analog signal. This error as a function of time varies between -1/2 LSB and +1/2 LSB (least significant bit). The difference between the quantized value and the actual value gives rise to quantization noise. Quantization noise is white and its amplitude depends on the value of the LSB of the ADC [3]. The derivation of the frequency content of quantization noise starts by treating the quantization error, Q_e, as a random variable. The probability density function of this variable is plotted in Fig. 1.1a. The quantization error noise power is given by,

$$P_{Qe} = \int_{-\frac{1}{2}LSB}^{+\frac{1}{2}LSB} \rho * (Q_e) * dQ_e = \frac{V_{LSB}^2}{12} \tag{1.3}$$

The RMS quantization noise voltage is the square root of the quantization noise power and is given by,

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \tag{1.4}$$

In order to get the spectral density function, the quantization noise power is set equal to the following integral,

$$\frac{V_{LSB}^2}{12} = 2 * \int_0^{\frac{fs}{2}} V_{Qe}^2(f) * df \tag{1.5}$$

The integral is multiplied by 2 to account for the power contributed by the negative frequencies of the spectrum. Solving this equation results in

$$V_{qe}(f) = \frac{V_{LSB}}{\sqrt{12 * f_s}} \tag{1.6}$$

The key result from this equation is that the amplitude of the quantization noise is equal to $\frac{V_{LSB}}{\sqrt{12*fs}}$ and is equally distributed to the Nyquist frequency of $f_n = \frac{fs}{2}$. This is illustrated in Fig. 1.1b.

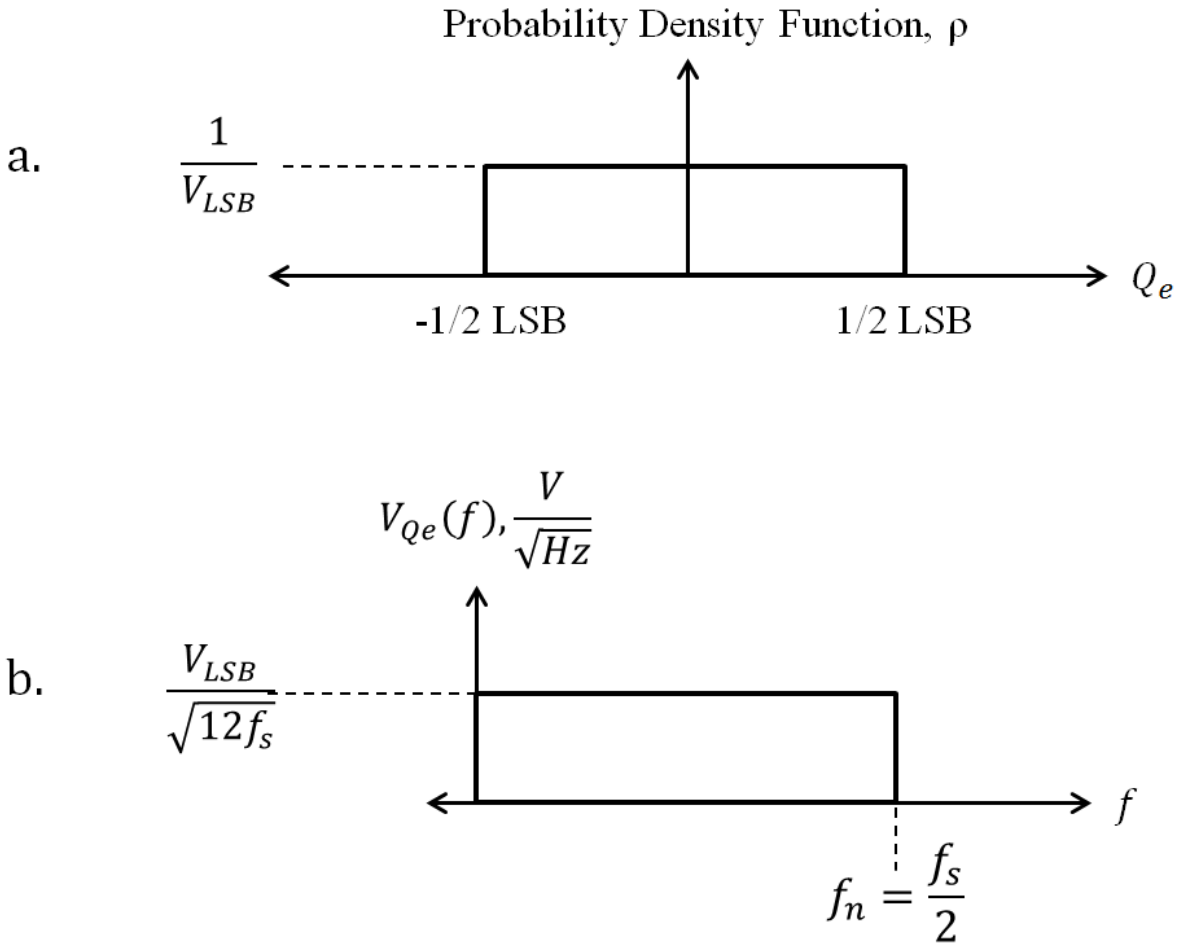


Figure 1.1 – (a) Probability density function and (b) quantization noise spectral density.

The power of the RMS quantization noise, $\frac{V_{LSB}}{\sqrt{12}}$, depends on the amplitude of V_{LSB} which is constant for a given data converter resolution. Stated another way, the area under the function in Fig 1.1b is always the same regardless of the bandwidth. However, as the Nyquist frequency is increased, the amplitude of the quantization noise is proportionally reduced. This is illustrated in Fig. 1.2. It is important to note that in order for the integral to give the correct answer, a factor of two must be used to account for the negative frequencies as in Eq. 1.5. However intuitively it is clear that doubling the sampling frequency halves the amplitude of the quantization noise voltage. Clearly increasing the

sampling frequency alone does not reduce the quantization noise of an ADC. The spectrum also needs to be bandlimited with a filter in order to actually reduce the quantization noise.

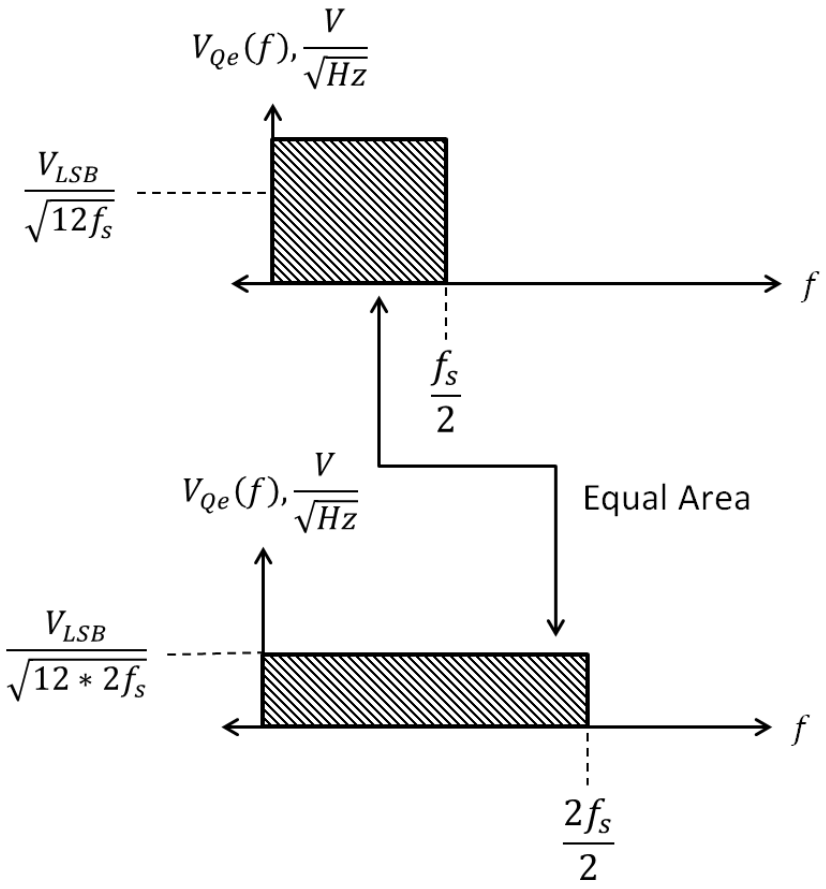


Figure 1.2 – Effect of increasing sampling frequency on quantization noise spectral density.

After oversampling, the digital output signal needs to be filtered to bring the bandwidth back down to the original desired Nyquist rate. An example for 2X oversampling is shown in Fig. 1.3. After the signal is oversampled by 2X, an ideal low-pass filter is used to halve the quantization noise. In reality, this extent of noise reduction is not possible since an ideal low-pass filter is unrealizable. High-order analog filters are also difficult to realize,

therefore in practical data converters usually some type of high-order digital filter is used. The quantization noise directly relates to the resolution of the data converter.

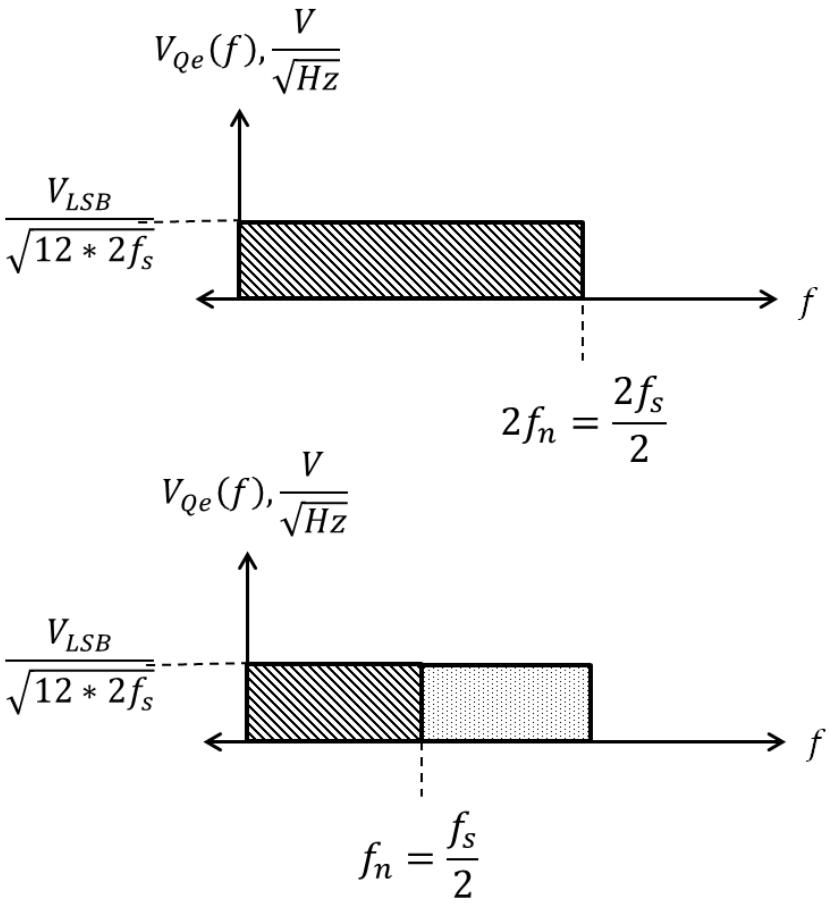


Figure 1.3 – Bandlimiting an oversampled signal.

The resolution of a data-converter is calculated from the signal-to-noise ratio (SNR). This is the effective resolution and not the nominal resolution. An ADC can be nominally described as an *n*-bit ADC if it outputs an *n*-bit word. However, this doesn't mean that the ADC can actually resolve a signal to that resolution. The term for the actual resolution of a data converter is effective number of bits (ENOB). The ideal SNR is given by

$$SNR_{ideal} = 20 * \log \frac{V_p/\sqrt{2}}{V_{LSB}/\sqrt{12}} = 20 * \log \frac{2^N\sqrt{12}}{2\sqrt{2}} = (6.02N + 1.76)dB \quad (1.7)$$

Where n is the number of bits and Vp is the maximum amplitude that can be applied to the ADC. Rewritten from Eq. 1.7, the effective number of bits is given by

$$N_{eff} = \frac{SNR-1.76}{6.02} \quad (1.8)$$

The SNR can be either an ideal SNR, as is the case when assuming quantization noise only, or a measured SNR from actual test equipment. Generally, measured SNR can be quite lower than the theoretical ideal SNR.

Oversampling and band-limiting the signal increases SNR and thus the ENOB. For simple oversampling, Eq. 1.6 is modified to

$$V_{qe}(f) = \frac{V_{LSB}}{\sqrt{K*12*2*f_n}} \quad (1.9)$$

where K is the oversampling ratio and f_n is the Nyquist frequency or desired bandwidth of the input signal. The variable for sampling rate in Eq. 1.6 has been replaced with $2 * f_n$ for clarity since the actual sampling rate is OSR-times higher.

Noise-shaping

The problem with simple oversampling is that a very high oversampling ratio is required to get a significant increase in resolution. For example, a 1-bit ADC would need an OSR of 2^{16} (65536) just to have an 8-bit resolution. For example, a 1 MHz bandwidth signal

would require a sampling rate of 65 GHz, which is unfeasible. Instead, sigma-delta ADCs must combine noise-shaping with oversampling to get high resolutions. Noise-shaping is simply the use of a filter to shift quantization noise to frequencies outside the signal bandwidth of interest. This principle allows a sigma-delta ADC to achieve much higher resolution with a given OSR than otherwise possible.

The RMS quantization noise $V_{Qe,RMS}$ remains the same for a given sampling rate. However, with noise-shaping, the spectral density function shifts to higher frequencies. This is illustrated in Fig. 1.4c. For comparison, Fig 1.4a illustrates Nyquist rate sampling and Fig 1.4b illustrates simple oversampling. In all three cases, the total areas under the spectral density functions are the same, but the quantization noise in the bandwidth of interest in Figs 1.4b and 1.4c is reduced. In this case, the noise-shaping shown has a high-pass characteristic. The transfer function of this type of filter differentiates the quantization noise causing most of the energy to be concentrated at higher frequencies.

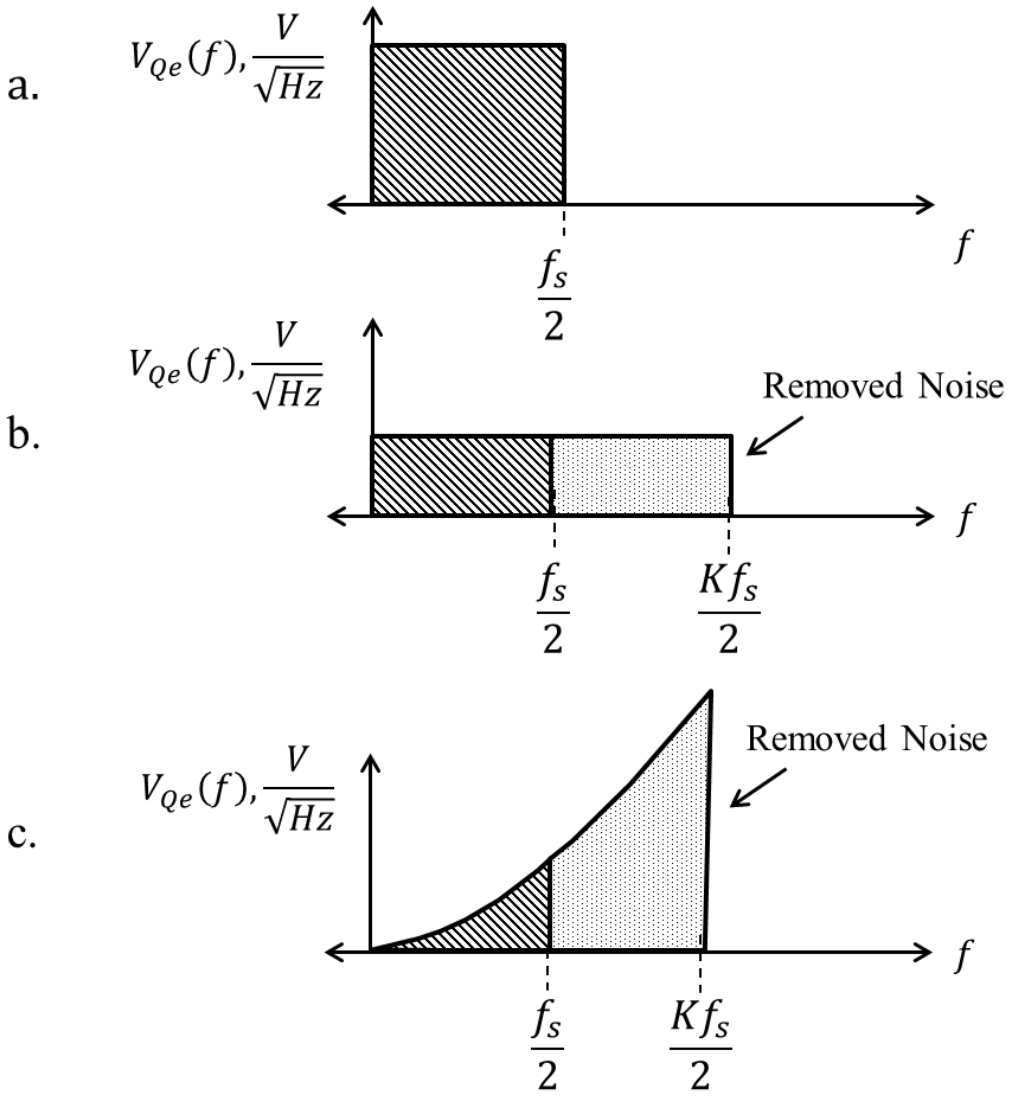


Figure 1.4 – Comparison of quantization noise for (a) Nyquist rate, (b) simple oversampling and (c) noise-shaping.

The shape of the spectral density curve is determined by the order of the noise-shaping. The simplest case is that of 1st-order noise-shaping which displays a 10dB per decade rise in the noise voltage amplitude until the oversampled Nyquist frequency, $Kf_s/2$. For passive sigma delta ADCs, noise-shaping is generally limited to 2nd-order. For active sigma-delta topologies stability issues come into play after 2nd-order, although 4th order

designs and beyond are now common [5]. A comparison of 1st and 2nd order noise-shaping is shown in Fig. 1.5. The quantization noise in the region of interest is lower for the 2nd order curve; however the trade-off is higher quantization noise at higher frequencies. Since all frequencies beyond the Nyquist frequency are filtered out, this noise does not matter.

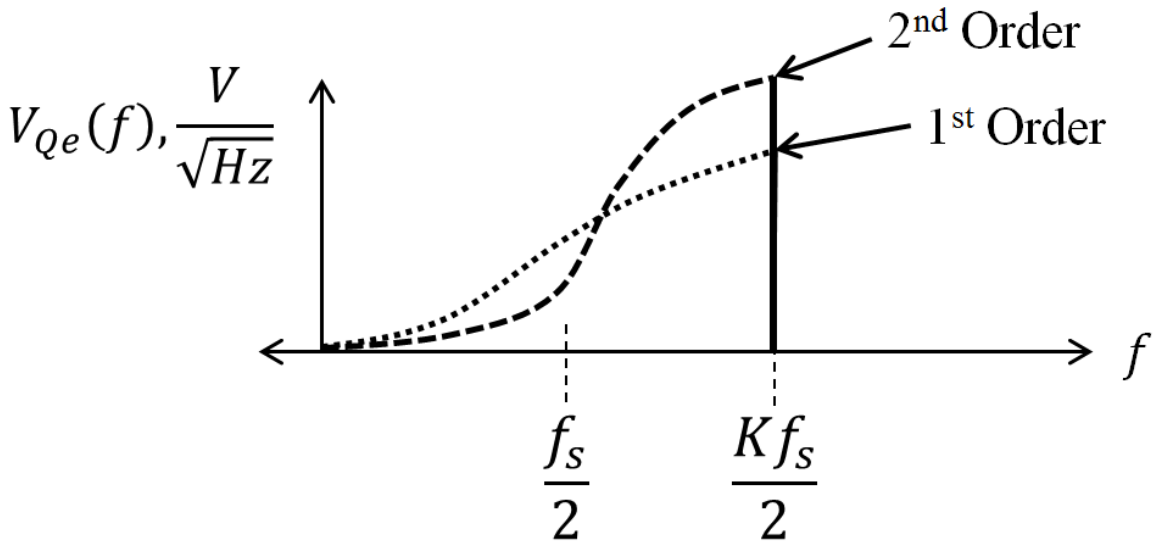


Figure 1.5 – Comparison of 1st and 2nd order noise-shaping.

Sigma Delta Principles

Sigma-delta ADCs are pervasive in almost all high resolution, low to medium speed data conversion applications. Despite this, many individuals find it difficult to understand the basic operation of sigma-delta ADCs. It is beneficial to examine the qualitative operation of a sigma-delta modulator before delving into detailed theory. A system-level block diagram of a sigma-delta modulator is shown in Fig. 1.6. There are four basic components to this diagram. These are a summing junction, an integrator, a 1-bit quantizer, and a 1-bit digital-to-analog converter (DAC). These components form a classical feedback

system, although there are additional caveats to treating a sigma-delta modulator as a linear system due to the fact that the quantizer and DAC are fundamentally nonlinear components [6]. The function of the summing block is to create an error signal, which is the difference between the input and output voltages. The integrator then sums these differences together. The 1-bit quantizer compares the integral of the error signal with a fixed reference voltage. The output of the quantizer is a "1" if the integral of the error signal is larger than the reference voltage. Otherwise the output is a "0". This bit-stream is a digital representation of the analog input. Understanding why this is a valid representation requires following an analog input signal through each block in the system.

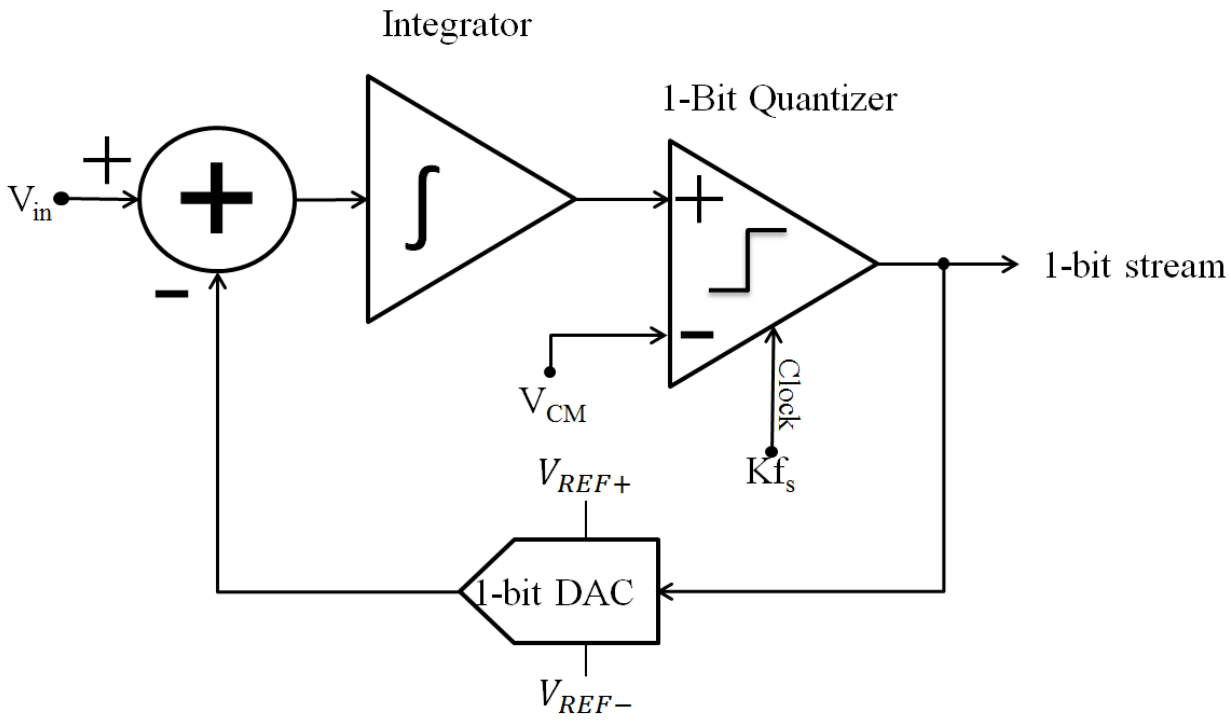


Figure 1.6 – System level block diagram.

If a static analog signal (DC) is applied to the input of the sigma-delta modulator in Fig. 1.6, after a certain period of time, the average value of the bit-stream will represent the

value of the analog input. Before proceeding with how this occurs, some constraints for the system must be defined. The system has a maximum full scale input range ($V_{REF+} - V_{REF-}$). In a practical circuit these are usually assumed to be the power supply rail voltage and ground. The common-mode voltage V_{CM} is generally set to be half of the full scale input range. For example, a circuit with a power supply voltage of 5V would have a 2.5V common-mode voltage. The signal swing for all components in the system is between 0V and 5V.

The seemingly random output of the sigma-delta modulator makes time domain analysis difficult. However if the data is averaged, then a meaningful result can be obtained. If an input of 2.5V is applied to the system in Fig. 1.6 with a 5V V_{REF+} and a 0V V_{REF-}, then the output of the sigma-delta modulator will have an equal amount of zeros and ones on average. This output waveform is shown in Fig 1.7. Each time the integrator output crosses 2.5V with a positive or negative slope, the comparator outputs either a one or zero respectively.

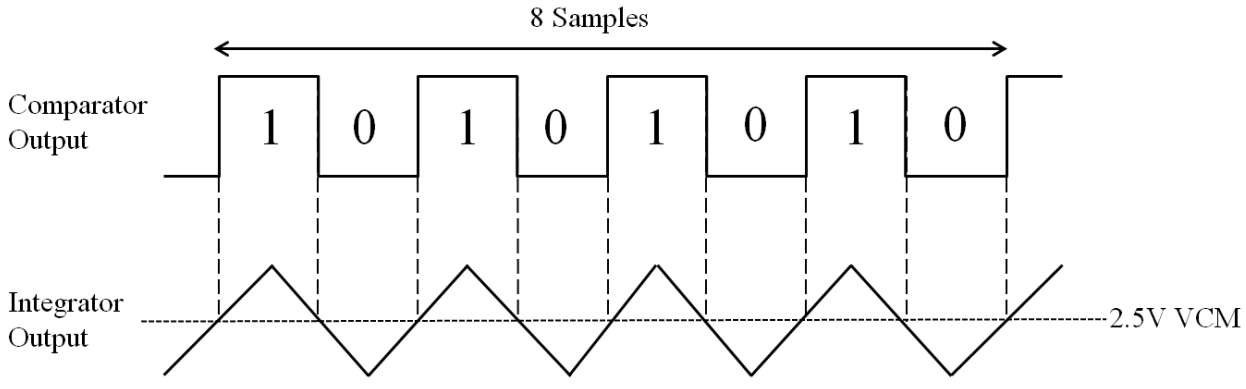


Figure 1.7 – Comparator and integrator outputs.

If 8 samples are averaged from the modulator output, then the average value is $\frac{4}{8} = 0.5$. Multiplying the average value by the full scale input value of 5 V does indeed result in the input voltage of 2.5 V. Had the input voltage been higher than 2.5 V, then there would be a correspondingly higher average value. Had the input voltage been lower, then there would be a lower average value. Simply stated, the average value of the output represents the input value. The resolution of the ADC can be increased by increasing the number of samples. This is simple averaging and for N-bits of resolution, 2^N samples are required. The example in Fig. 1.7 has 3 bits of resolution. Obviously the number of samples becomes prohibitive for high resolutions because this example does not take noise-shaping into account. It is not productive to examine noise-shaping in the time domain and a frequency domain model is required.

The sigma-delta modulator is in a broader category known as feedback modulators [7]. A block diagram of a feedback modulator is shown in Fig. 1.8. The summing junction on the left is where the feedback signal is subtracted from the input in order to create the error signal. The error signal is fed into an analog filter, $A(f)$, before going into the next stage, an ADC. The ADC is fundamentally a nonlinear device but in order to use classical linear systems theory, it is instead modeled as a summing junction where the quantization noise is added to the input signal. The next stage is a digital filter, $B(f)$, which filters the digital output before feeding it into the DAC which converts the signal back to analog.

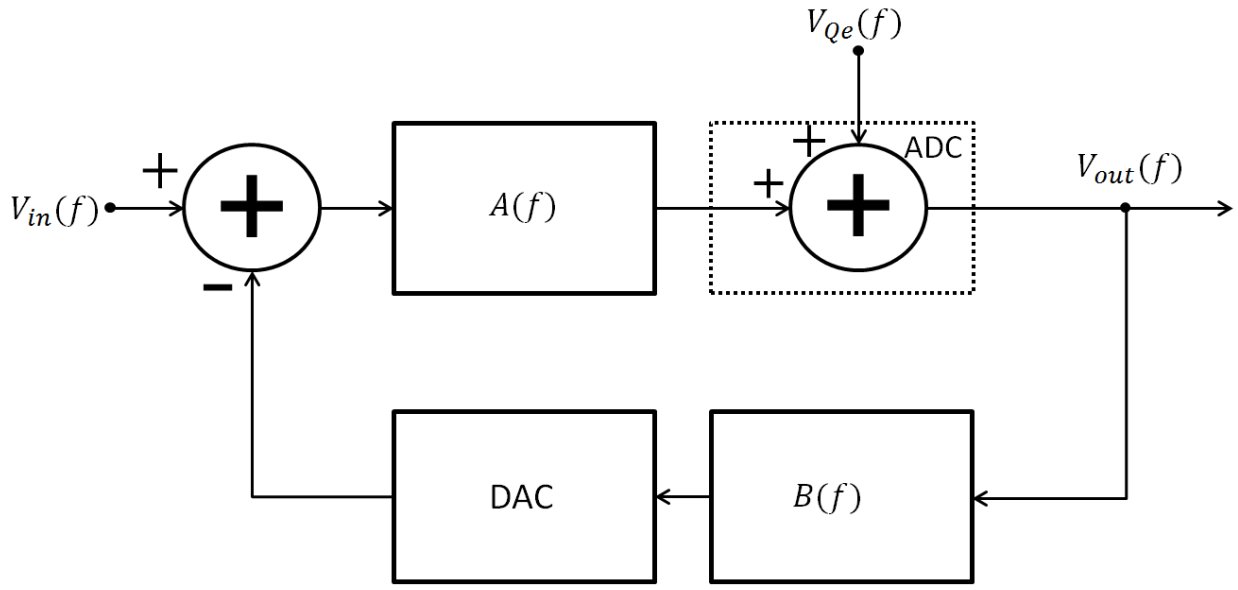


Figure 1.8 – Block diagram of feedback modulator.

The sigma-delta topology simplifies this general feedback modulator diagram by setting $B(f)$ to one. The ADC has a 1-bit resolution and is usually either a comparator or a D flip-flop (DFF). The 1-bit DAC is either an inverter or the complementary output from the ADC. With these simplifications the output can be given in terms of the input and quantization error as

$$v_{out}(f) = \frac{A(f)}{1+A(f)*1} * v_{in}(f) + \frac{1}{1+A(f)*B(f)} * V_{Qe}(f) \tag{1.10}$$

The signal transfer function (STF) is the term multiplying $v_{in}(f)$ and is written alone as

$$STF = \frac{A(f)}{1+A(f)*1} \tag{1.11}$$

The noise transfer function (NTF) is the term multiplying $V_{Qe}(f)$ and is written alone as

$$NTF = \frac{1}{1+A(f)*B(f)} \tag{1.12}$$

The forward path, $A(f)$, is an integrator with a low-pass filter characteristic. The gain in the passband of the filter is large which results in an STF of nearly unity. Conversely, the NTF displays a high-pass characteristic and ideally approaches zero in the same region. This is how the quantization noise is reduced in the bandwidth of interest.

Chapter 2 Passive Sigma-Delta Modulators

Transfer Function Derivations

In order to approach the theoretical ideal performance for a sigma-delta modulator, an active integrator is typically employed for the integration function in the forward path. This uses active electronic amplifiers which generally have a quiescent current draw that is constant. The other components in a sigma-delta ADC only draw current when actively switching between high and low states. One way of reducing the power consumption of a sigma-delta modulator is to reduce the clock frequency. However this does not reduce the power consumption of the active integrator portion of the modulator and consequently the active integrator becomes responsible for a significant percentage of the total power consumption. Replacing the active integrator with a passive version can eliminate this portion of the power consumption at the expense of resolution. To examine why a passive integrator has reduced resolution requires a detailed analysis of a passive sigma-delta modulator.

The simplest possible version of a sigma-delta modulator using ideal components is shown in Fig. 2.1A. The one bit ADC is a comparator and the one bit DAC is an inverter. The values of the resistors are the same in order to keep the gain of the circuit at unity. This schematic can be redrawn as the block diagram shown in Fig. 2.1B. The ADC is replaced with a summing junction where quantization noise is added. The DAC is replaced with a multiply by -1. The output of the modulator is given by

$$V_{Qe}(f) + v_{int}(f) = v_{out}(f) \tag{2.1}$$

Where v_{int} is the voltage at the capacitor node. Next, nodal analysis can be used to rewrite v_{int} in terms of the currents flowing into the node. There are two currents flowing into this node, the current from the input and the feedback current. The feedback current has a negative polarity due to the inverter.

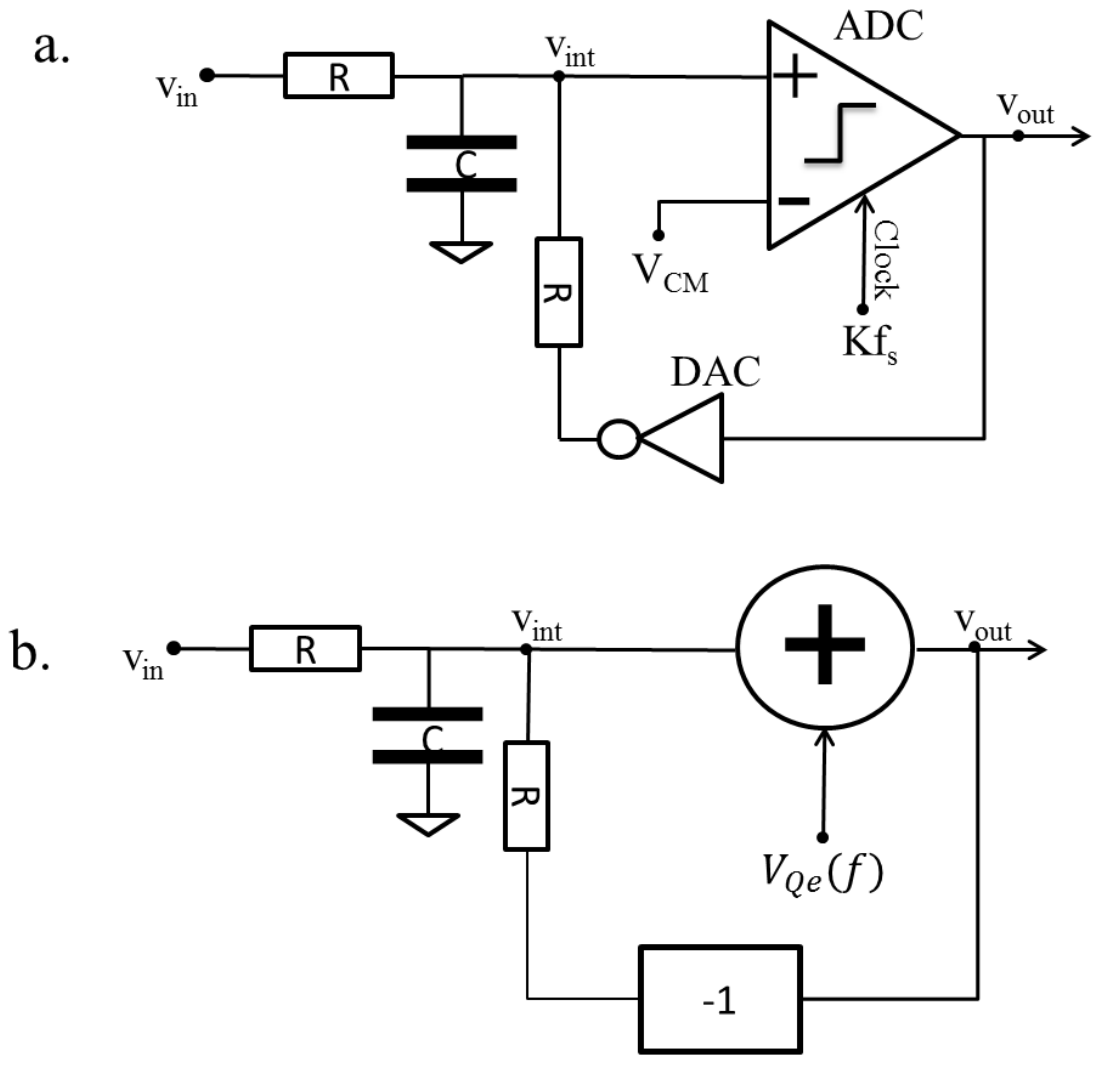


Figure 2.1 – Circuit (a) and block diagram and (b) schematic of 1st order passive sigma-delta modulator.

The sum of these two currents is given by,

$$i_{int} = \frac{v_{in} - v_{int}}{R} + \frac{-v_{out} - v_{int}}{R} \tag{2.2}$$

This current is then multiplied by the impedance of the capacitor to give a voltage,

$$v_{int} = \left(\frac{v_{in} - v_{int}}{R} + \frac{-v_{out} - v_{int}}{R}\right) * \frac{1}{j\omega C} \tag{2.3}$$

Substituting this into Eq. 2.1 results in

$$V_{Qe}(f) + \left(\frac{v_{in} - v_{int}}{R} + \frac{-v_{out} - v_{int}}{R}\right) * \frac{1}{j\omega C} = v_{out}(f) \tag{2.4}$$

The transfer function can be found by rearranging the terms

$$v_{in} - v_{out} - 2v_{int} + V_{Qe} * J\omega RC = j\omega RC * v_{out} \tag{2.5}$$

$$v_{in} - 2v_{int} + V_{Qe} * J\omega RC = v_{out}(j\omega RC + 1) \tag{2.6}$$

This then yields,

$$v_{out} = \frac{1}{1 + j\omega RC} v_{in} + \frac{j\omega RC}{1 + j\omega RC} V_{Qe} + \frac{-2 * v_{int}}{1 + j\omega RC} \tag{2.6}$$

Breaking down this equation gives the STF, NTF, and an extra noise/distortion term.

$$STF = \frac{1}{1 + j\omega RC} \tag{2.7}$$

$$NTF = \frac{j\omega RC}{1 + j\omega RC} \tag{2.8}$$

$$Distortion = \frac{-2 * v_{int}}{1 + j\omega RC} \tag{2.9}$$

It is clear from these equations that the STF displays a 1st order low-pass filtering characteristic and the NTF displays a 1st order high-pass filtering characteristic. For a continuous time sigma-delta modulator there is an inherent anti-aliasing filter. The distortion term is the result of the voltage varying at the v_{int} node. With an active integrator this term is negligible because the amplifier attempts to keep the node voltage constant. The key limit to the resolution of a passive modulator is the distortion term. Deriving an equation for the resolution of a passive sigma delta modulator is difficult with the distortion term included. Instead, an equation for an ideal active sigma delta modulator is used with a constraint. The ideal SNR of a 1st order sigma-delta modulator is given by

$$SNR_{ideal} = 20\log\frac{{V_p}/{\sqrt{2}}}{V_{noise,RMS}} = 6.02N + 1.76 - 20\log\frac{2\pi RCf_s}{\sqrt{12}} + 20\log K^{3}/_{2} \quad (2.10)$$

The derivation for this equation is found in [7]. For a passive modulator the time constant for RC needs to be significantly larger than the period of the sampling clock in order for this equation to be valid. If RC is set to $4.4/T_s$, then Eq. 2.10 becomes

$$SNR_{ideal} = 6.02N + 1.76 - 18.06 + 30\log K \quad (2.11)$$

Rewriting this equation in terms of the number of bits of increased resolution yields

$$N_{inc} = \frac{30\log K - 18.06}{6.02} \quad (2.12)$$

$$SNR_{ideal} = 6.02(N + N_{inc}) + 1.76 \quad (2.13)$$

For every doubling of K beyond 4 there is a 1.5 bit increase in resolution which is 0.5 bits greater than with simple oversampling. In order to increase the ratio of resolution increase to oversampling, the order of the noise shaping should be increased to 2nd order.

A conventional passive 2nd-order sigma-delta modulator requires two feedback paths. The schematic of this circuit is shown in Fig. 2.2. This circuit has two feedback paths and does not have a set common mode voltage. Instead, the circuit acts to drive both capacitor nodes to the same value. A detailed description of this topology is found in [8].

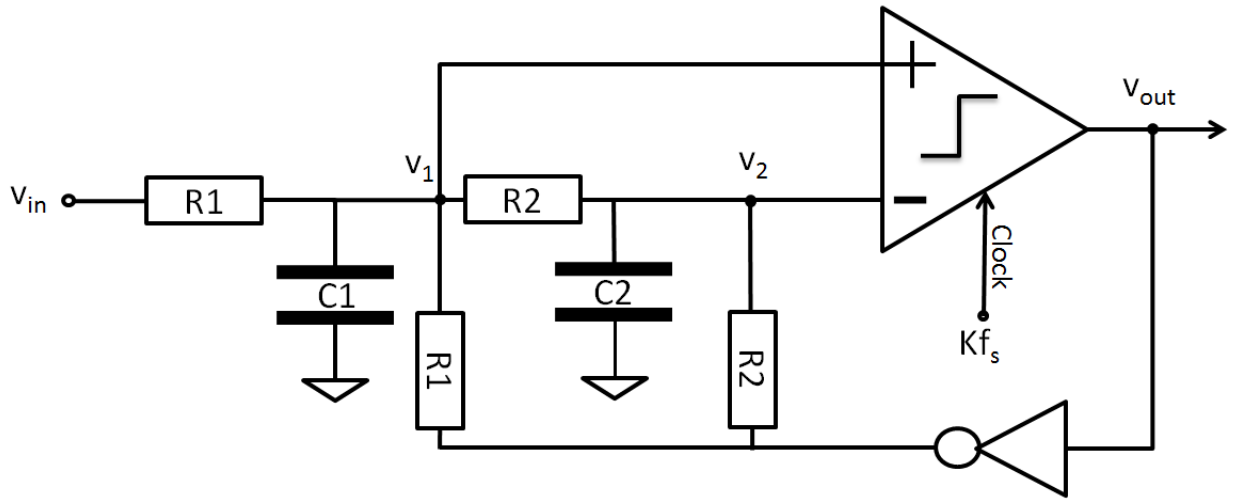


Figure 2.2 – Schematic of 2nd order passive sigma-delta modulator.

The output equation of this circuit in terms of the input signal and quantization noise is given by,

$$v_{out}{}^2 = \frac{1}{1+(\omega RC)^2} \cdot v_{in}{}^2 + \frac{(\omega RC)^2}{1+(\omega RC)^2} \cdot \frac{V_{Qe}{}^2}{2} + \frac{2v_1+v_2}{1+(\omega RC)^2} \qquad (2.14)$$

The output is squared because of the way this 2nd- order equation was solved. This form also preserves the standard form for the transfer functions which allows direct comparisons to be made to the 1st-order modulator. Breaking the equation down, the STF, NTF and distortion terms are given by

$$STF = \frac{1}{1+(\omega RC)^2} \tag{2.15}$$

$$NTF = {}^{1}/_{2} * \frac{(\omega RC)^2}{1+(\omega RC)^2} \tag{2.16}$$

$$Distortion = \frac{2v_1+v_2}{1+(\omega RC)^2} \tag{2.17}$$

Each transfer function is similar to that of the 1st-order sigma-delta modulator except that they are 2nd-order. A striking difference though is that the quantization noise power is cut in half. The ideal SNR can be solved as

$$SNR_{ideal} = 6.02N + 1.76 - 15.13 + 30\log K \tag{2.18}$$

This equation verifies that the noise power is halved (3dB reduction) over the 1st-order modulator. In practice, a 2nd-order modulator offers a much higher performance increase than apparent from the ideal SNR equations. The reason for this is because of limitations and assumptions used in the linear model. Actual circuit simulations and measurements can show significantly different results although the general trends are still valid. This will become apparent in later chapters.

Performance can be significantly improved by using a modified passive 2nd order topology. This design simply adds an additional RC loop filter to the passive 1st order

circuit. The schematic of the modified passive 2nd order circuit is shown in Fig. 2.3. On the surface, a big benefit of this is that there is just one feedback path and only two resistors need to be reasonably matched. Resistors R1 need to be matched but R2 can be a different value and not affect the gain of the circuit. Likewise, C1 and C2 do not need to be matched either. This allows a wide range of values that can be used in the circuit. Analyzing the transfer function and simulations show that performance is maximized when certain constraints are applied to component values.

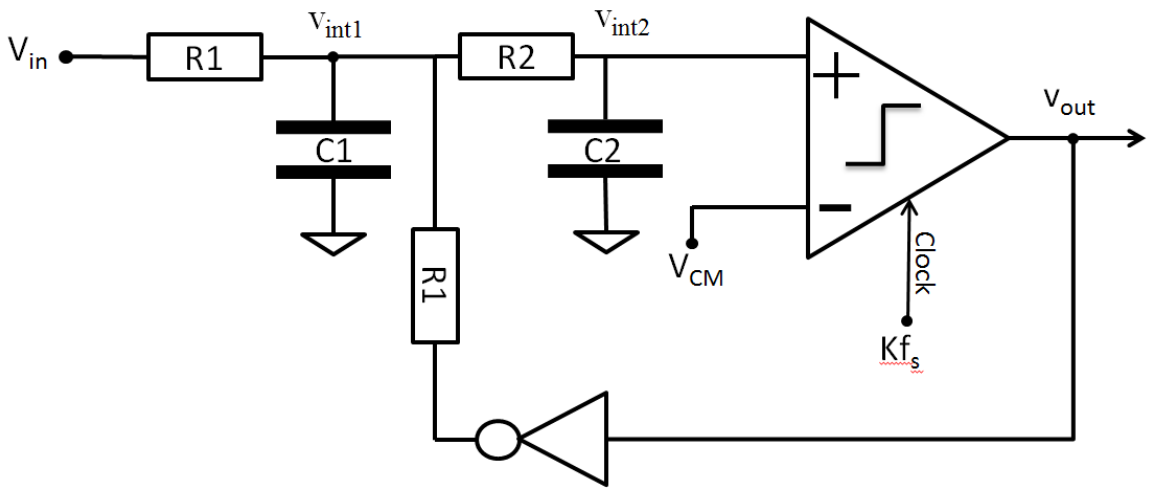


Figure 2.3 – Schematic of modified 2nd order passive sigma-delta modulator.

Due to the high number of variables, it is difficult to derive the transfer function of the modified 2nd order sigma-delta modulator. First the circuit needs to be converted into a block diagram as in Fig. 2.4. The RC filters have been replaced with their equivalent frequency domain transfer function. Although there is a system level diagram it can be convenient to use both schematics to derive the transfer function.

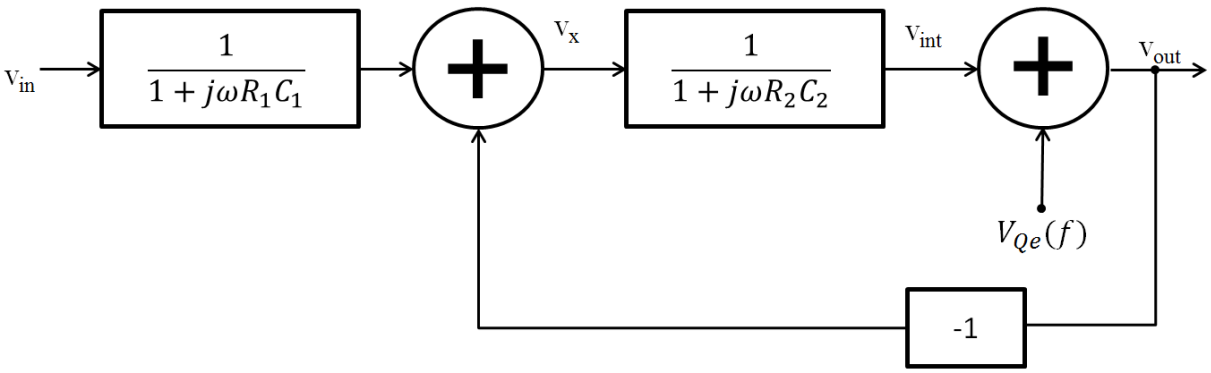


Figure 2.4 – Block diagram of modified 2nd order passive sigma-delta modulator.

Using nodal analysis the current flowing out of the summing junction at the v_x node is

$$\frac{v_{in}-v_x}{R_1}+\frac{-v_{out}-v_x}{R_1}=\frac{v_x}{1/j\omega C} \tag{2.19}$$

This can be rearranged as

$$\frac{v_{in}-2v_x-v_{out}}{R1}=v_x*j\omega C \tag{2.20}$$

Solving for v_x

$$v_x=\frac{v_{in}-v_{out}}{R_1*j\omega C_1+2} \tag{2.21}$$

The output voltage, v_{out} can be written in terms of

$$v_{out}=V_{Qe}+v_x*\frac{1}{1+j\omega R_2C_2} \tag{2.22}$$

Substituting v_{int1} results in

$$v_{out} = V_{Qe} + \left(\frac{v_{in}-v_{out}}{R_1 * j\omega C_1 + 2}\right) * \frac{1}{1+j\omega R_2 C_2} \tag{2.23}$$

These equations can be solved using Mathematica to give v_{out} in terms of v_{in}, V_{Qe}, and v_{int}

$$v_{out} = \frac{1+sR_2C_2}{1+sR_2C_2+sR_1C_1} \cdot v_{in} + \frac{s(sR_1C_1R_2C_2+R_1C_1)}{1+sR_1C_1+s^2R_1C_1R_2C_2} \cdot V_{Qe} + \frac{1}{1+sR_1C_1+(1+sR_2C_2)} \cdot v_{int} \tag{2.24}$$

The STF, NTF and DTF are

$$STF = \frac{1+sR_2C_2}{1+sR_2C_2+sR_1C_1} \tag{2.25}$$

$$NTF = \frac{s(sR_1C_1R_2C_2+R_1C_1)}{1+sR_1C_1+s^2R_1C_1R_2C_2} \tag{2.26}$$

$$DTF = \frac{1}{1+sR_1C_1+(1+sR_2C_2)} \tag{2.27}$$

From examining the transfer functions a few things become apparent. The signal transfer function is 1st order meaning that input signals are filtered by a simple 10 dB per decade low-pass filter. The noise transfer function is indeed 2nd order which allows this topology to be classified as a 2nd order sigma delta modulator [9]. The distortion transfer function is also 1st order and is not multiplied by two like the first order and conventional second order topologies. This means that distortion should nominally be halved with the modified second order topology. The fact that there are 2 different RC filters allows a

significant range of choices. A design methodology needs to be developed to select optimal values for the passive components.

This can be done by plotting all the transfer functions and examining how they change with different component values. For example, R1 can be at a fixed value and R2 can be varied and the transfer function examined. This was done in Mathematica and the Bode plot of the signal transfer function is shown in Fig 2.5. The transfer function exhibits a 1^{st} order roll off until reaching an amplitude value where it flattens out. For each decade decrease in R2 value, the amplitude where the curve flattens out is reduced by 20 dB. The corner frequency for the STF is not affected at all by varying R2. If R2 remains fixed and R1 is varied the resulting bode plot is as shown in Fig. 2.6. The corner frequency does indeed change when R1 is varied. The amplitude then flattens out at a certain frequency, indicating an all-pass characteristic. The phase plot confirms that there is indeed a form of all-pass behavior. If R1 and R2 are varied in opposite directions, then the amplitude and phase plots shown in Fig. 2.7 are the result. Again, the all-pass characteristic is visible. The STF plots will need to be taken into account when designing a modulator for a particular input signal range but they don't reveal much about the actual performance of this topology. For that, the NTF needs to be examined.

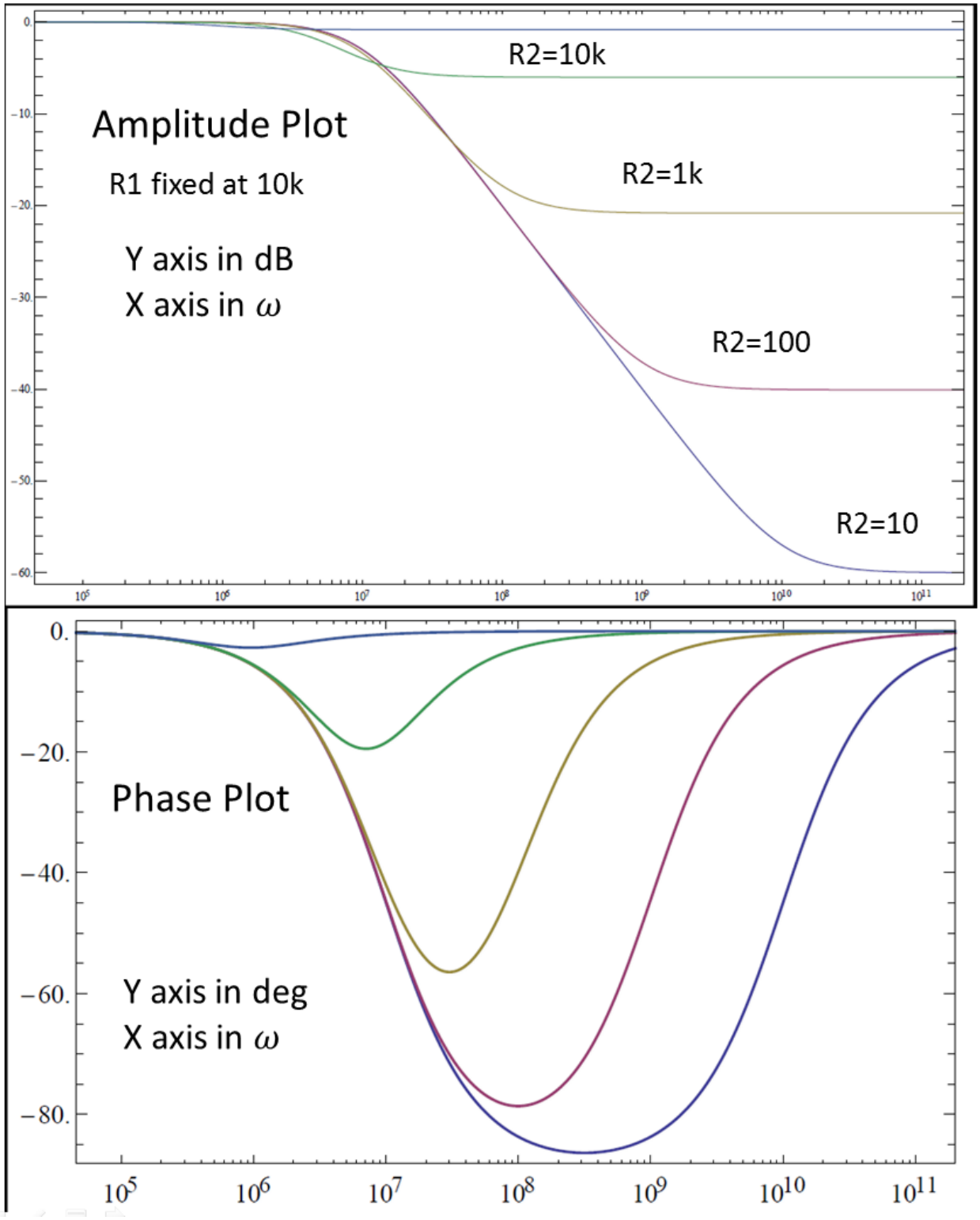


Figure 2.5 – Bode plot of STF with fixed R1 and varying R2.

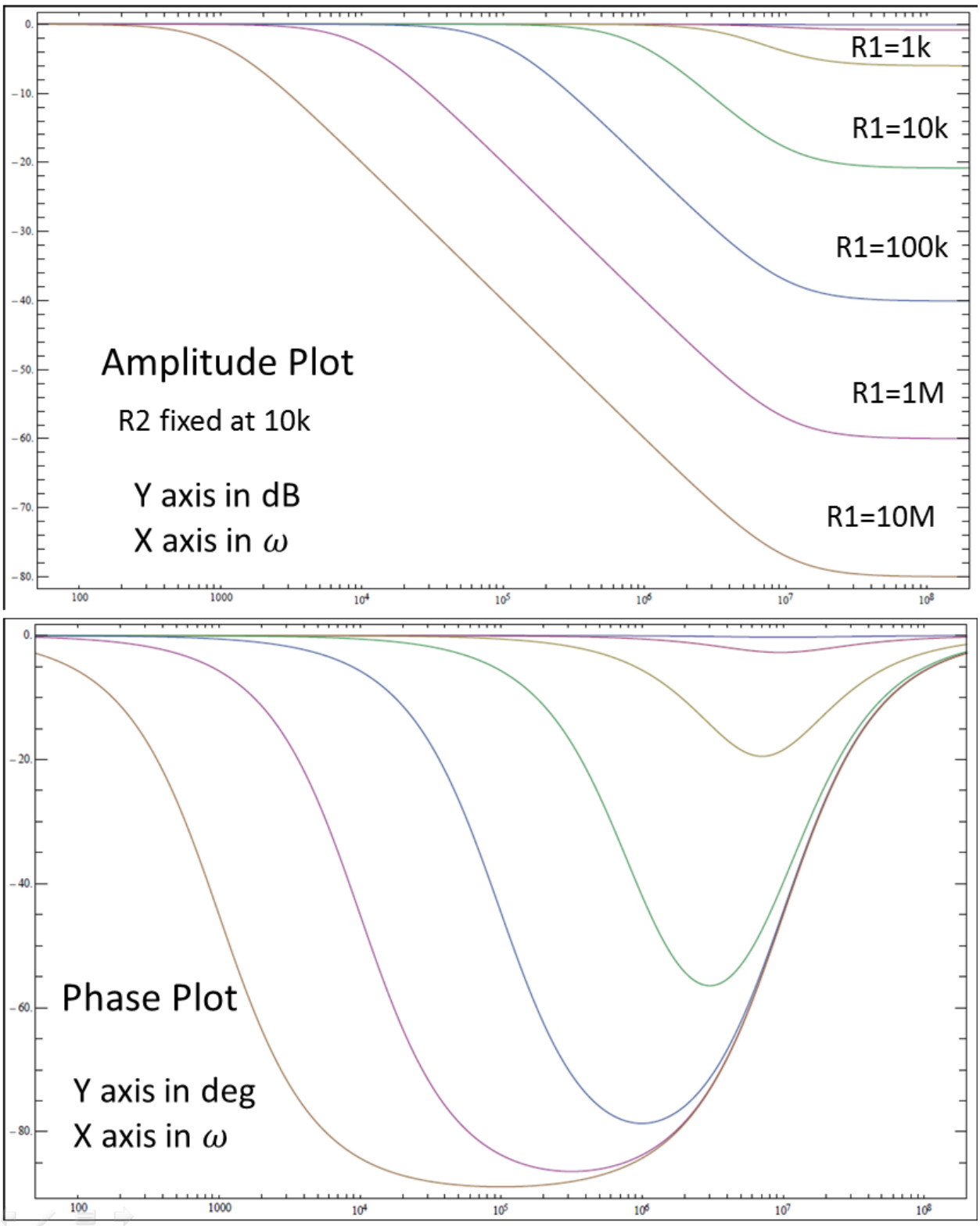


Figure 2.6 – Bode plot of STF with fixed R2 and varying R1.

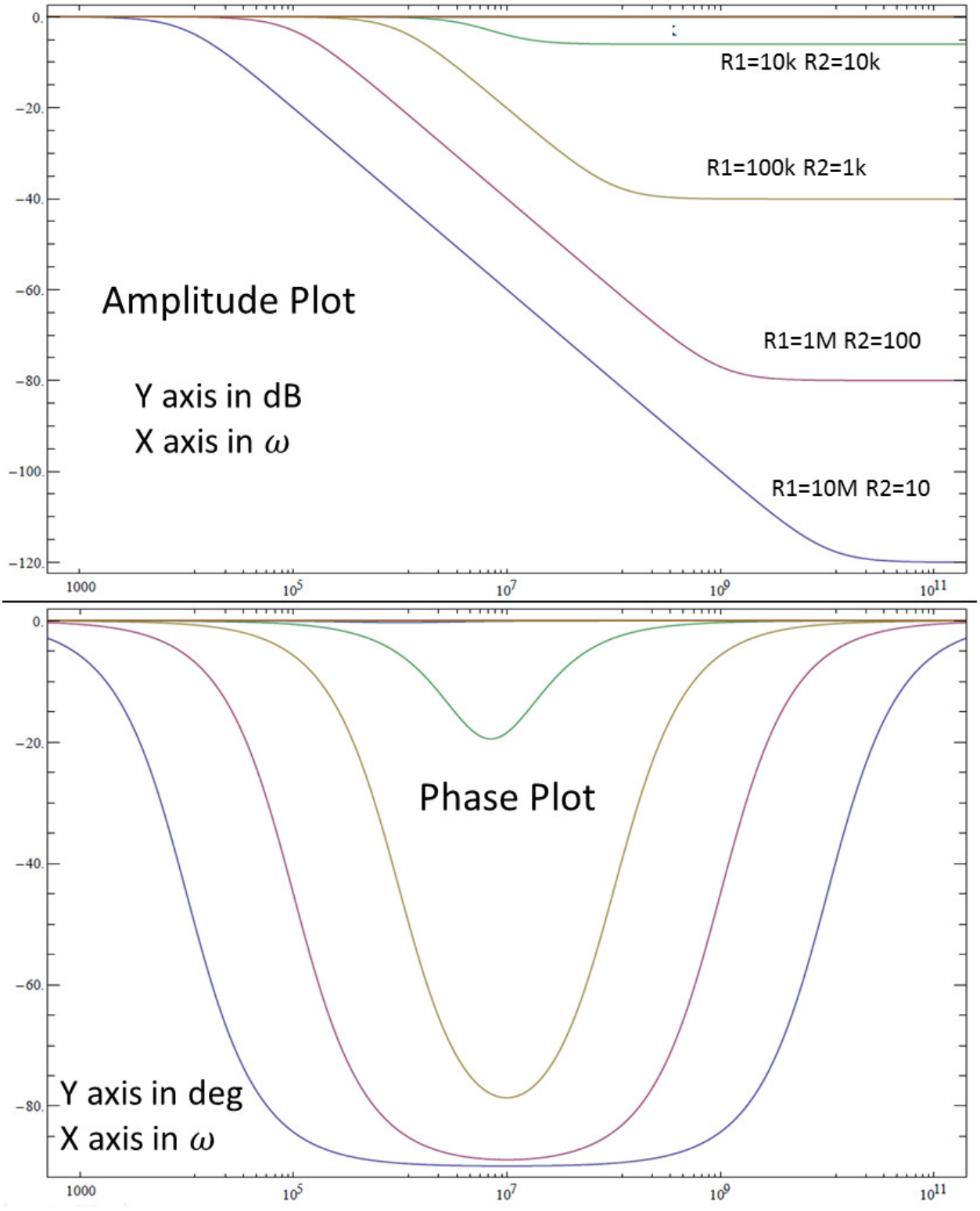


Figure 2.7 – Bode plot of STF with R1 and R2 varying in opposite directions.

The next three figures, Fig. 2.8, Fig. 2.9 and Fig, 2.10 all illustrate what occurs to the NTF as the resistor values are varied. The method of judging these plots is by examining the amount of noise at the lower frequencies which are in the signal bandwidth of interest. In Fig. 2.8, R1 is held constant while R2 is varied. From this plot, it is apparent that there is some sort of resonant behavior occurring and that perhaps it is best to have the value of R2 maximized. However, the next plot in Fig. 2.9 seems to indicate that R1 should also be minimized. Finally, examining Fig. 2.10, it is apparent that the value of R1 should be as low as possible and the value of R2 should be as high as possible, given the constraint of desired signal bandwidth. The actual total noise power throughout the bandwidth is the same for all values. However, it appears that noise is shifted to a resonant peak which results in much lower quantization noise at lower frequencies of interest. This shifting of noise to a resonant peak is the mechanism by which this sigma-delta modulator topology achieves its higher resolution compared to standard passive designs.

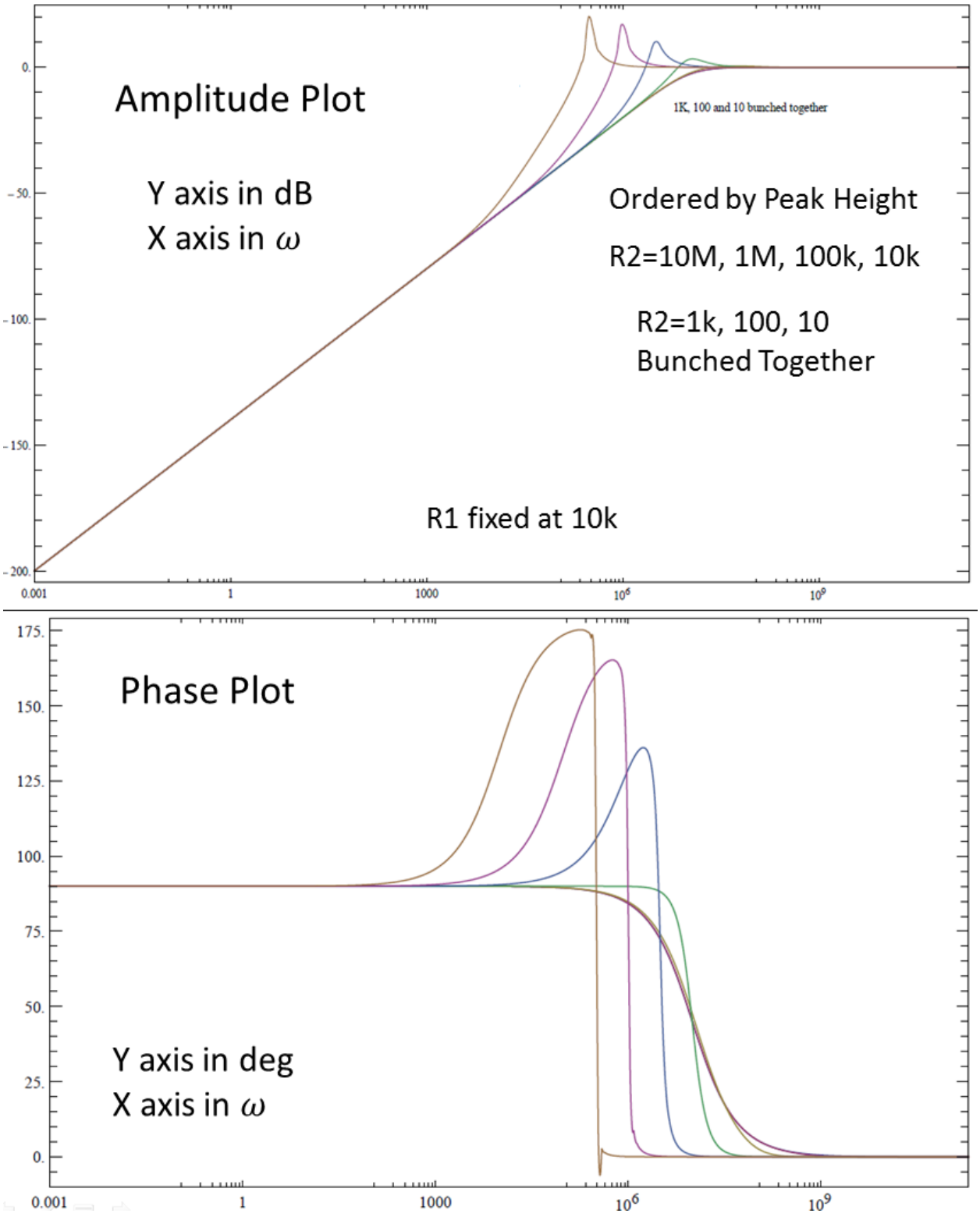


Figure 2.8 – Bode plot of NTF with fixed R1 and varying R2.

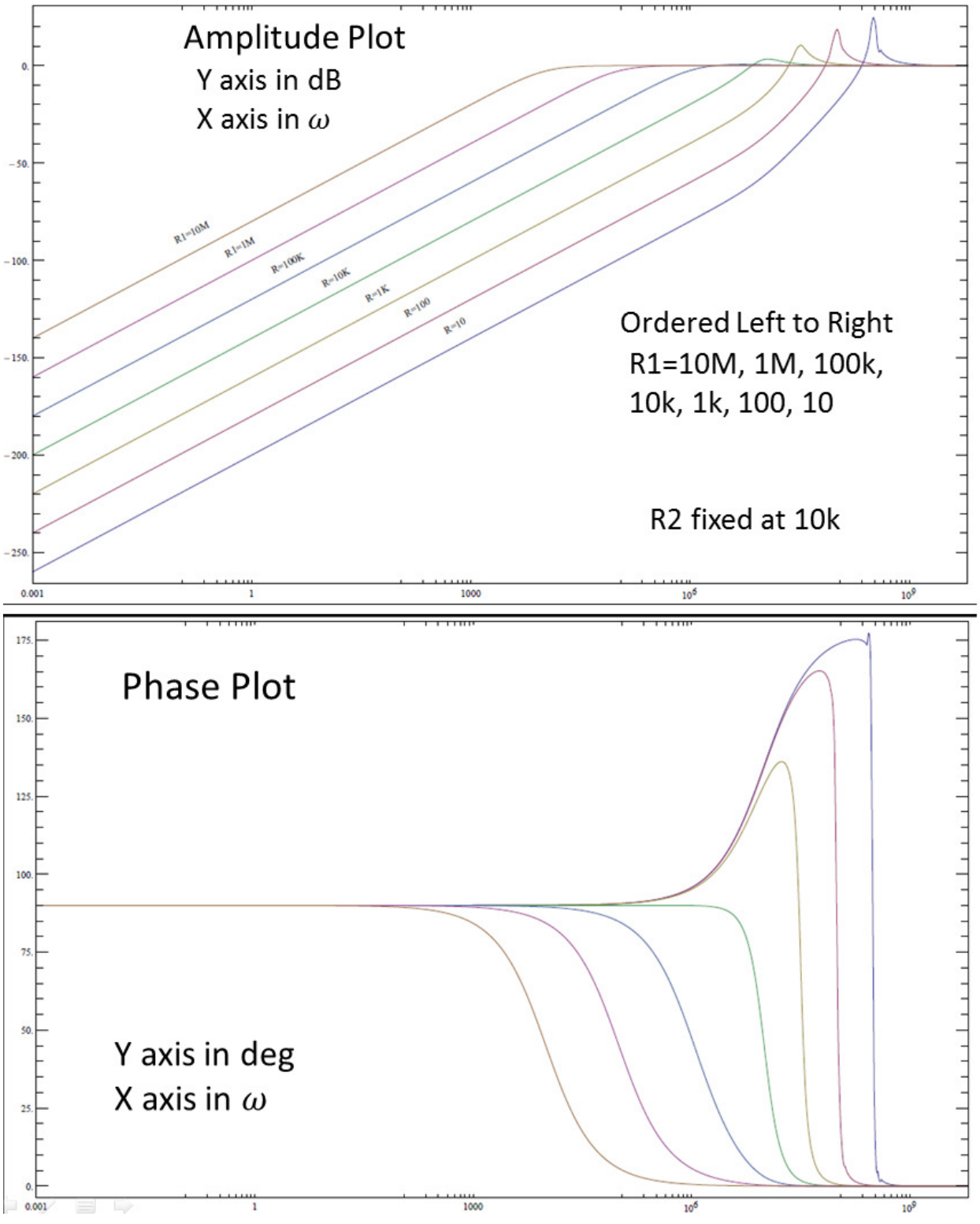


Figure 2.9 – Bode plot of NTF with fixed R2 and varying R1.

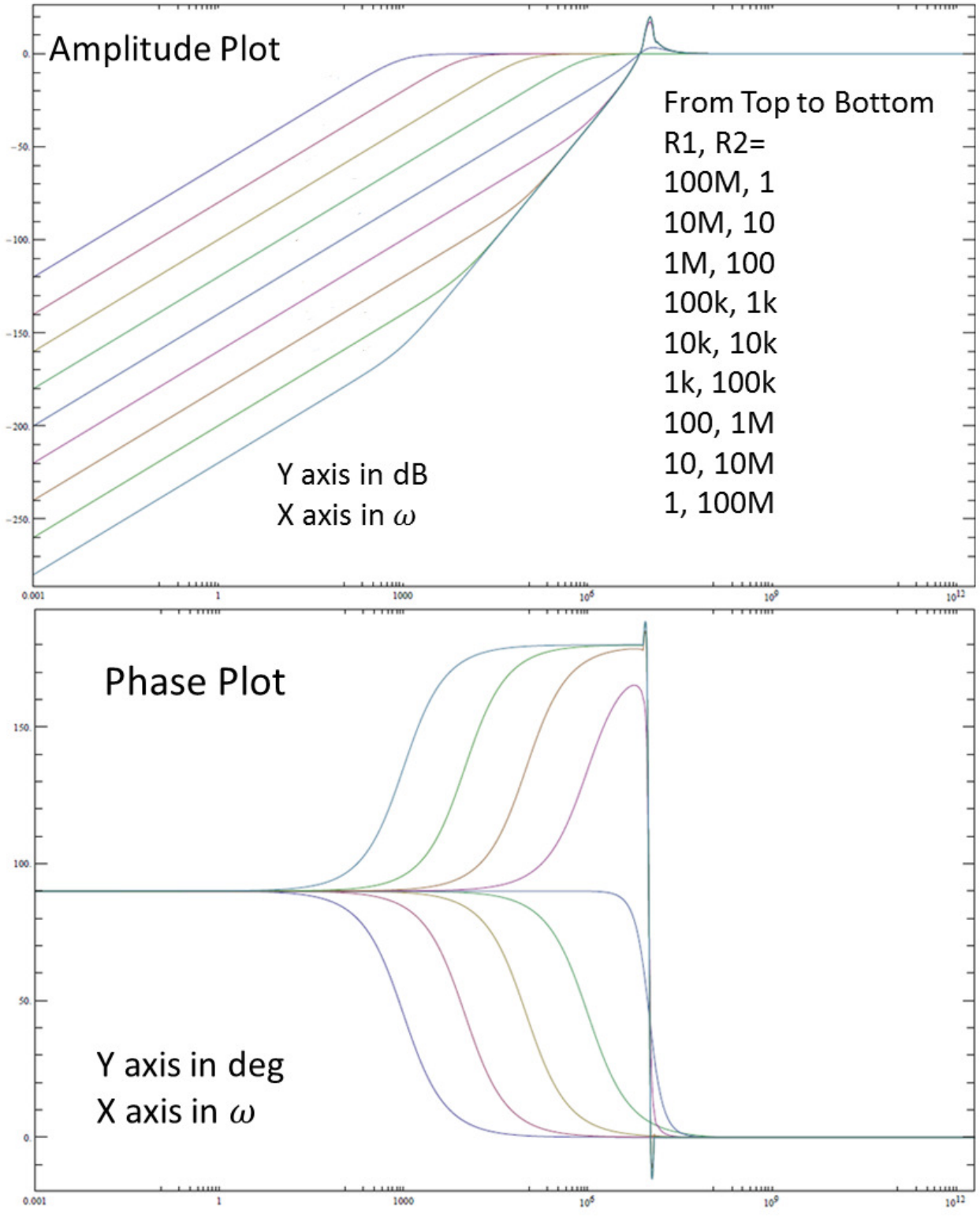


Figure 2.10 – Bode plot of NTF with R1 and R2 varying in opposite directions.

Finally, the bode plots of the remaining term in the output equation, the distortion term, needs to be examined. The next three figures, Fig 2.11, 2.12, and 2.13 show the effect of varying R1 and R2 on the distortion term bode plot. The overall behavior is that the distortion term rolls off with a 1st-order characteristic until a particular frequency where it rolls off with a 2nd-order characteristic. For some combinations, resonance causes a 2nd order roll-off without an initial 1st order roll-off. In Fig. 2.11, it is clear that increasing the value of R2 while keeping R1 fixed, causes an increase in the "Q" of the resonant peak while also shifting the resonant frequency lower. This is verified by examining the phase as well, with the sharpness in the transition to full phase inversion. In Fig 2.12, where R1 is varied and R2 is fixed, the same effect occurs for decreasing values of R1. The only difference is that the resonant frequency increases.

The condition in Fig. 2.11 is not desirable since it means that distortion increases within the signal bandwidth of interest. This appears to be contradictory to the conclusion drawn from examining the NTF – that R2 should be as high as possible. However, Fig 2.13 shows that indeed this conclusion is correct. When R1 has a low value and R2 has a high value, the distortion transfer function rolls off earlier with a 1st order characteristic and does not exhibit any resonance. The phase plot also confirms this, with a wide region of constant 90 degree phase shift.

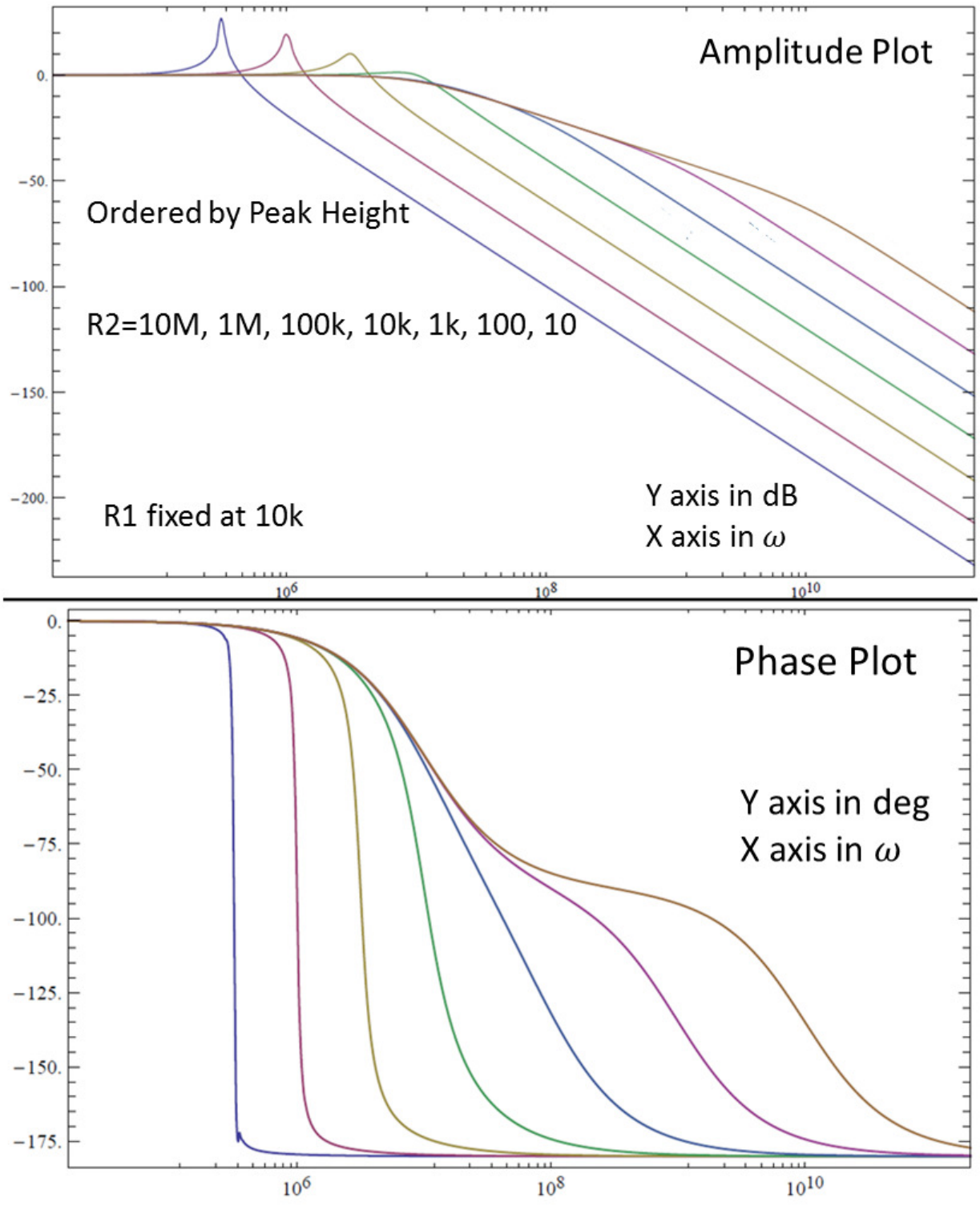


Figure 2.11 – Bode plot of DTF with R1 fixed and R2 varying.

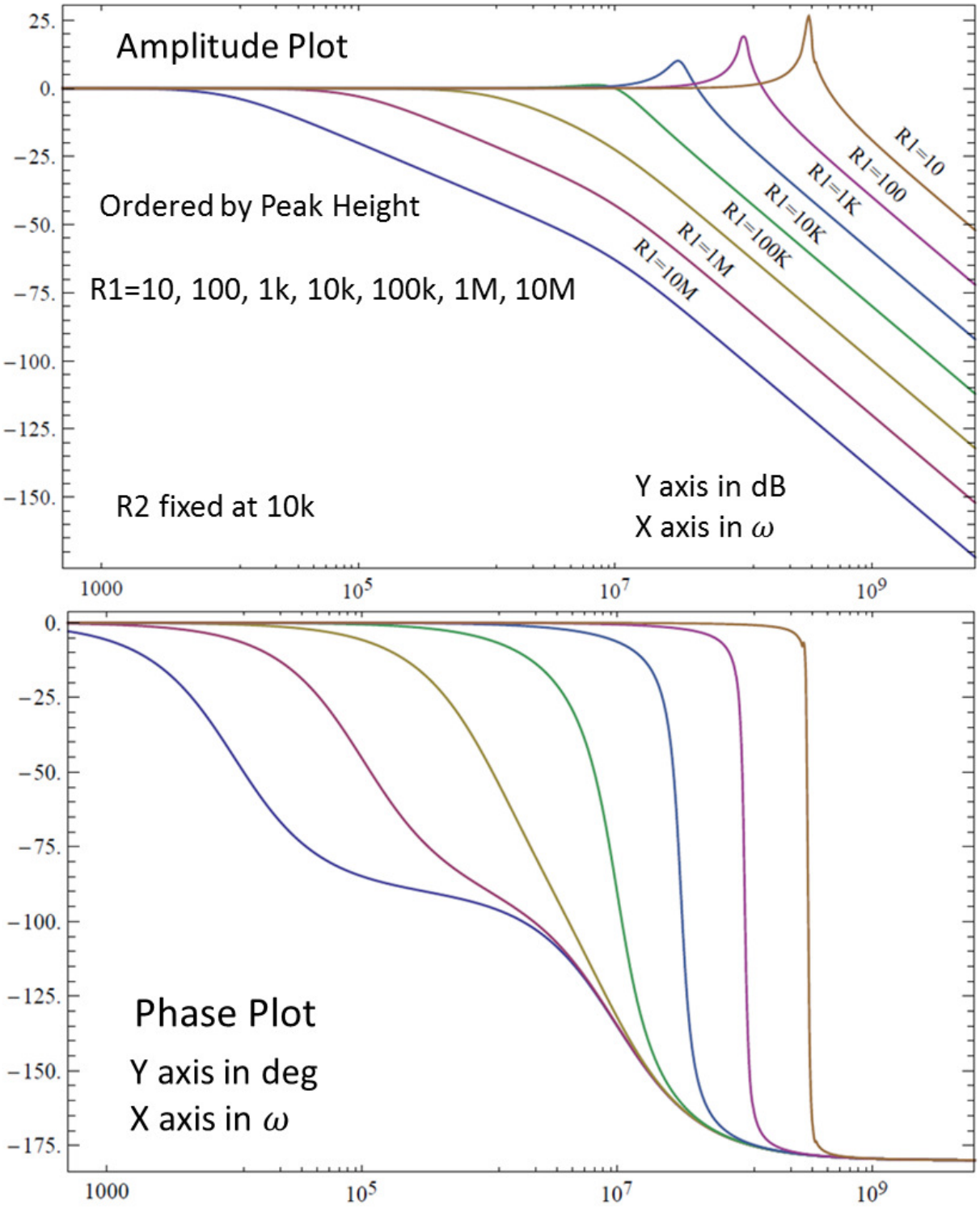


Figure 2.12 – Bode plot of DTF with R2 fixed and R1 varying.

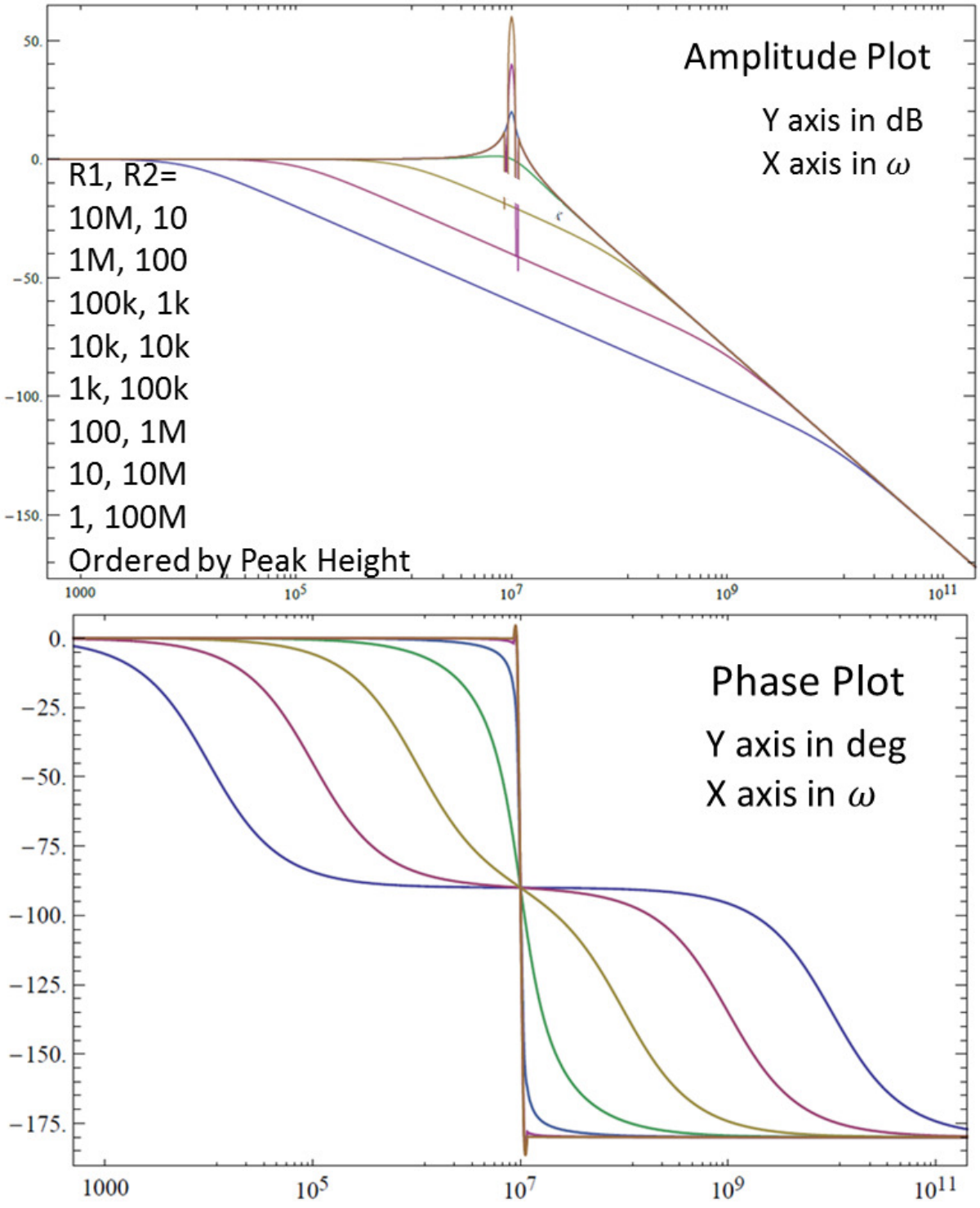


Figure 2.13 – Bode plot of DTF with R1 and R2 varying in opposite directions.

Simulated Comparison

Circuit level simulations are needed to verify that the transfer functions are indeed valid. In order to remove the effects of nonlinearities in circuit elements, ideal circuit components were used to isolate topology related effects. The ideal components used are those found in [cite] and are made up of SPICE switches, behavioral elements, and dependent sources. The components allow for ideal component level simulation in order to verify topological aspects of circuits without the nonlinearities of real components. The schematic used for simulation is displayed in Fig. 2.12.

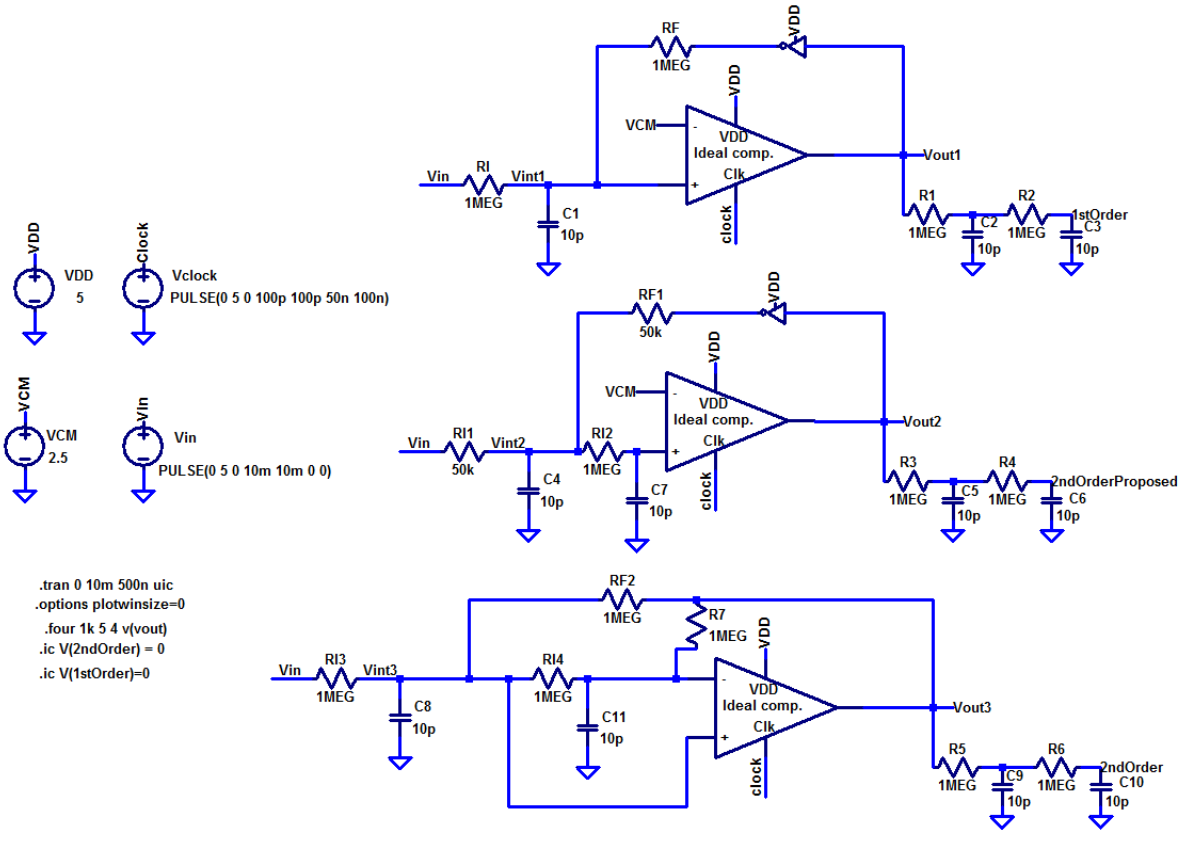


Figure 2.14 — Simulation testbed for 1st and 2nd order passive modulators.

Each topology described in this chapter is compared side by side in this simulation. A 10 ms ramp signal is applied to each input and the output is filtered to create a transfer curve. The VDD is 5V, the VCM is 2.5V and the clock frequency is 10 MHz. Since ideal components are used any value can be used for VDD and VCM. These values were selected because they are commonly used for CMOS logic levels. All passive component values were adjusted such that each modulator had the same corner frequency of 16 KHz to allow for fair comparison.

The filtered outputs and their resulting transfer curves are shown in Fig. 2.13. At first glance, all the curves seem very close to each other and almost identical. However, upon closer inspection it is apparent that the "noise" that remains after filtering is different. In the left inset, it is clear that the proposed 2nd order topology has less noise than either the 1st or 2nd order designs. The inset on the right shows the biggest disadvantage of the 1st order modulator which is the presence of dead-zones. The output stops responding and a charging RC characteristic can be seen for the 1st order modulator.

When each design is compared with the same corner frequency, the proposed 2nd order modulator exhibits the best performance but only by a small margin. However, each design differs by the number of components and the space occupied by these components in a practical implementation. For a discrete board level implementation of a sigma-delta modulator (rare in practice) the board space and component cost considerations make the 1st order modulator attractive. The proposed 2nd order modulator offers an increase in performance with only two additional components. The traditional 2nd order design requires four which is not a good solution for board level implementations.

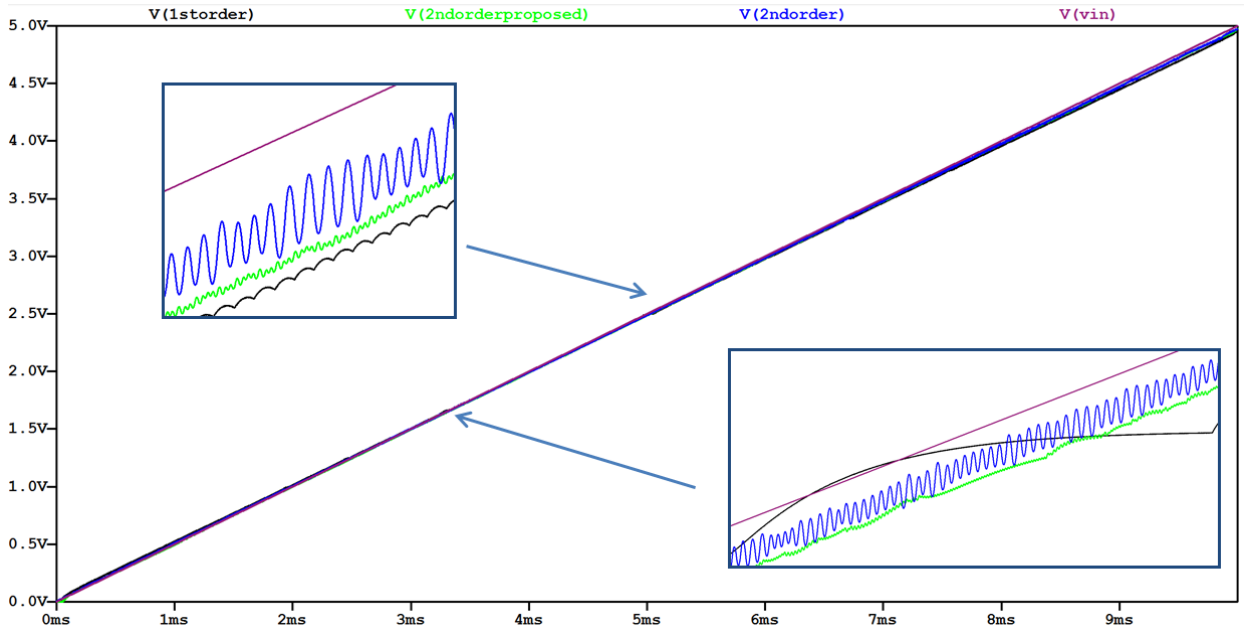


Figure 2.15 – Transfer curves and zoomed insets.

For IC implementations, layout area considerations are different. For example, resistors affect the layout area based on their value rather than quantity. It is in this area, where the proposed 2nd order design offers the greatest benefit. The passive component count for each design is shown in table 2.1. The layout areas for the 1st order and proposed 2nd order topologies are about the same. This is because the area for a 50 kΩ resistor is quite small compared to a 1 MΩ one. However, the proposed 2nd order design requires an additional 10 pF capacitor which has a layout area that's comparable to a 1 MΩ resistor. Therefore in the proposed 2nd order design, a 1 MΩ resistor is traded for a 10 pF capacitor which results in roughly the same area. The traditional 2nd order design has quite a large layout area requiring four 1 MΩ resistors and two 10 pF capacitors.

Topology	**Resistors**		**Capacitors**		**Comments**
1st Order	2	1 MΩ	1	10 pF	About equal to proposed 2nd order
Proposed 2nd Order	1	1 MΩ	2	10 pF	50 kΩ layout area is small compared to 1 MΩ
	2	50 kΩ			
2nd Order	4	1 MΩ	2	10 pF	Largest passive component area

Table 2.1 – Passive Components

Taking layout area into consideration, an additional simulation was performed which reduced the value of the resistors in the traditional 2nd order modulator to 250 kΩ or one quarter their value used in the simulation in Fig. 2.13. The results in Fig. 2.14 show how performance differs between the modulators when adjusting for layout area considerations. Both the 1st and traditional 2nd order modulators show dead-zones in the inset in Fig. 2.14. Overall, when adjusted for area, the proposed 2nd order modulator offers the best performance.

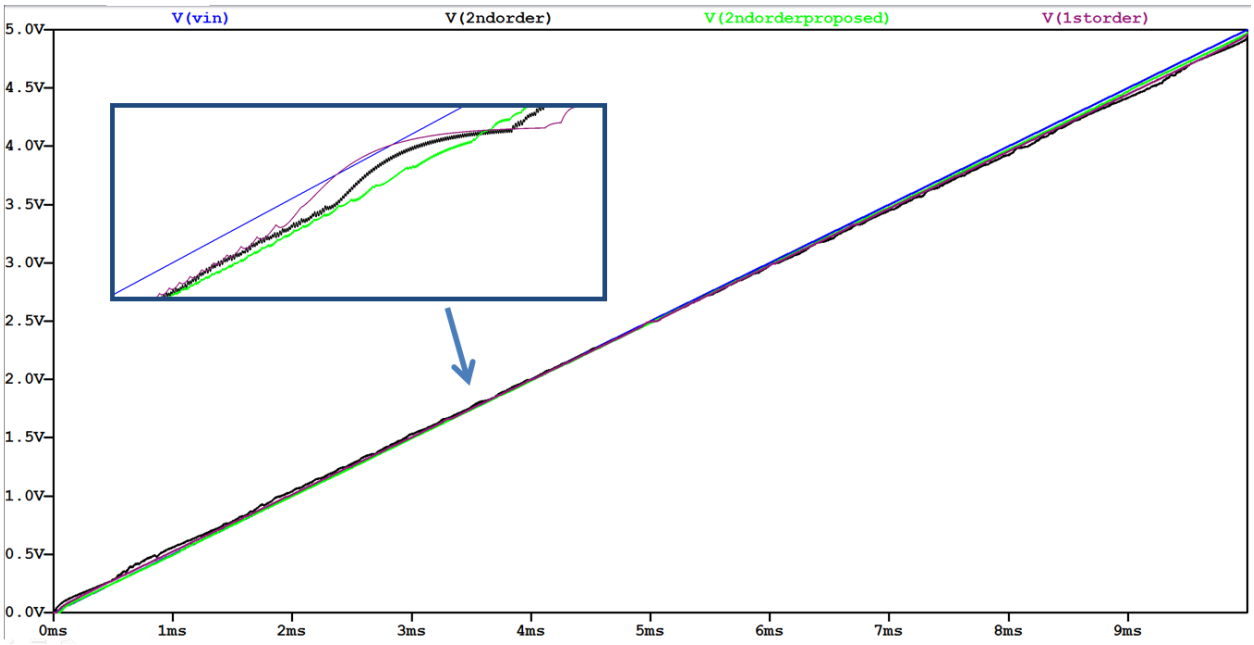


Figure 2.16 – Transfer curves for equal area and zoomed inset with dead zones.

A transient analysis was performed in LTSpice with 20 cycles of a 1 KHz sine wave and the resulting FFT was used to compare the AC performance between modulators. These waveforms are shown in Fig. 2.14. The FFT of each modulator's filtered output is shown in Fig. 2.15. From this, it is clear that the 1st and proposed 2nd order modulators have less distortion components than the traditional 2nd order design. The ".four" function was used to compute the THD values and the results are shown in table 2.2. These results were obtained by calculating THD for the first five harmonics. The THD for the 1st order and proposed 2nd order modulators are almost identical although the 1st order is marginally worse. Since the results aren't conclusive, the simulations were repeated for an input frequency of 2 KHz. In this case the proposed 2nd order modulator clearly has the lowest distortion.

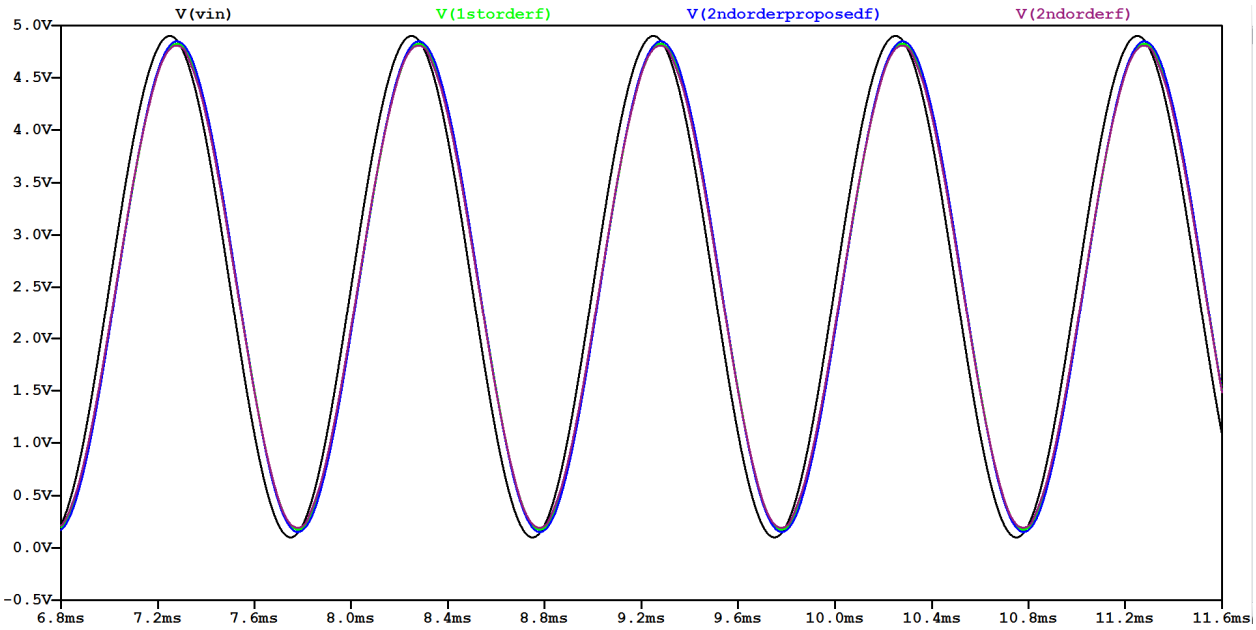


Figure 2.17 – Filtered output of each modulator with a 1 kHz input signal.

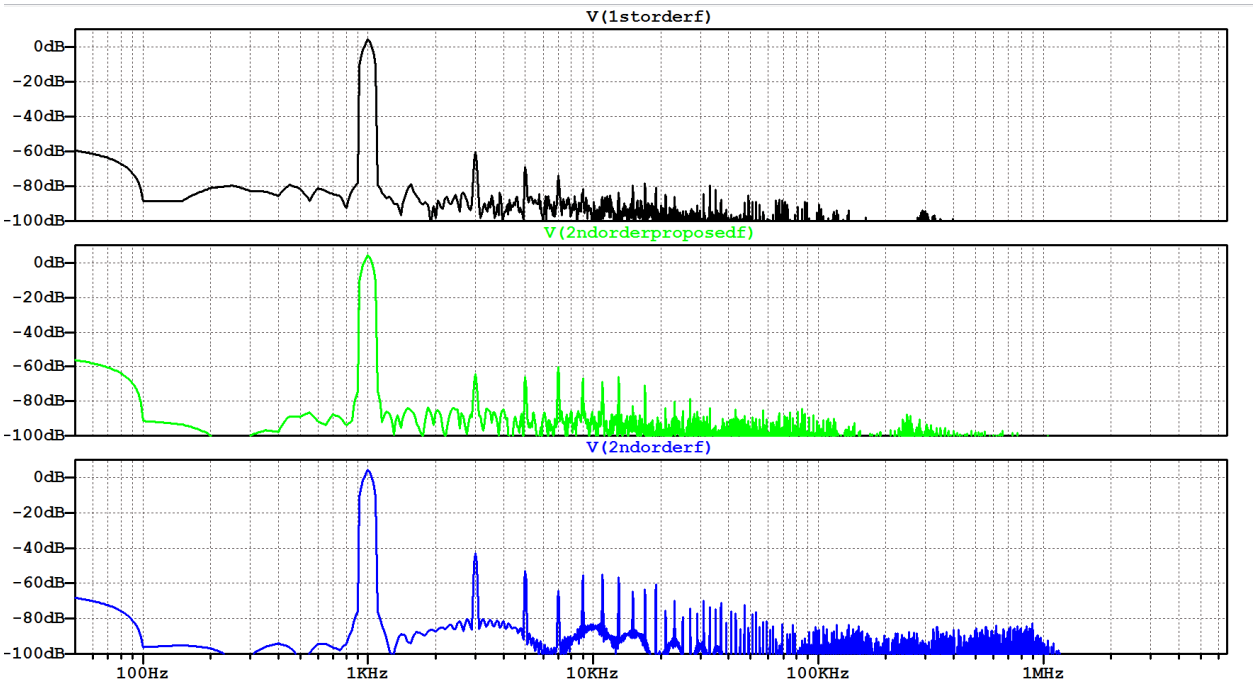


Figure 2.18 – FFT of each modulator's filtered output.

<table>
<tr><th>Topology</th><th>Total Harmonic Distortion (THD) %</th></tr>
<tr><td>1st Order</td><td><table><tr><td>Frequency</td><td>THD</td></tr><tr><td>1 KHz</td><td>0.061%</td></tr><tr><td>2 KHz</td><td>0.052%</td></tr></table></td></tr>
<tr><td>Proposed 2nd Order</td><td><table><tr><td>Frequency</td><td>THD</td></tr><tr><td>1 KHz</td><td>0.058%</td></tr><tr><td>2 KHz</td><td>0.041%</td></tr></table></td></tr>
<tr><td>Traditional 2nd Order</td><td><table><tr><td>Frequency</td><td>THD</td></tr><tr><td>1 KHz</td><td>0.46%</td></tr><tr><td>2 KHz</td><td>0.35%</td></tr></table></td></tr>
</table>

Table 2.2 –THD for each Topology

Finally, the FFT of the unfiltered digital output is shown in Fig. 2.16. It is important to examine this to see how the quantization noise is distributed amongst the frequencies. From this plot, it is clear that the noise-shaping for the 2nd order modulators is sharper than that of the 1st order modulator as expected. It is also clear that the noise floor for the proposed 2nd order modulator is the lowest of the three designs.

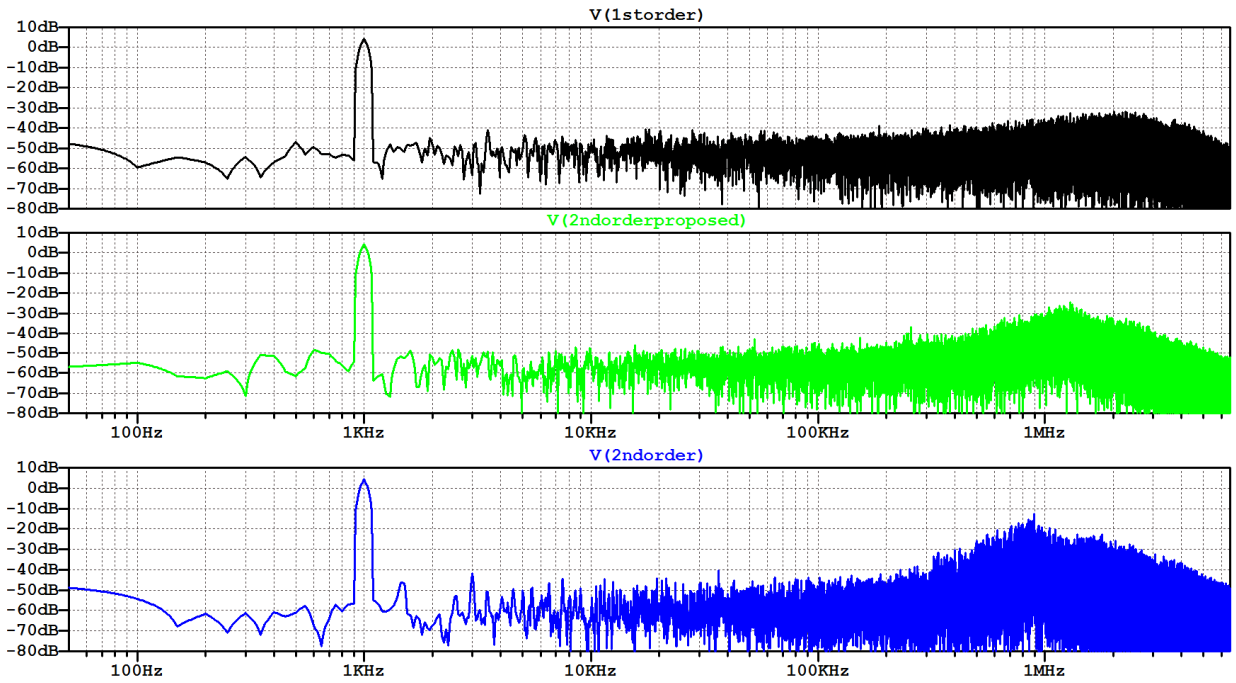


Figure 2.19 – FFT of each modulator's digital output.

Overall, it appears that the proposed 2nd order modulator topology is better than both the 1st order and traditional 2nd order topologies. This has been verified through the use of transfer functions which show better noise-shaping and lower quantization noise in the region of interest. Furthermore, SPICE simulations with ideal components show that the proposed 2nd order topology exhibits the best DC transfer linearity, lowest THD and lowest noise of all the presented designs.

Chapter 3 Discrete Component Level Implementation

It is important to verify simulation results using ideal components by building an actual circuit and determining if the basic principles still hold true when translated into the real world. In order to do this, the passive modified 2nd order topology from chapter 2 was implemented using a discrete commercially available comparator and standard passive components. The results of this exercise demonstrate that the concept does indeed work in a real circuit and also that there is much room for improvement.

The schematic of the circuit is displayed in Fig. 3.1. This circuit is based around the LT1671 comparator made by Linear Technology [10]. This latched comparator is marketed as a low-power and high-speed device. In this application, the comparator was set up for dual supply operation, using +/- 5V power supplies. One advantage of this set-up is that no common-mode voltages need to be created since there is a ground reference. The passive network on the left of the LT1671 is the noise-shaping and feedback network. The passive network on the right of the chip is a simple 2nd order filter with a corner frequency of 72 KHz. The clock frequency was set to 1 MHz. This results in a very wide bandwidth and consequently a low OSR. A much lower corner frequency would likely be selected in a final implementation. The goal in this case was to examine the output harmonics clearly without attenuating them.

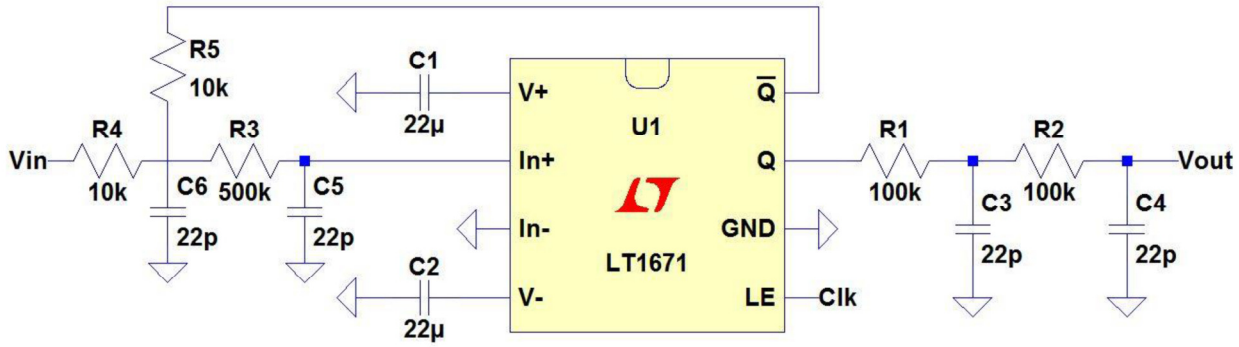


Figure 3.1 – Schematic of LT1671 based 2nd-order ∑-Δ modulator.

The circuit was built on an SOIC-8 breakout board with through-hole components directly soldered onto the pins. The top and bottom images of the circuit are shown in Fig. 3.2. Standard ¼ carbon film resistors were used. The capacitors were of film and NP0 ceramic dielectric types. These capacitors have stable capacitances that do not vary with changes in applied voltage. It is worth noting that if ceramic capacitors are used in any sort of filtering application they must be of NP0 type. Other ceramic dielectrics can introduce as much as 1% distortion into the signal. The completed circuit was mounted onto a copper-clad board with proper decoupling capacitors at the power supply connections and BNC connectors for input/output signals. This is shown in Fig. 3.3 and is the set-up used to collect data for SNDR testing.

Figure 3.2 – Top and bottom of circuit on SOIC-8 breakout board.

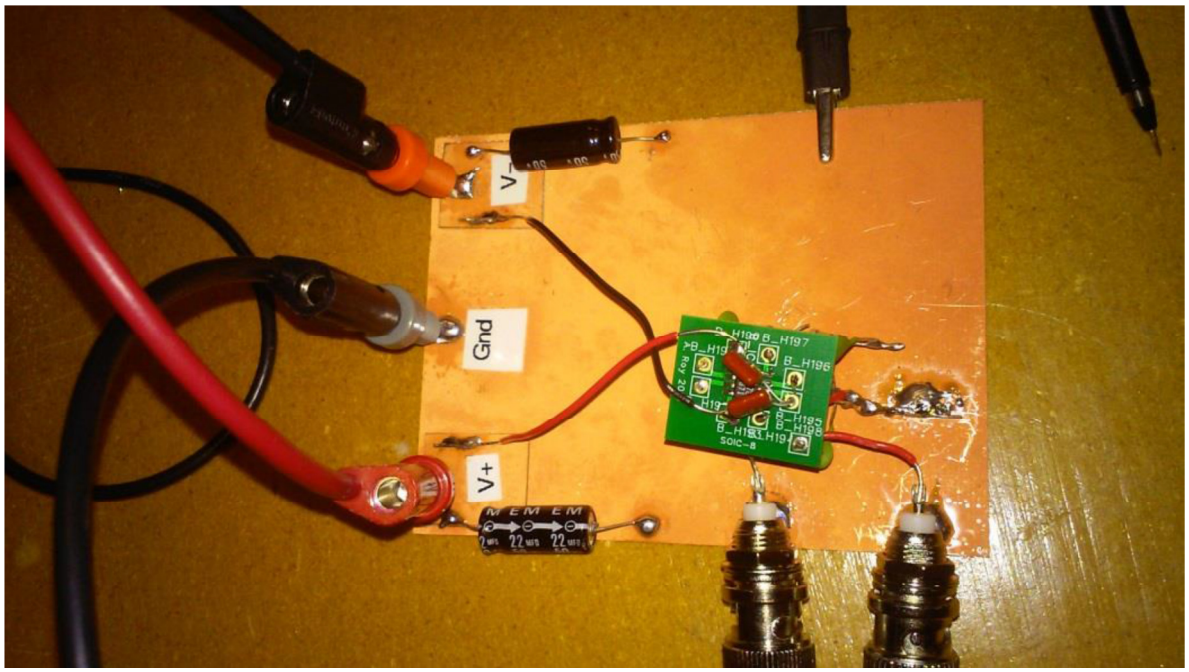


Figure 3.3 – Set-up used for SNDR testing.

The complete set-up was tested using basic, student level test equipment. The regulated dual output power supply was set to +/- 5V. The input signal was set to be a 3.3V sine wave and came from a low distortion function generator. The output of the circuit was connected to a PC oscilloscope with 14-bits of vertical resolution and 10 MHz bandwidth [11]. This high resolution allows for meaningful SNDR testing. An example of an FFT spectrum is displayed in Fig. 3.4. For this plot, the input signal is 1 KHz and the total span of

the FFT is 8 KHz. The noise floor is at around -80 dB. The smoothness of the noise floor is due to averaging of 16 samples. Furthermore, coherent sampling was used to increase the spectral resolution of the FFT. This allows for an integer number of sinusoidal cycles within the sampling interval. Since the output filter is only 2nd order, there is still some energy at the 1 MHz clock frequency. This is shown in Fig. 3.5.

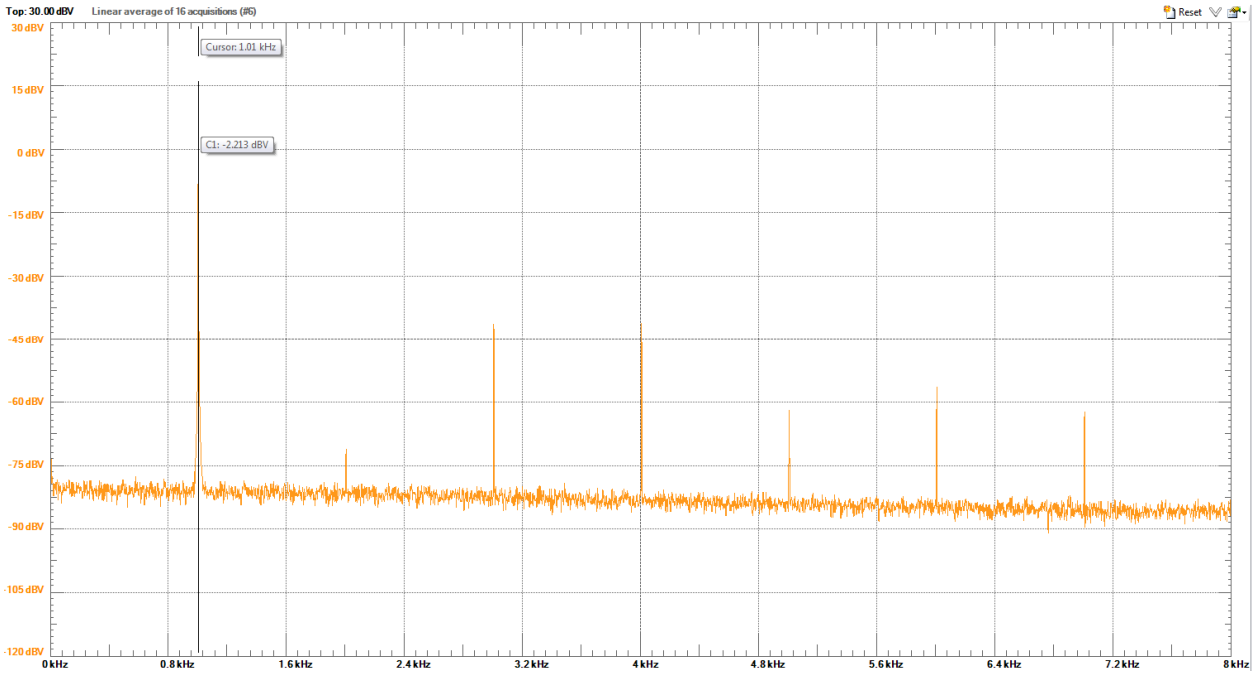


Figure 3.4 – Example output spectrum.

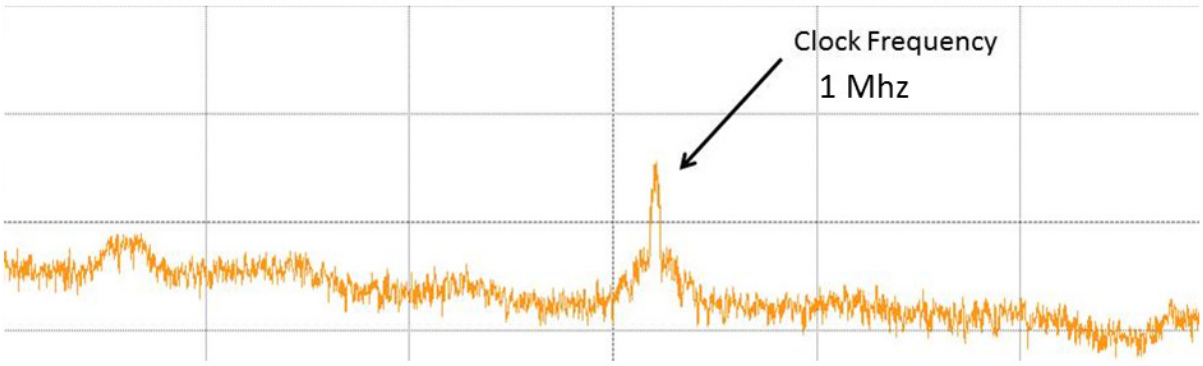


Figure 3.5 – Remnant of 1 MHz clock frequency.

The SNDR was characterized by using THD. This is appropriate in this case because the distortion components are much higher than the noise power within the signal bandwidth. The THD was calculated by using the formula,

$$THD_f = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

The levels of the first five harmonics were examined on the FFT and tabulated in Excel to make a THD plot. The THD as a function of frequency is shown in Fig. 3.6. The THD remains at less than 40 dB below the fundamental for most of the frequency range. The THD decreases with increasing frequency mainly due to the fact that the higher order harmonics are being attenuated as they approach the corner frequency of the 2nd order output filter. These THD levels are translated into ENOB in Fig. 3.7. The ENOB remains between 6 and 7 bits for most of the frequency range. While this is not good performance, it is important to note that no special precautions were taken in the implementation of this modulator. No matching was performed between components, no optimization of clock frequencies nor were output filters implemented.

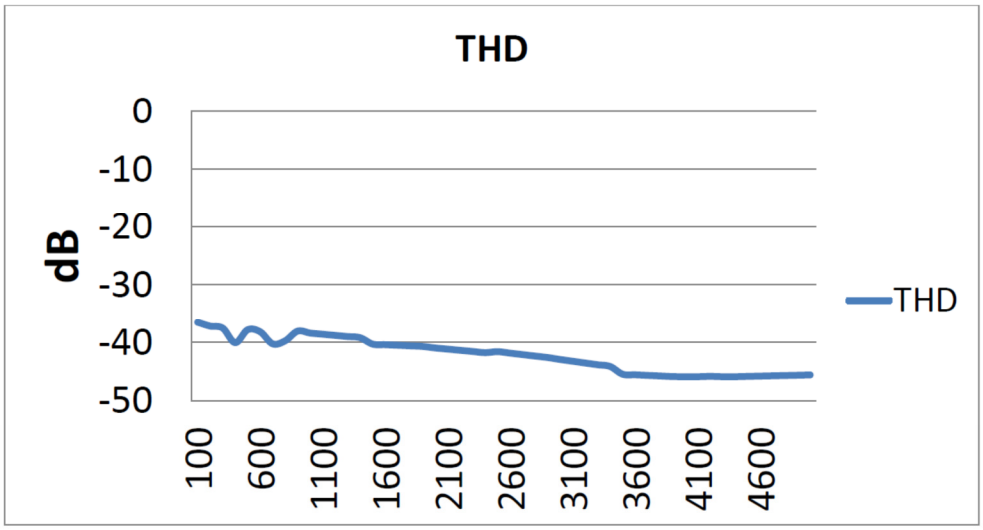


Figure 3.5 – THD as a function of input frequency (Hz).

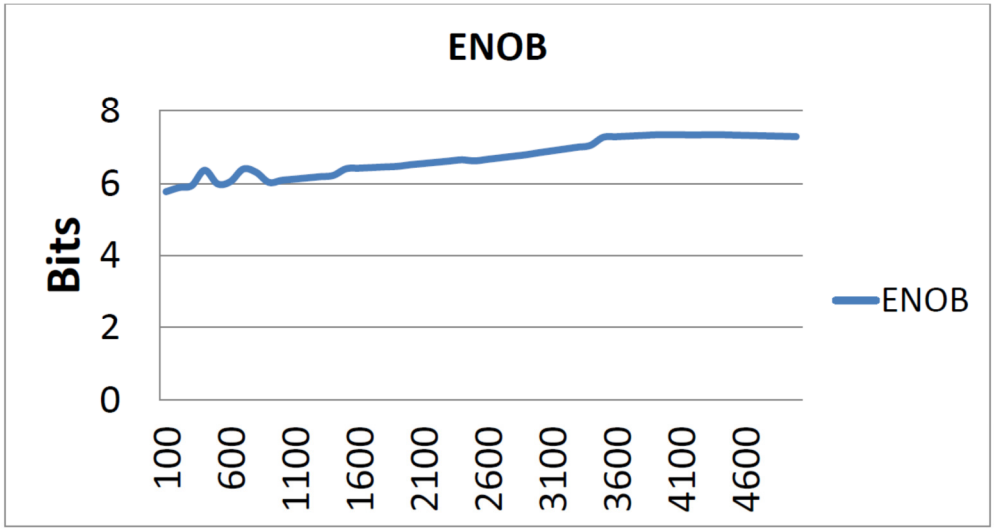


Figure 3.6 – ENOB as a function of input frequency (Hz).

Chapter 4 Continuous Time Sigma Delta Modulators

Circuit Design

To verify the validity of theory and simulations, a physical implementation of the modified 2nd order passive sigma-delta topology is required. A simple continuous-time integrated circuit (IC) implementation on a mature CMOS process is a good starting point. The insights gained from such an exercise should scale well into modern CMOS processes. The C5 process by On Semiconductor is ideal for this application because of the high quality poly resistors and capacitors available which allow for the high resistance and capacitance values required by this topology [12]. The process also allows for the design of high quality analog components and digital logic at convenient 5V and 3.3V levels. A cell based methodology using the Electric VLSI software was used to design and layout the chip [13]. LTspice was used as the SPICE engine for both schematic and layout level simulation.

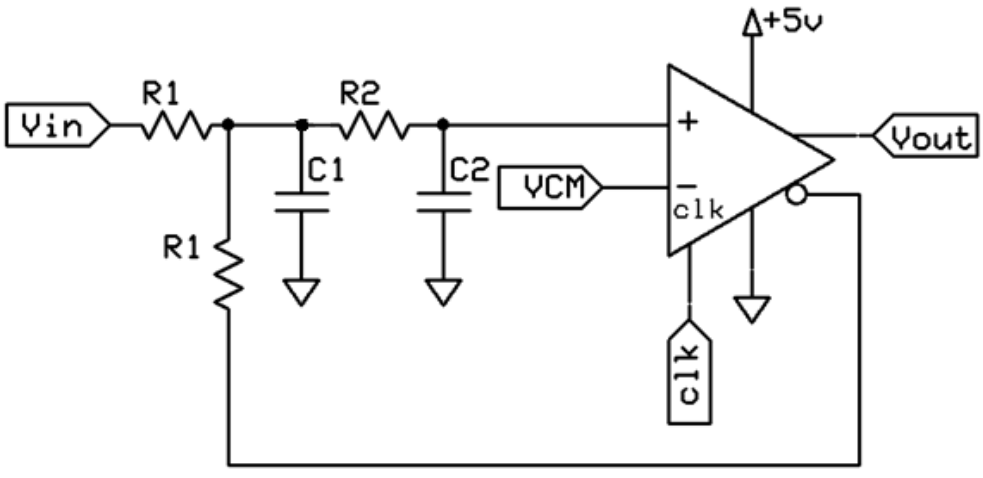


Figure 4.1 – Basic schematic of continuous time sigma-delta modulator.

The basic schematic of the continuous-time sigma-delta modulator is shown in Fig. 4.1. The values of the passive components are given in Table 4.1. The resistors are created using the high-resistivity polysilicon in the C5 process. This high-resistivity treatment allows for high resistor values that are not possible using well resistors. The capacitors are formed using poly-poly capacitors available in the C5 process. Although the passive components are relatively large and take up most of the chip area, it is still practical to use them for an IC implementation. The layout views of the passive cells are shown in Fig. 4.2. These are not to scale and are intended to simply illustrate the components.

Part	**Value**	**Layout Size**
R1	50 kΩ	162 um x 4.2 um
R2	1 MΩ	312 um x 63 um
C1/C2	10 pF	240 um x 60 um

Table 4.1 – Passive Component Values

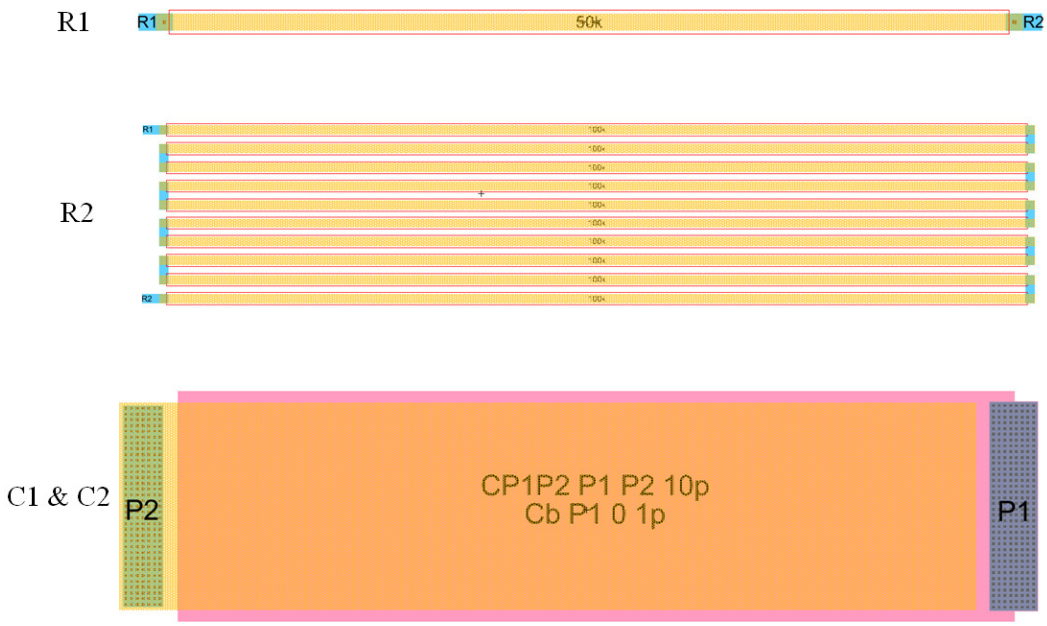


Figure 4.2 – Layouts of passive components (not to scale).

The most important part of the sigma-delta modulator is the clocked comparator. Much of the performance limitations are directly the result of the design of this component. For this application, a comparator needs to be decisive. This means that small input signals need to cause the output to swing either high or low without toggling back and forth until settling to one state. If the comparator was not decisive then metastability would ultimately reduce the resolution of the data converter. Although, it is worth noting that the sigma-delta topology inherently reduces the effect of noise since many samples are averaged together.

There are many comparator topologies that can be used in a sigma-delta modulator. For simplicity and low power, a memory sense amplifier with an SR latch and output inverters was selected as the comparator topology in this design. The block diagram of this circuit is shown in Fig. 4.3. The clocked comparator with differential outputs is on the left,

the S-R latch is in the middle and the output buffers are on the right. The S-R latch is used so that the output toggles only on the rising edge of the clock. The latch is comprised of two cross-coupled NAND gates. The output buffers are simple inverters.

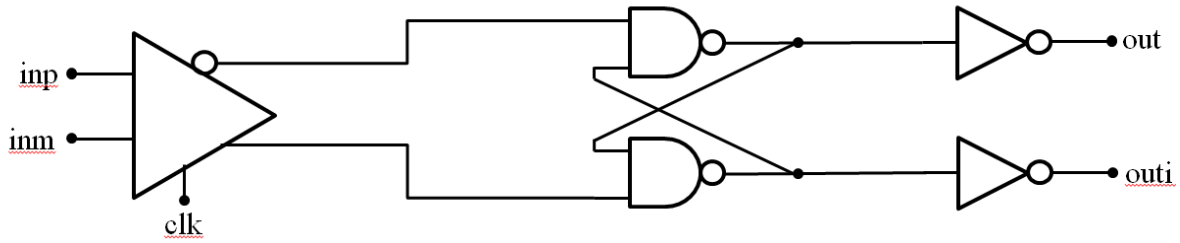


Figure 4.3 – Block diagram of comparator.

The memory sense amplifier uses a topology adapted from [14]. This type of amplifier is usually used for sensing in DRAM applications. As there may be hundreds of these amplifiers in a typical memory chip, reducing power consumption is very important. The low power consumption of this sense amplifier design is attractive in a passive sigma-delta modulator application. The schematic of the sense amplifier is shown in Fig. 4.4. The reason that this topology has low power consumption is due the use of long length MOSFETs operating in the triode region. These are the input MOSFETs in the bottom of the schematic. The long length MOSFETs reduce the contention current that flows to ground each time the clock switches state. Furthermore, the resistances of the long length MOSFETs isolate the inputs from the clock kickback noise. The operation of the circuit depends on the voltage imbalance of the inputs. Once the imbalance is sufficient, the input MOSFET with the higher input voltage pulls down the gate-source voltage (V_{gs}) of the MOSFET above it. This causes that MOSFET to conduct resulting in the cross-coupled latch

to switch. A cross-coupled latch uses positive feedback to increase the gain and response time.

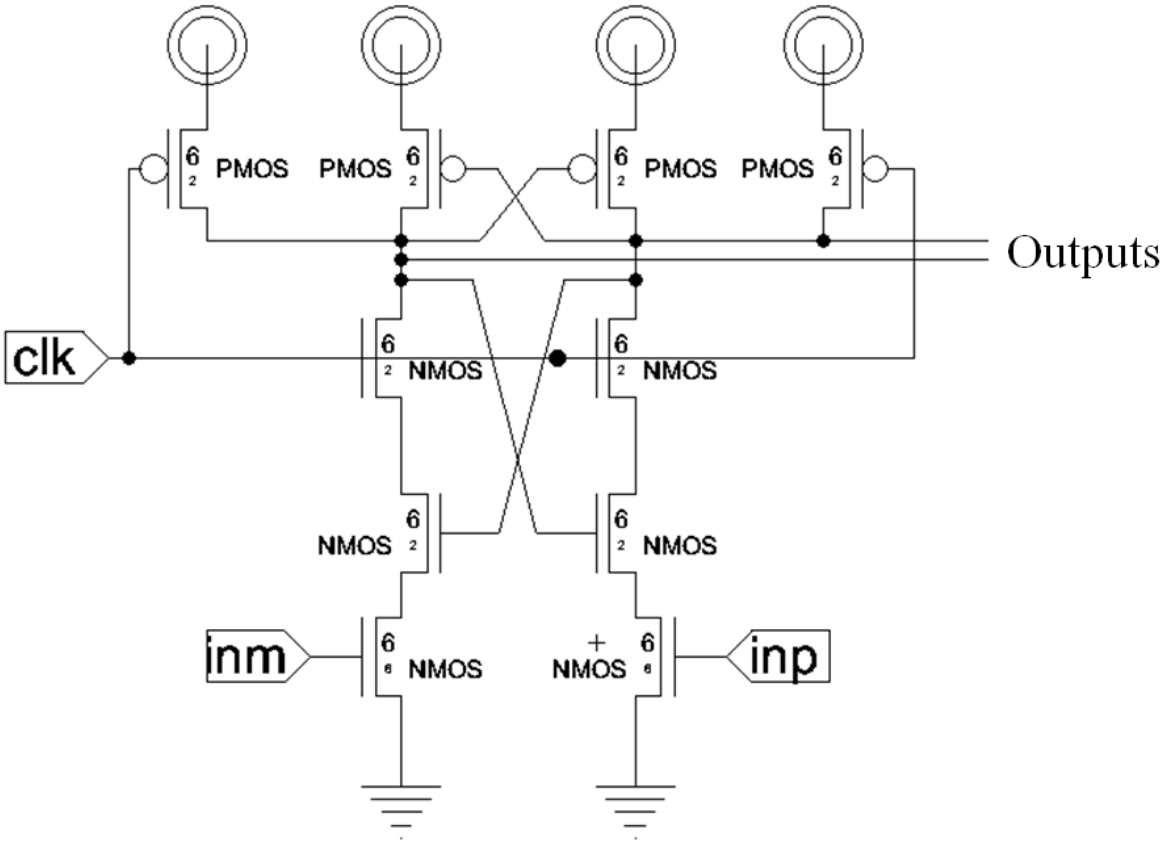


Figure 4.4 – Sense amplifier schematic.

The remainder of the comparator design is made up of an S-R latch and output inverters. The S-R latch is made up of dual two-input NAND gates. The output inverters are made from identically sized PMOS and NMOS devices. All MOSFETs are minimum size in order to minimize power consumption. This does result in differing low to high (t_{PLH}) and high to low (t_{PHL}) transition points. The reason this occurs is because NMOS devices have about double the transconductance for a given size than PMOS devices. Generally, in most logic applications, the PMOS devices are twice the size of NMOS devices to result in equal

transconductance and therefore equal transition points. The switching point for the inverter is shown in Fig. 4.5.

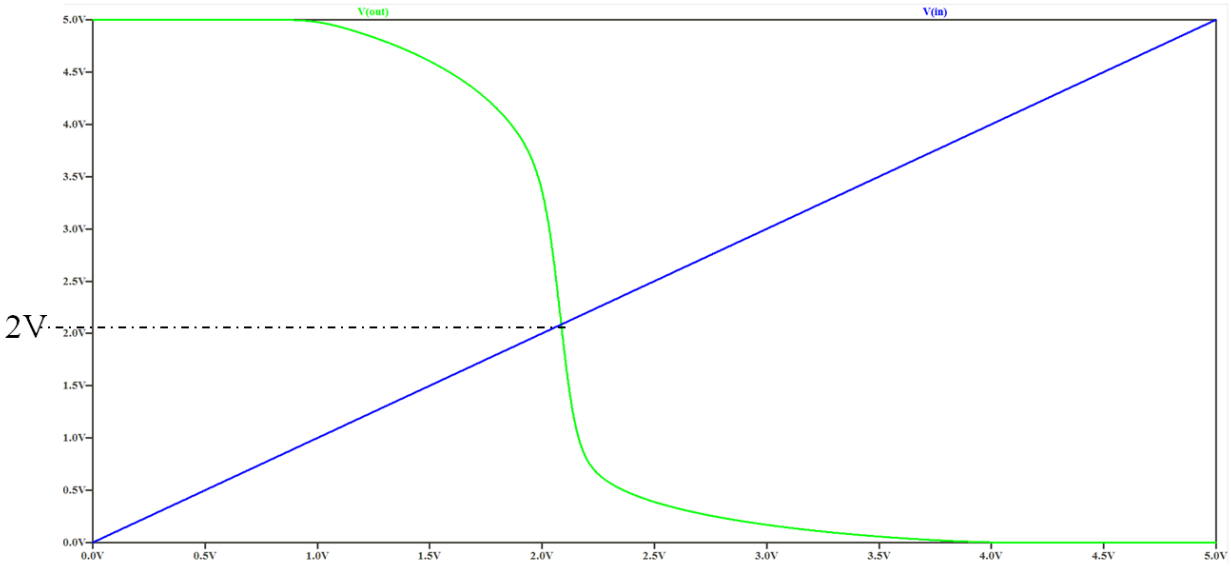


Figure 4.5 – Inverter switching point.

The full schematic of the comparator with a side by side comparison to its block diagram is shown in Fig. 4.6. Generally a common mode input of half the supply voltage is applied to the negative terminal of the comparator. When the voltage applied to the positive terminal exceeds that of the negative terminal, the output of the comparator switches high and the complementary output switches low. This is shown in Fig. 4.7. For this simulation the input signal is an arbitrary waveform to show that the comparator switches at the correct points. The complementary output is required to provide negative feedback and eliminates the need for an additional inverter and its associated delays in the feedback loop.

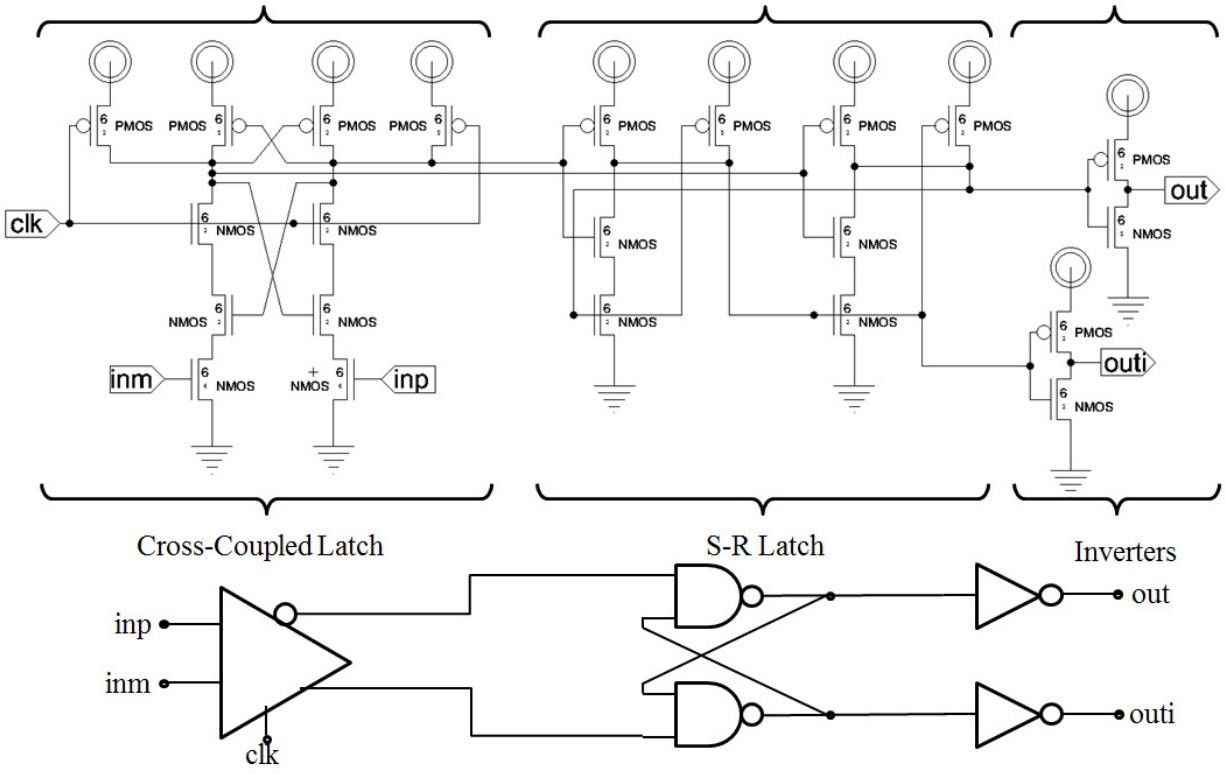


Figure 4.6 – Full schematic of comparator.

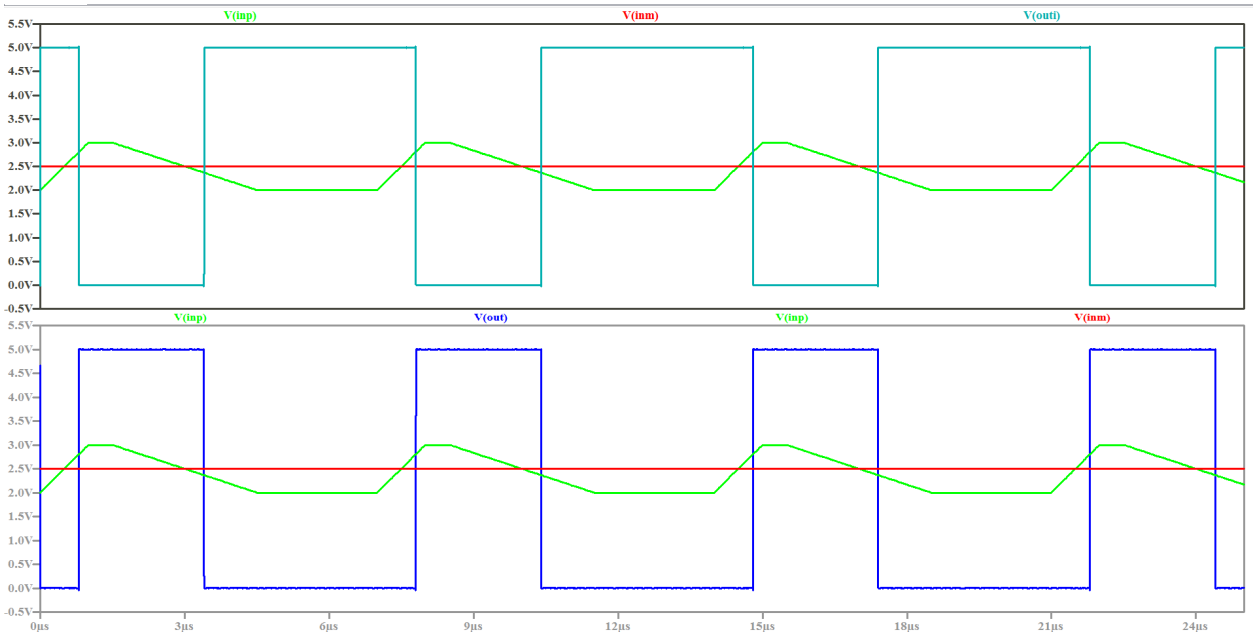


Figure 4.7 – Comparator operation with V_{inp} (green), V_{inm} (red), V_{out} (blue), and V_{outi} (teal).

The layout of the comparator is carefully optimized to take up as little area as possible. Most component spacing is as close as possible while following C5 process design rules. The layout of the comparator is shown in Fig. 4.8. All MOSFETs are minimum size except for the input MOSFETs where the longer channel lengths are clearly visible. The size of the layout is 61.3 um by 37.6 um. This small size is critical because the passive components will occupy the majority of the space on the chip. A simulation of the layout with conservative RC modeling gives almost identical results to the schematic simulation. This means that parasitic effects from the layout are negligible. The full modulator layout is shown in Fig. 4.9. The total size of this layout is 400 um by 270 um. A micrograph of the modulator is shown in Fig. 4.10. This micrograph is a portion of a complete test chip which was fabricated with other test structures shown in Fig. 4.11.

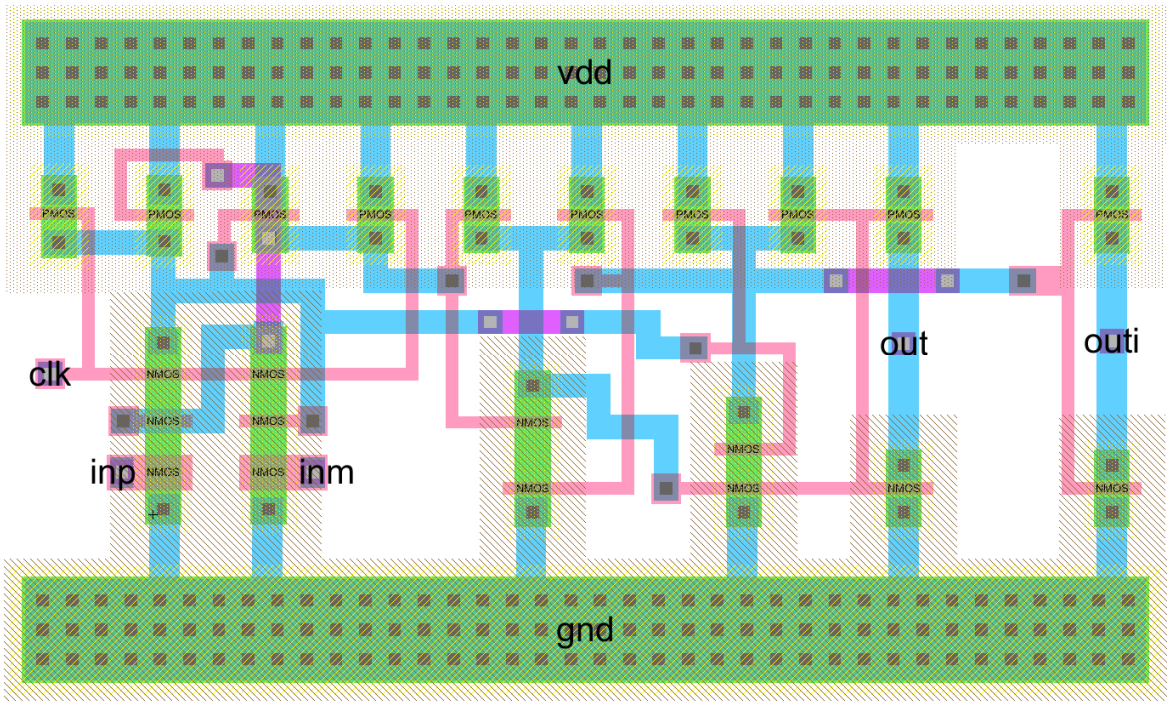


Figure 4.8 – Comparator layout.

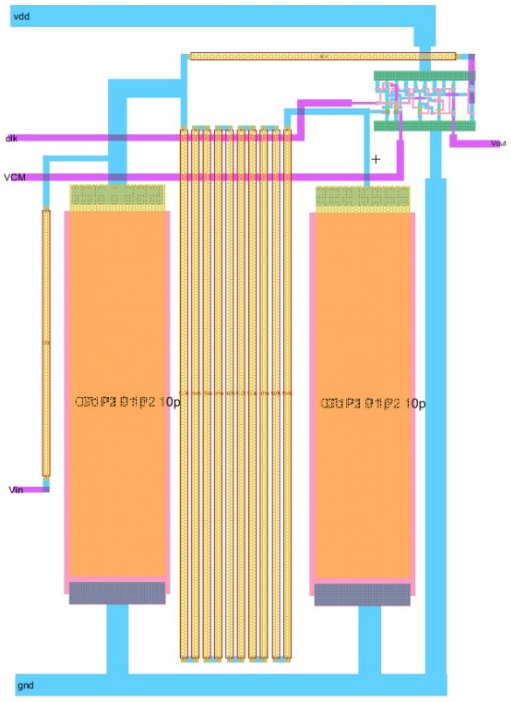


Figure 4.9 – Complete modulator layout.

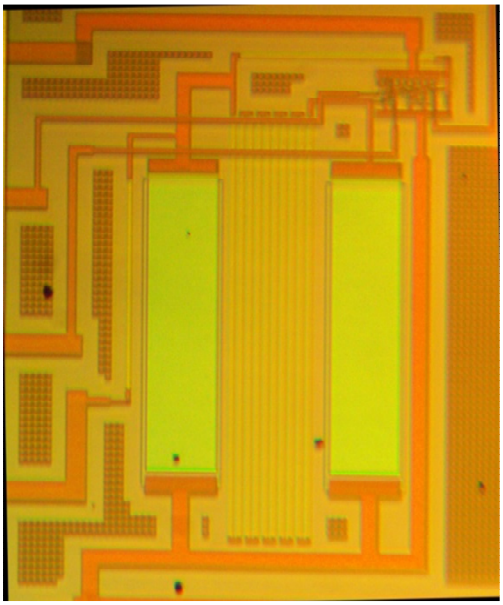


Figure 4.10 – Micrograph of modulator.

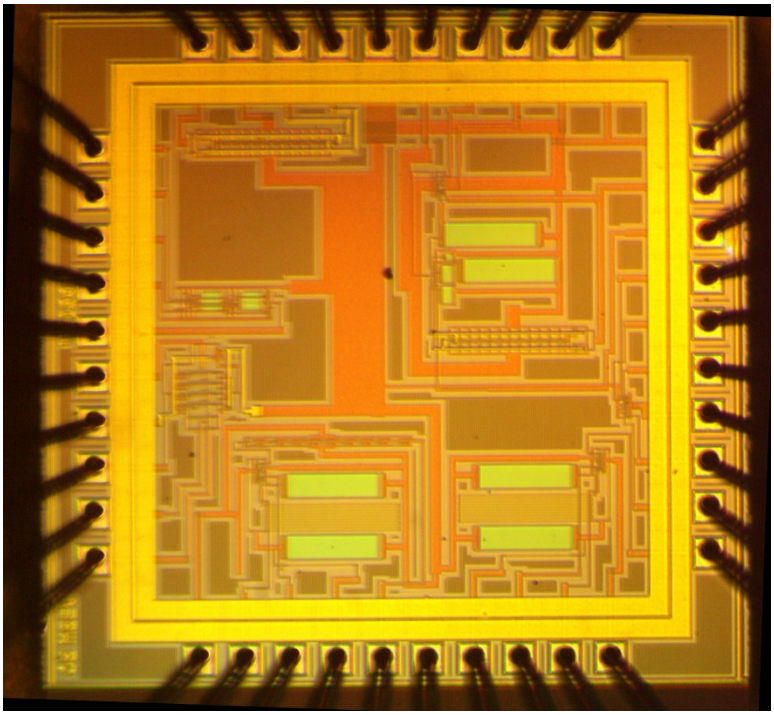


Figure 4.11 – Micrograph of complete chip.

Simulations of the passive modified 2nd order sigma-delta modulator are needed to quantify its performance. Since a sigma-delta modulator operates by averaging a large number of samples, different types of testing must be done than other ADCs. Traditionally the linearity of Nyquist-rate ADCs are characterized with a plot of input voltage vs. output code. This is not possible with sigma-delta modulators since the output is 1-bit. Instead, a very slow ramp signal is applied to the input and averaged to create a linearity plot. A simulation of this sigma-delta modulator showing the input ramp signal and unfiltered 1-bit output is shown in Fig. 4.12. The input range of this design appears to be between 0.6V and 4.5V. Outside of this range, the output does not respond. At first glance, this can be attributed to the fact that the comparator design does not have a symmetrical input stage and thus fully rail to rail inputs. However, this is not the case since the comparator is used

with feedback which keeps the signal at the inputs around the common mode voltage which is well within the input range for the comparator. Rather this is due to the inability of the comparator to switch with input signal differences of below a few millivolts. This will be examined later and is a source for improvement with this design.

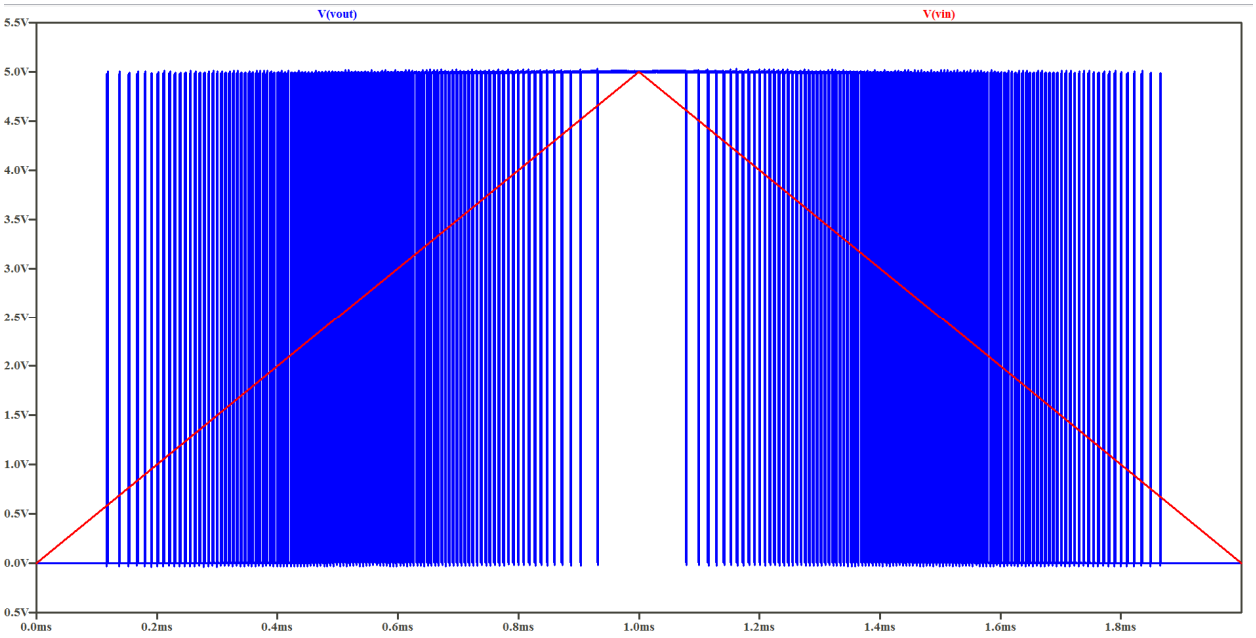


Figure 4.12 – Input ramp (red) and 1-bit output (blue).

Filtering the output results in a reconstructed ramp signal and reflects the linearity of the modulator. This output ramp is shown in Fig. 4.13 along with the input ramp signal. The perturbations along the slope of the output ramp are artifacts due to a non-ideal filter. A second order RC filter was used to create this plot. Using a higher order digital filter will remove these artifacts.

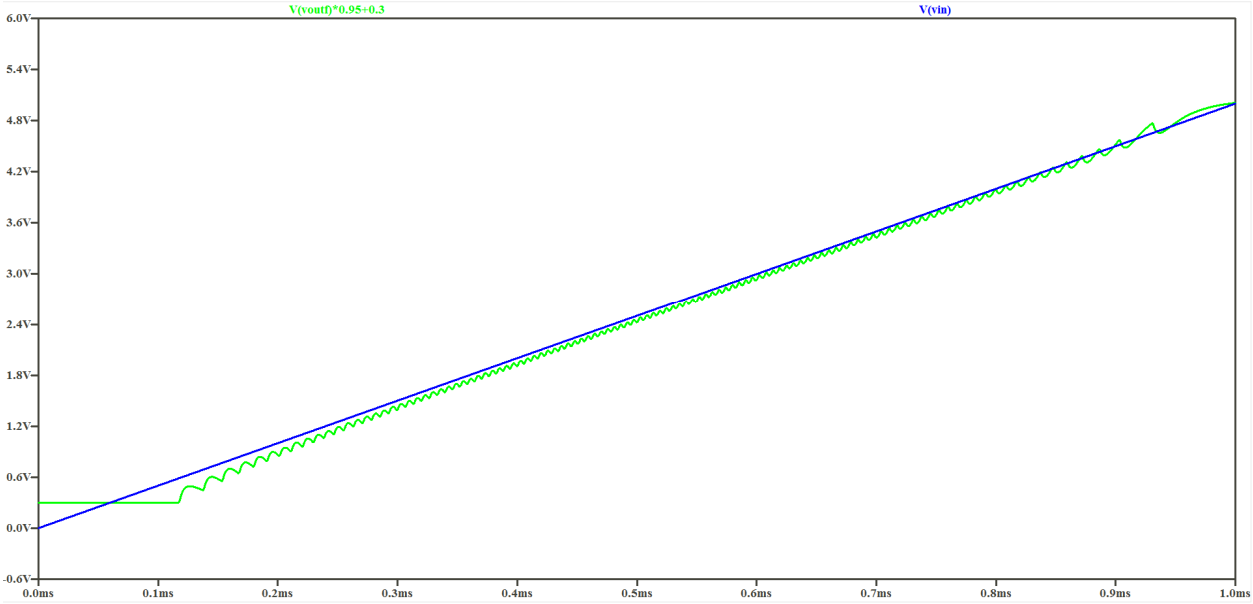


Figure 4.13 – Filtered reconstructed output ramp compared to input ramp.

The mostly linear transfer function of this modulator indicates good AC performance as well. The small slope error that is visible in Fig 4.13 is due to the gain of the modulator not being exactly unity. While this is detrimental to DC input signals and results in a large error, it does not affect the linearity of AC signals. This is because AC linearity only depends on the slope of the transfer function being linear and is independent of gain. However, the gain error can be reduced through software trimming and calibration in the intended application of the ADC. A simulation of a reconstructed sine wave after passing through a digital sinc filter is shown in Fig. 4.14. The clock frequency for this simulation is 5 MHz, the input signal is 1 KHz and the OSR is set to 256. This results in a bandwidth of 10 KHz. The noise components within this 10 KHz bandwidth are added to the SNR. The FFT of the modulator output is shown in Fig. 4.15. The red portion of the spectrum is within the bandwidth that contributes to the SNR of 49.8 dB. The blue component represents out of band (OOB) noise. The MATLAB script was used to compute SNR removes the 2nd and 3rd

harmonic distortion tones [15]. This is done to get an indication of the linearity of the modulator at lower input levels before distortion sets in at high output levels. Overall the simulation results indicate an ENOB of around 8 bits.

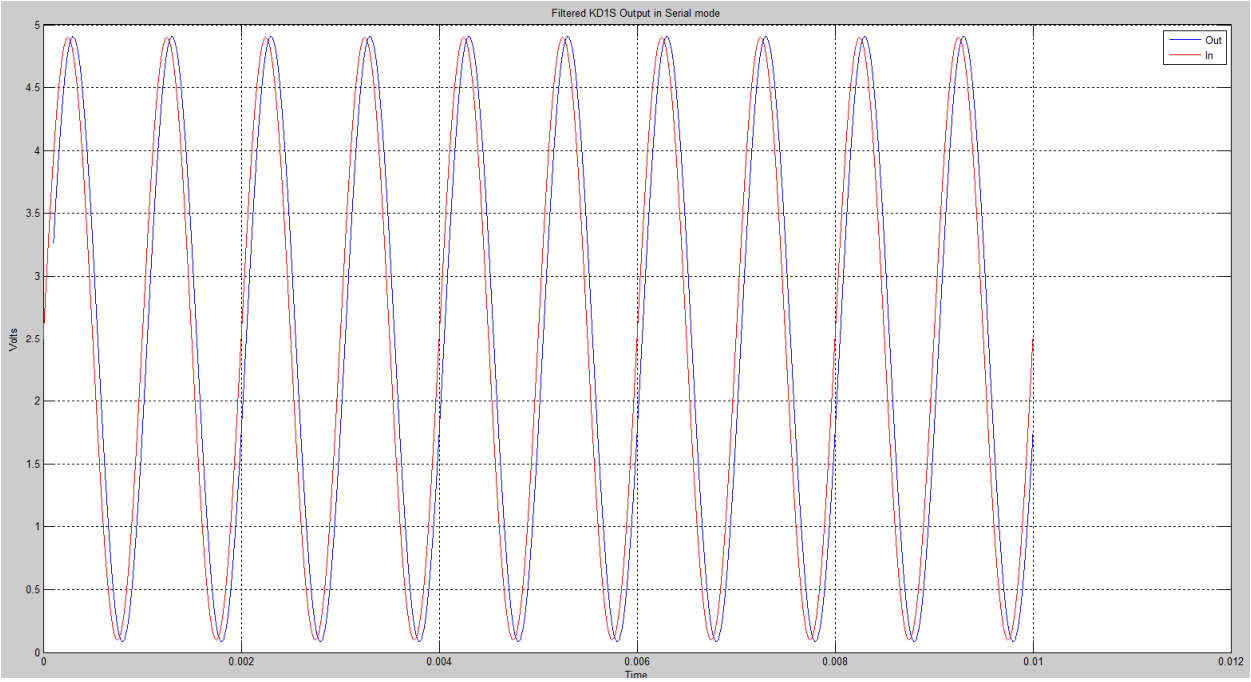


Figure 4.14 – Reconstructed output (blue) and input (red).

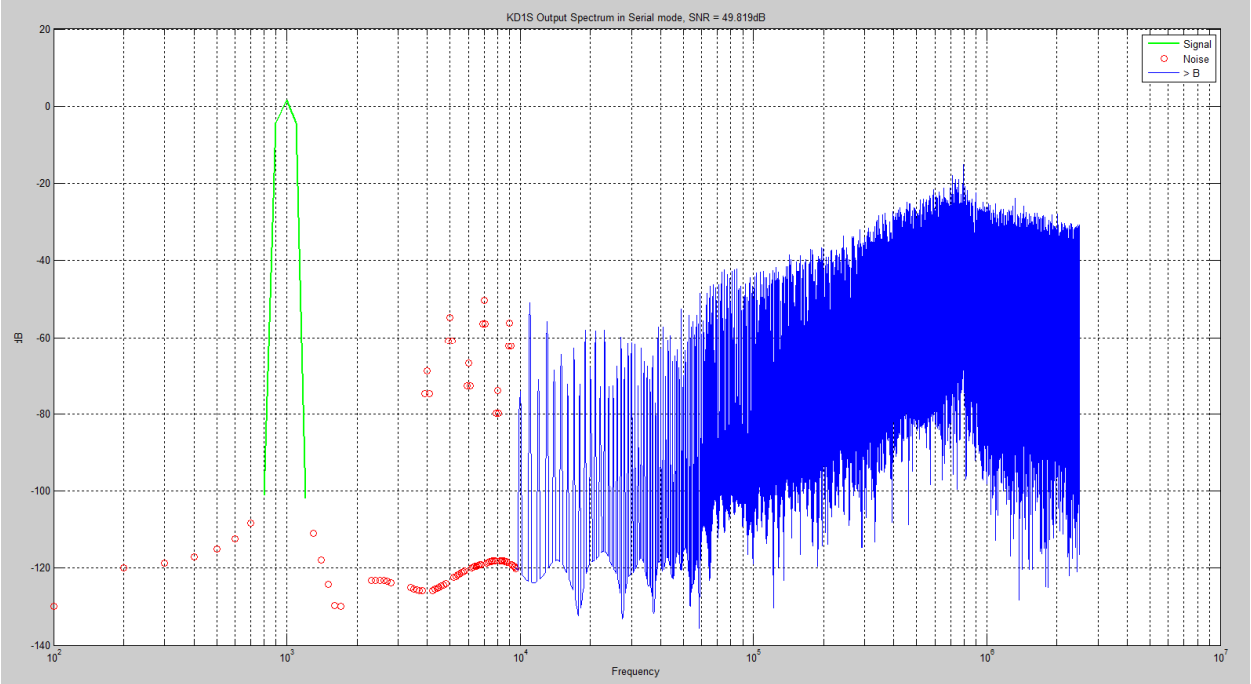


Figure 4.15 – FFT of modulator output with SNR bandwidth (red) and out of band noise (blue).

Measurements

Ultimately, simulation results need to be validated with real world measurements to verify true circuit performance. For a low power IC this is difficult since optimization for low power reduces the ability to drive off chip loads. As a result the test set-up was carefully optimized to ensure that test data is meaningful and accurate. The test set-up is shown in Fig. 4.16. This set-up is used to measure the harmonic distortion of the filtered output signal using the oscilloscope's software FFT feature. This harmonic distortion measurement accurately reflects the SNDR of the modulator. The set-up can also measure current consumption of the modulator. A carefully constructed "deadbug" style breadboard was used to reduce the effect of parasitic capacitances. This circuit is shown in Fig. 4.17. There is an onboard clock generator, an LTC1799 which has a variable frequency output

between 1 KHz and 33 MHz [16]. A precision 25 turn potentiometer is used to adjust the frequency. All circuitry is properly bypassed with a combination of electrolytic, film and ceramic capacitors to ensure low source impedance at all frequencies.

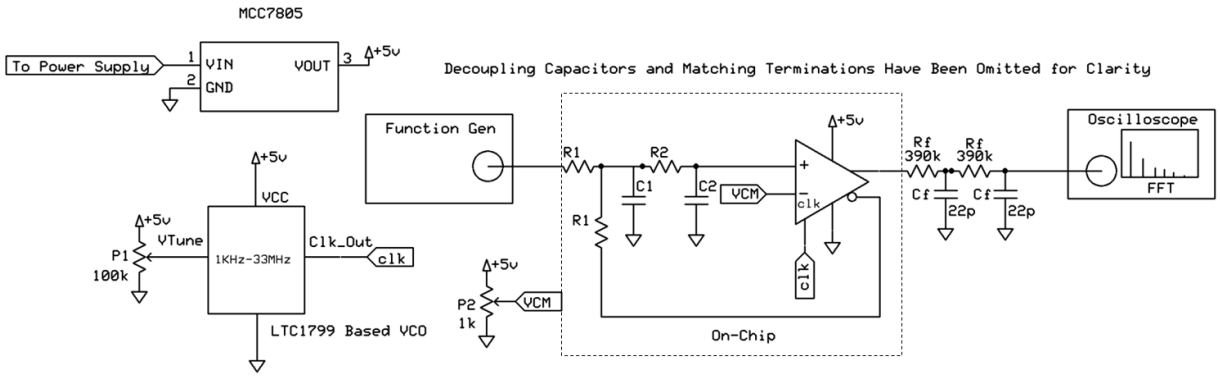


Figure 4.16 – Simplified schematic of test set-up.

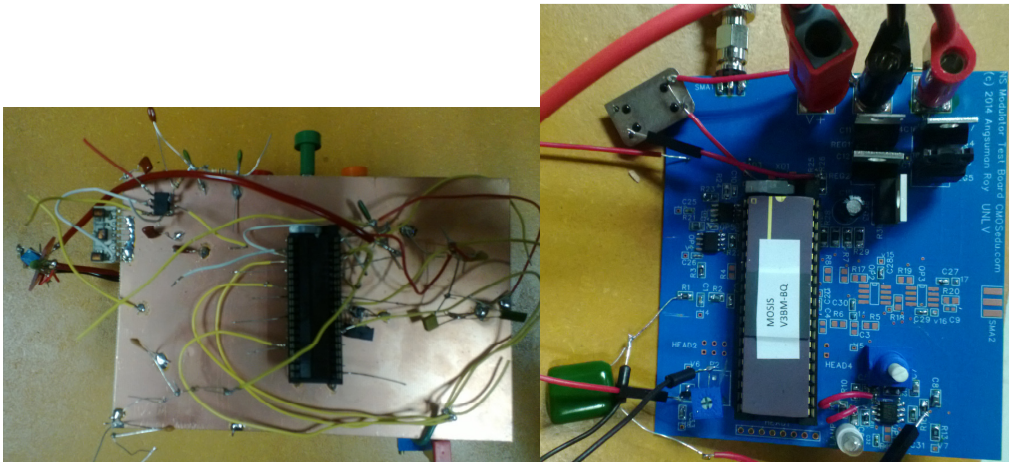


Figure 4.17 – "Deadbug" [17] test board (left) and PCB (right).

Using this test set-up and its variations, the DC transfer function, differential nonlinearity, power consumption and harmonic distortion were measured. The DC transfer function is shown in Fig. 4.18. For this set-up a stable variable voltage source was applied to the input and the resulting output voltage was measured. Both input and output voltages are measured using an Agilent 34405A 5 ½ digit multimeter. From the transfer function it is apparent the linear region falls between 0.6V and 4.5V. The applied input signal should be bounded within these limits for accurate conversion. A slight gain error is also apparent, but this should not be an issue after software calibration.

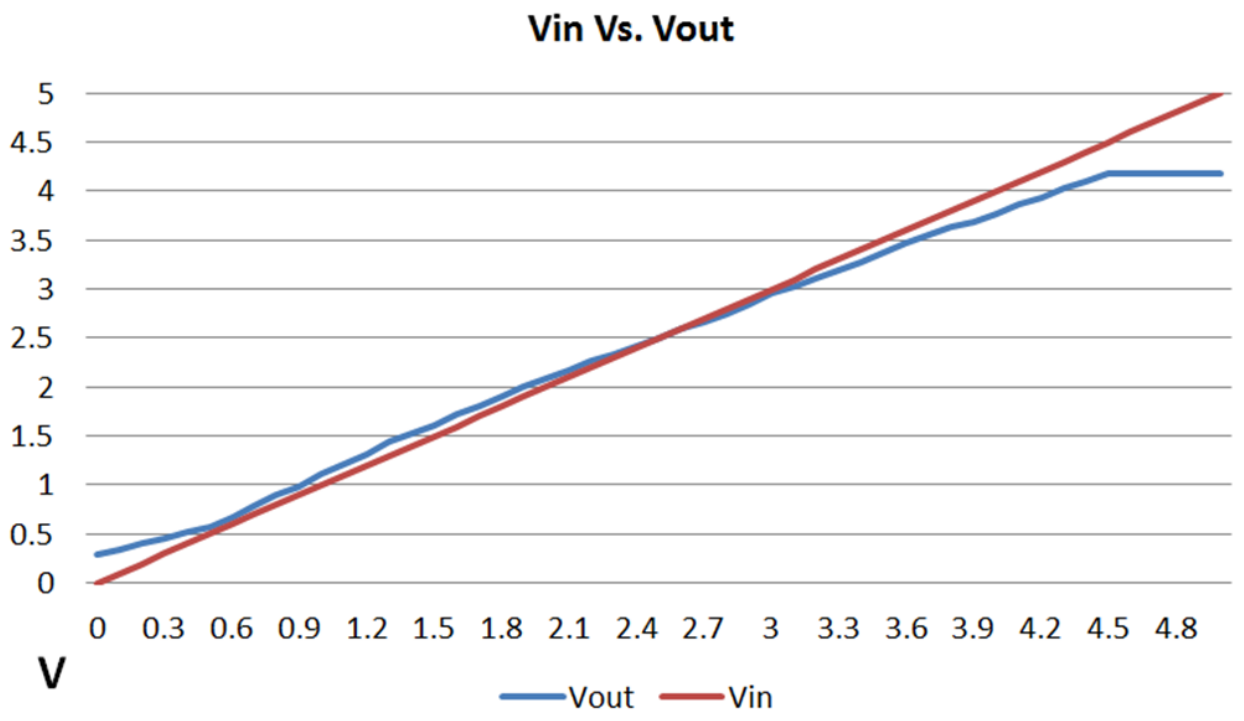


Figure 4.18 – Measured DC transfer function.

The differential nonlinearity (DNL) of the modulator can be obtained from the DC transfer function as done in Fig. 4.19. The units on the Y axis are percentages. The DNL is a measure of the change in linearity between each consecutive point on the DC transfer function. In essence, it can be viewed as a derivative of the DC transfer function. Traditionally DNL is not used to characterize sigma delta ADCs because the output is not static. For this measurement, significant averaging is used which makes the output nearly static for each data point. Examining the DNL data, it is clear that the modulator is quite linear between 0.6 V and 4.2 V which is to be expected from the DC transfer function. Between the 0.6 V and 4.2 V range, the DNL is kept within 0.4%. This indicates that the AC performance should be quite good.

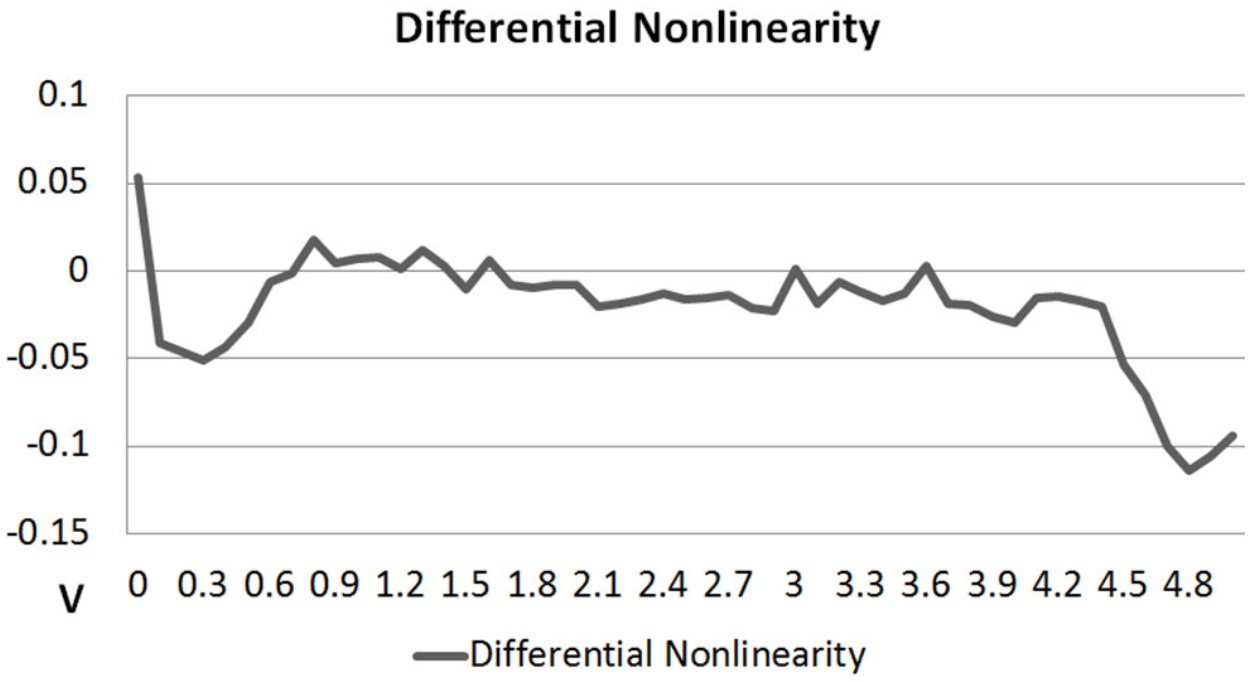


Figure 4.19 – Measured differential nonlinearity (DNL).

In order to maximize AC performance the test signal was restricted within the 0.6 V to 4.5 V input range. The test signal had peak amplitude of 1.5 V with a 2.5 V DC offset. This centers the sine wave about the 2.5 V common mode voltage applied to the modulator. The input frequency was varied from 10 Hz to 5 KHz. The clock frequency was set to 10 MHz. The modulator's digital output is filtered by a 2nd order 18 KHz low-pass filter with a Q (damping factor) of 0.33. This sets the oversampling ratio to 555 although this filter is not close to an ideal filter. In an ADC application with digital filtering, the nearest convenient OSR that can be implemented is 512 (2^9). The reason the input signal is limited to 5 KHz is due to the desire to include at least the 3rd harmonic component. Otherwise, the SNDR specification will be artificially inflated at higher frequencies due to the harmonic distortion being filtered out. A graph showing the level of individual harmonic components and the total harmonic distortion as a function of frequency is shown in Fig. 4.20. The Y axis shows the voltage amplitude in dB below the fundamental frequency. The X axis shows the frequency of the input signal.

This data was harvested using an 8-bit oscilloscope which limits the resolution to 50 dB although some averaging techniques within the oscilloscope can extend the resolution by a few dB. The measured THD of the modulator is less than 40 dB below the fundamental for all tested frequencies. It is interesting to note that the 2nd harmonic component is at -55dB for some frequencies. This could allow for a significant increase in resolution in applications where the signal bandwidth is low or centered around a specific frequency. Generally the lower order (2nd and 3rd) harmonics are the most dominant. In this modulator, the fact that the 2nd harmonic is the lowest implies there is some sort of cancellation due to symmetrical circuit structure which is generally seen in differential

amplifier topologies. The reason for the cancellation has not been investigated further due to limited test equipment availability. The peak ENOB achieved from this test set-up is 7.8 bits which makes this modulator perfect for an 8-bit ADC.

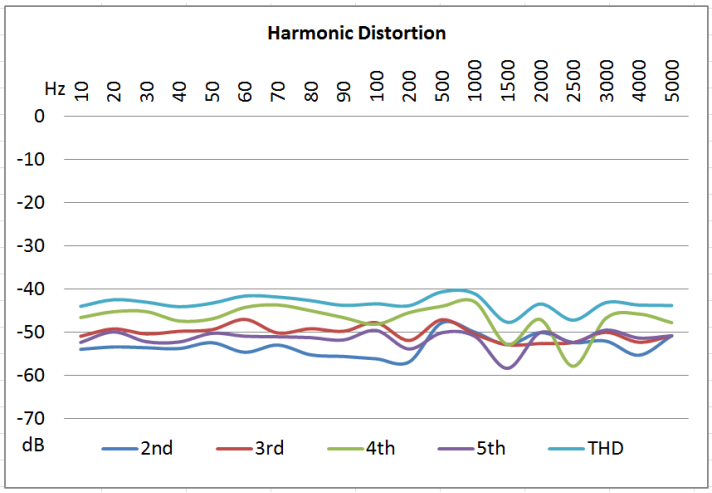


Figure 4.20 – Measured total harmonic distortion (THD) and individual components.

The power consumption of this sigma-delta modulator is quite low. The test set-up used an Agilent 34405A 5 ½ digit multimeter connected in series with the test circuit [18]. The power supply voltage was then adjusted to ensure that the voltage appearing at the test circuits VCC node was exactly 5V. This was done to reduce the error resulting from the series insertion voltage drop of the multimeter although this was found to be negligible. The power consumption tests were done with the modulator driving the passive output filter as well as a 10x scope probe to reflect a real world load. The worst case load impedance is at high frequencies relative to the filter's passband which is roughly 200 kΩ. Under these test conditions, with a 10 MHz clock the measured supply current varied from 12.9 uA to 30 uA. At the extreme ends of the transfer function the modulator's output is switching less often which results in the lower average current of 12.9 uA. At the middle of

the modulator's transfer function, the output is switching constantly at a rate that is close to the clock frequency. This results in the maximum 30 uA current consumption. A table summarizing all key measured performance parameters is shown in table 4.2.

Performance Parameter	Value	Test Conditions
Supply Voltage	1.8V – 5.5V	
Supply Current	12 uA – 30 uA	5V VCC
Power Consumption	64.5 uW – 150 uW	100 uW typical
Input Voltage Range	0.6 V – 4.2 V	Linear Range
Differential Non-Linearity	Within 0.4%	0.6 V – 4.2 V Input Range
Tested Frequency Range	10 Hz – 5 KHz	1.5 V peak with 2.5 V DC Offset
Clock Frequency	10 MHz	
Nyquist Rate Bandwidth	18 KHz	2nd order filter has significant components outside of passband.
Oversampling Ratio	512	Rounded to nearest convenient value.
SNDR	48 dB @ 1.5 KHz	1.5V peak with 2.5 V DC Offset
ENOB	7.8 @ 1.5 KHz	1.5V peak with 2.5 V DC Offset

Table 4.2 – Summary of Measured Parameters

Chapter 5 Switched-Capacitor Sigma-Delta Modulators

Switched-Capacitor Basics

Although continuous time sigma delta modulators can offer good performance, they have all the drawbacks inherent in passive components. These include large layout area and process variations. Furthermore, filter frequencies are fixed by passive component values and cannot be changed. All these drawbacks can be solved through the use of discrete-time switched capacitor (SC) circuits. Layout area is significantly reduced because high value resistors are replaced with MOSFETs and small capacitors. Filter frequencies can be changed by changing the clock frequency of the switched capacitors. Process variation effects are reduced because switched capacitor circuits do not depend on actual capacitor values but rather on their relative matching which is quite good in any IC process.

The fundamental concept in switched capacitor circuit techniques is that resistors can be replaced by MOSFET switches and capacitors [19]. The basic structure of a switched capacitor resistor is shown in Fig. 5.1. An SC resistor is formed by two switches in series and a capacitor connected between the junction of the switches and ground. The type of switch shown in Fig. 5.1 is a transmission gate (TG). This type of switch closely approximates an ideal switch because it can pass signals from ground level to the positive supply level, VDD. The value of the equivalent resistance is given by the equation in Fig. 5.1. The value of the resistance can be easily varied simply by changing the clock frequency.

However, this clock frequency has to be generated in a particular way for proper operation of the SC resistor.

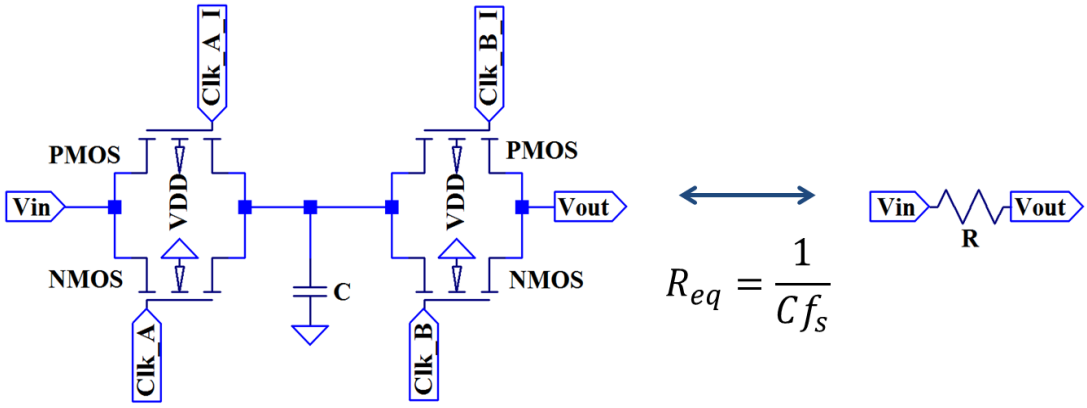


Figure 5.1 – Structure of switched-capacitor resistor and its relationship to a lumped resistor.

Four different clocks are needed for proper operation of a TG based SC-resistor. Two non-overlapping clocks are needed for each switch. These are labeled “Clk_A” and “Clk_B” in Fig. 5.1. Non-overlapping (NL) means that the clocks are neither high nor low at the same time. This prevents the capacitor from discharging into the output while it is being charged by the input signal. An inverted version of each NL clock is also required to turn on the PMOS portion of the TG. These clock signals and the zoomed view of their edges is shown in the simulation in Fig. 5.2. The short dead-time between clocks is clearly visible in Fig. 5.2b. This delay is the shortest that is practically possible in this process without causing overlap. Generally, there is a trade-off between shortening the delay and the risk of overlap. The simulation indicates that there is enough delay and overlap should not be a problem.

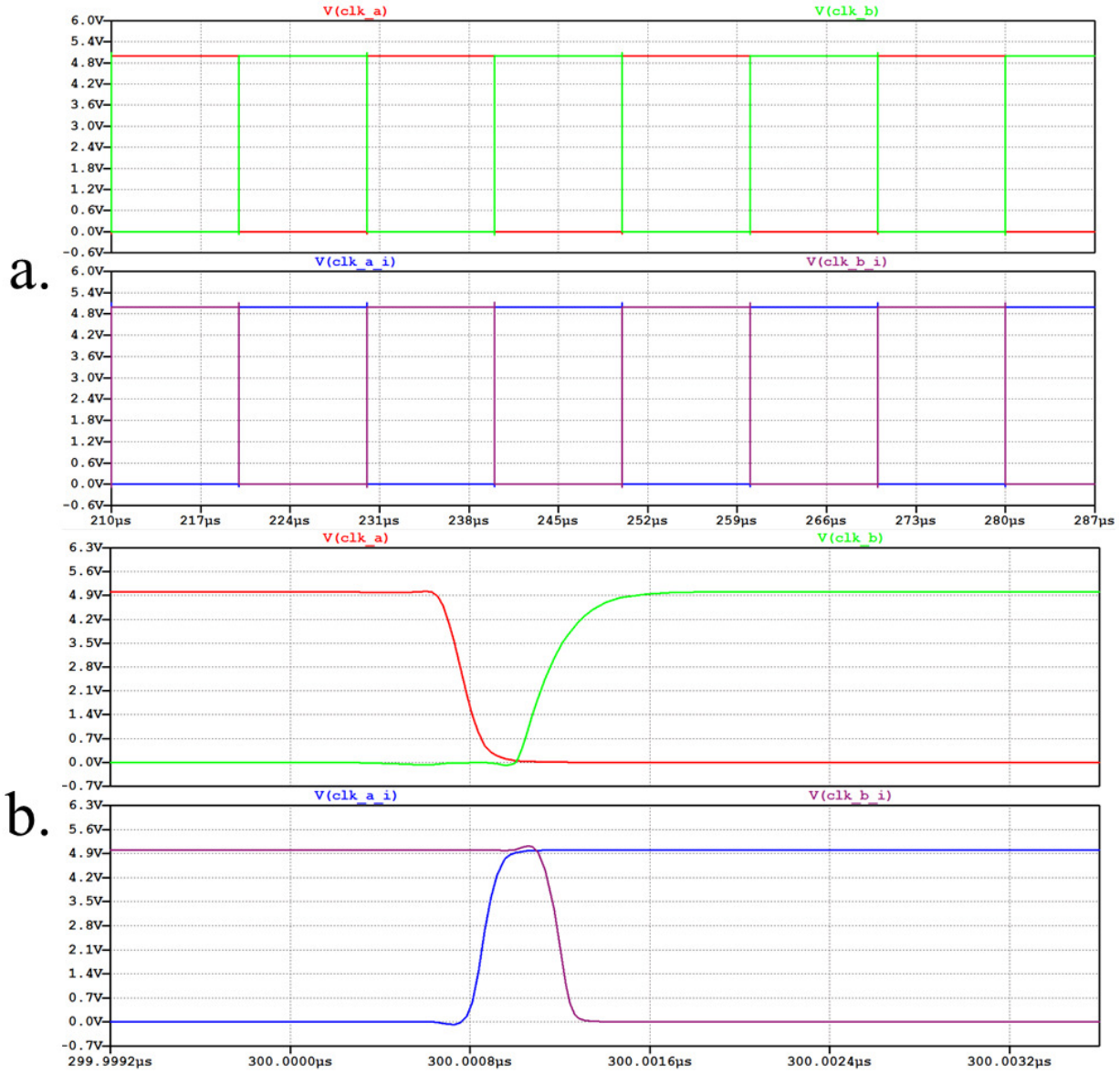


Figure 5.2 – Clock Signals (a) and zoomed view of edges (b).

Circuit Design

Power reduction was the main goal in the design of this NL clock generator. This is accomplished by using both minimum size devices and the minimum number of devices possible. The short delay is due to this fact and was not the primary design goal. Generally, it is better to have more delay to prevent any possibility of overlap [20]. The logic-level schematic of the NL clock generator is shown in Fig. 5.3. The circuit is made up of two NOR gates and five inverters. A NOR gate outputs a logic-high if both inputs are logic-low otherwise it outputs a logic-low. Each clock output switches state after a delay time set by the number of inverters in the feedback loop. If there were no inverters, then the outputs would simply toggle high and low with no delay between them. The minimum number of inverters in each loop is two although generally more are used to ensure that there are no overlapping edges. In this design, the minimum delay was chosen to reduce power consumption. The simulation in Fig. 5.2 shows that this is sufficient delay to prevent overlap. Generally, the outputs are buffered with an inverter that is outside the feedback loop to prevent loading from changing the delay time of the inverters. In this design, the loading is light enough that additional buffering is not needed.

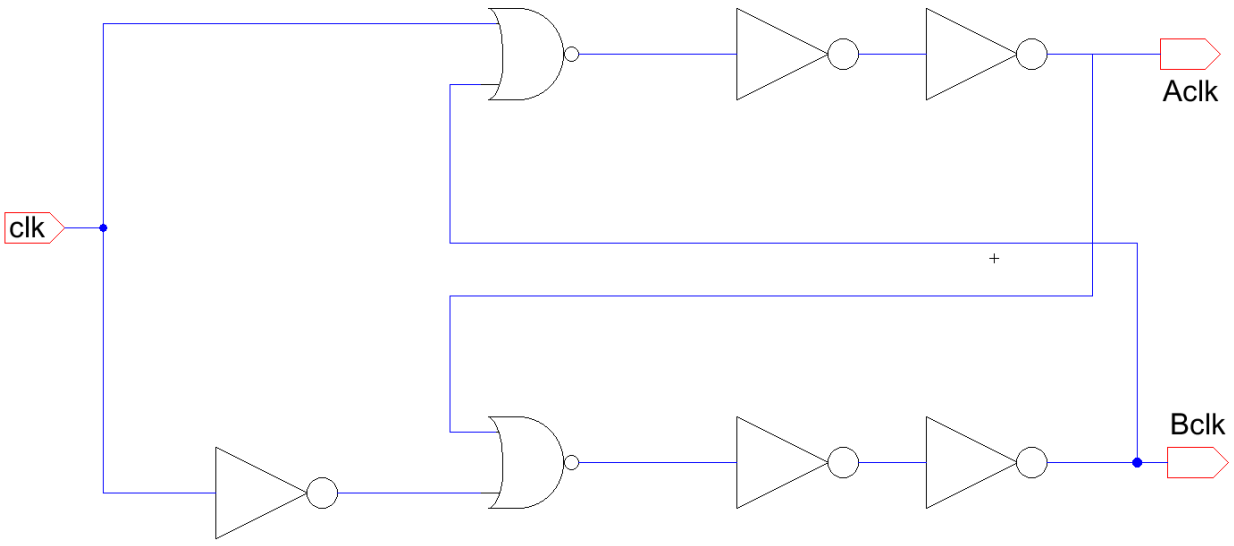


Figure 5.3 – Logic-level schematic of NL clock generator.

The NL clock generator can be built using either NOR or NAND gates. The reason NOR gates were chosen is because of reduced drive strength due to the PMOS devices being in series. This reduced transconductance reduces both power consumption and reduces the speed of the NOR gate. Reducing the speed increases the delay of the NOR gate which allows for minimizing the number of delay inverters. The schematic and layout of the NOR gate is shown in Fig. 5.4. All devices are the minimum size of 1.8 um / 0.6 um. The layout area excluding the metal connections is 28 um x 15 um.

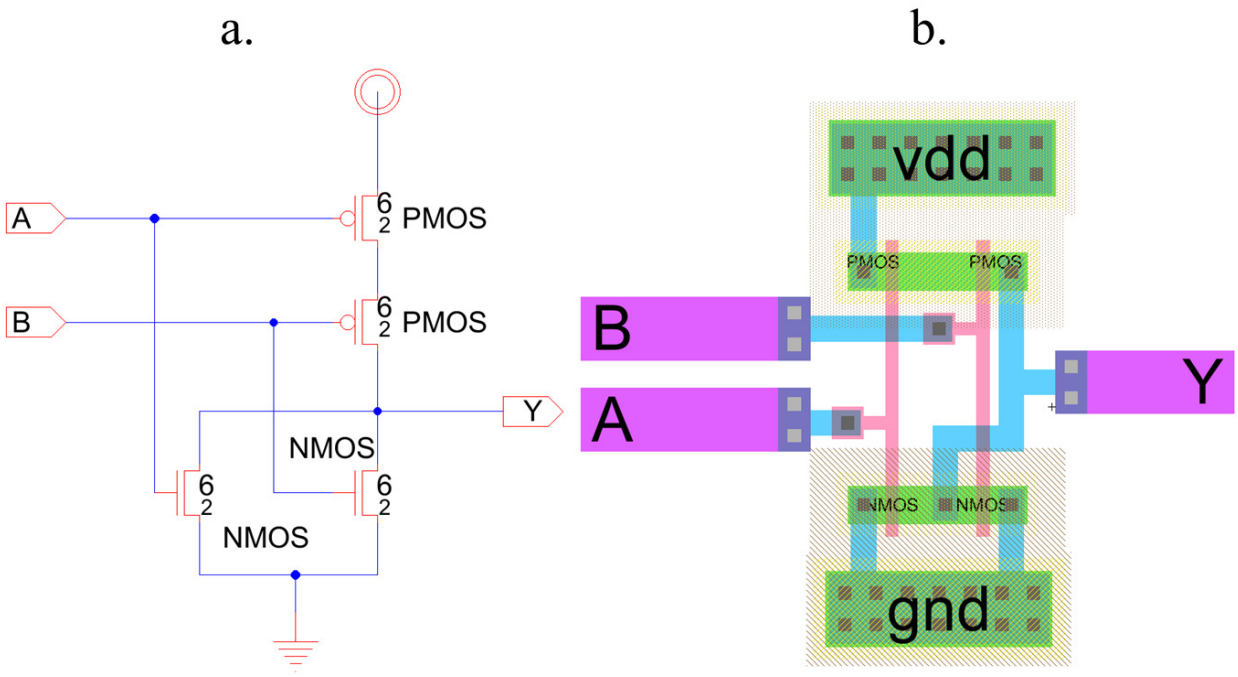


Figure 5.4 – Schematic (a) and layout (b) views of NOR gate.

The inverters are also minimum size devices. As a result of this, the NMOS devices have more drive strength which results in a switch point that is around 1.8V and not the optimal 2.5V. This should not be a concern in this design. The schematic and layout of the minimum size inverter is shown in Fig. 5.5. The total layout area excluding the metal connections is 8 um x 20 um.

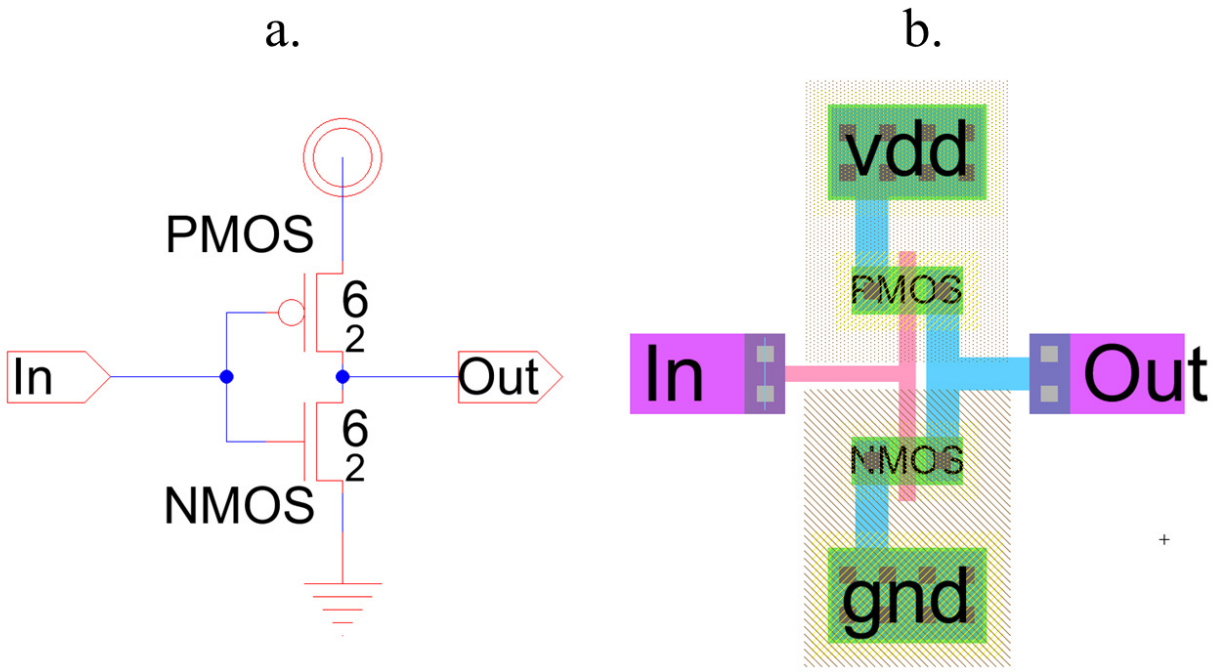


Figure 5.5 – Schematic (a) and layout (b) views of inverter.

Once a suitable NL clock is designed, the continuous time elements of the sigma-delta modulator need to be adapted to their discrete time counterparts. This is done by replacing the resistors in Fig. 4.1 with SC-resistors. The schematic of the passive filter network formed of SC-resistors and capacitors is shown in Fig. 5.6a. The capacitors in the SC-resistors were sized according to the equation in Fig. 5.1. A nominal clock frequency of 10 MHz was chosen. At this frequency, the equivalent resistances are 100 kΩ and 1 MΩ for R1 and R2 respectively as shown in Fig. 4.1. The layout of the SC filter network is shown in Fig. 5.6b. The majority of the layout is taken up by the capacitors. The TG switches occupy a small area in the top left corner. The total layout area is 344 um x 195 um.

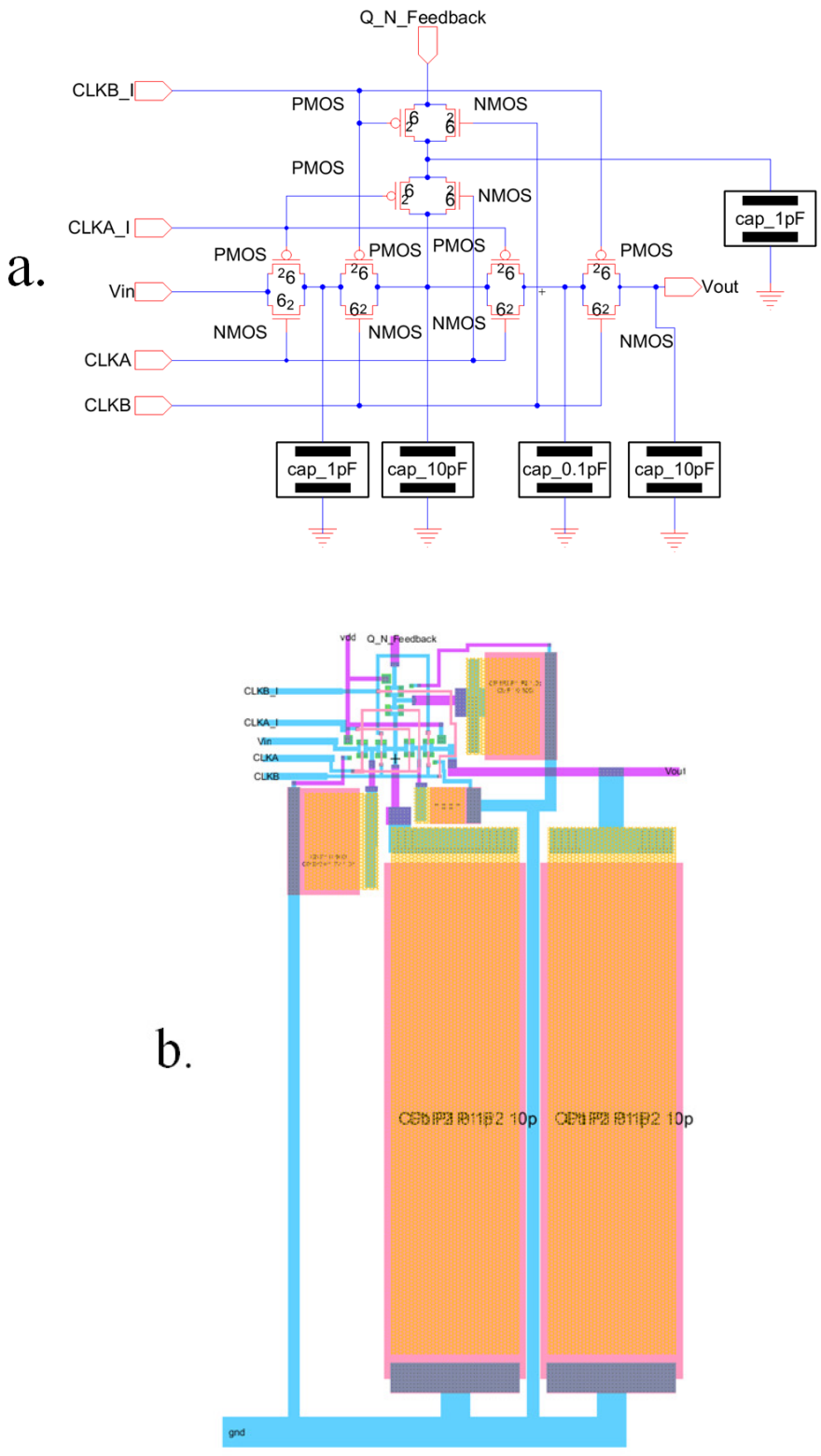


Figure 5.6 – Schematic (a) and layout (b) of SC-resistor based passive filter network.

The complete block level schematic of the sigma-delta modulator is shown in Fig. 5.7. This schematic combines the three main sections, the NL clock generator, the SC filter block, and clocked comparator into a sigma delta modulator. The two inverters are used to generate the inverted clock signals required by the PMOS devices in the TGs. The clocked comparator is the same as the one described in chapter 4 and shown in Fig. 4.7 and Fig. 4.8. The layout of the complete modulator is shown in Fig. 5.8. There was no optimization done to reduce the layout area as the goal was for functional verification and not minimal area. The total layout area is 405 um x 385 um. It should be possible to reduce this area by at least 25% with better layout techniques.

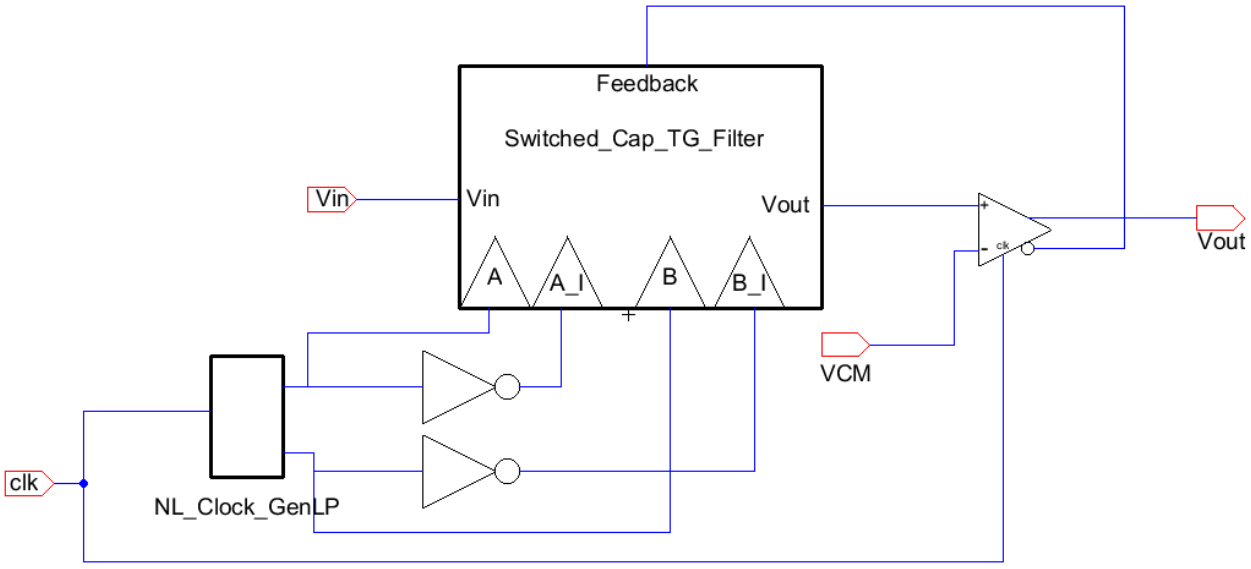


Figure 5.7 – Complete schematic of SC-based sigma-delta modulator.

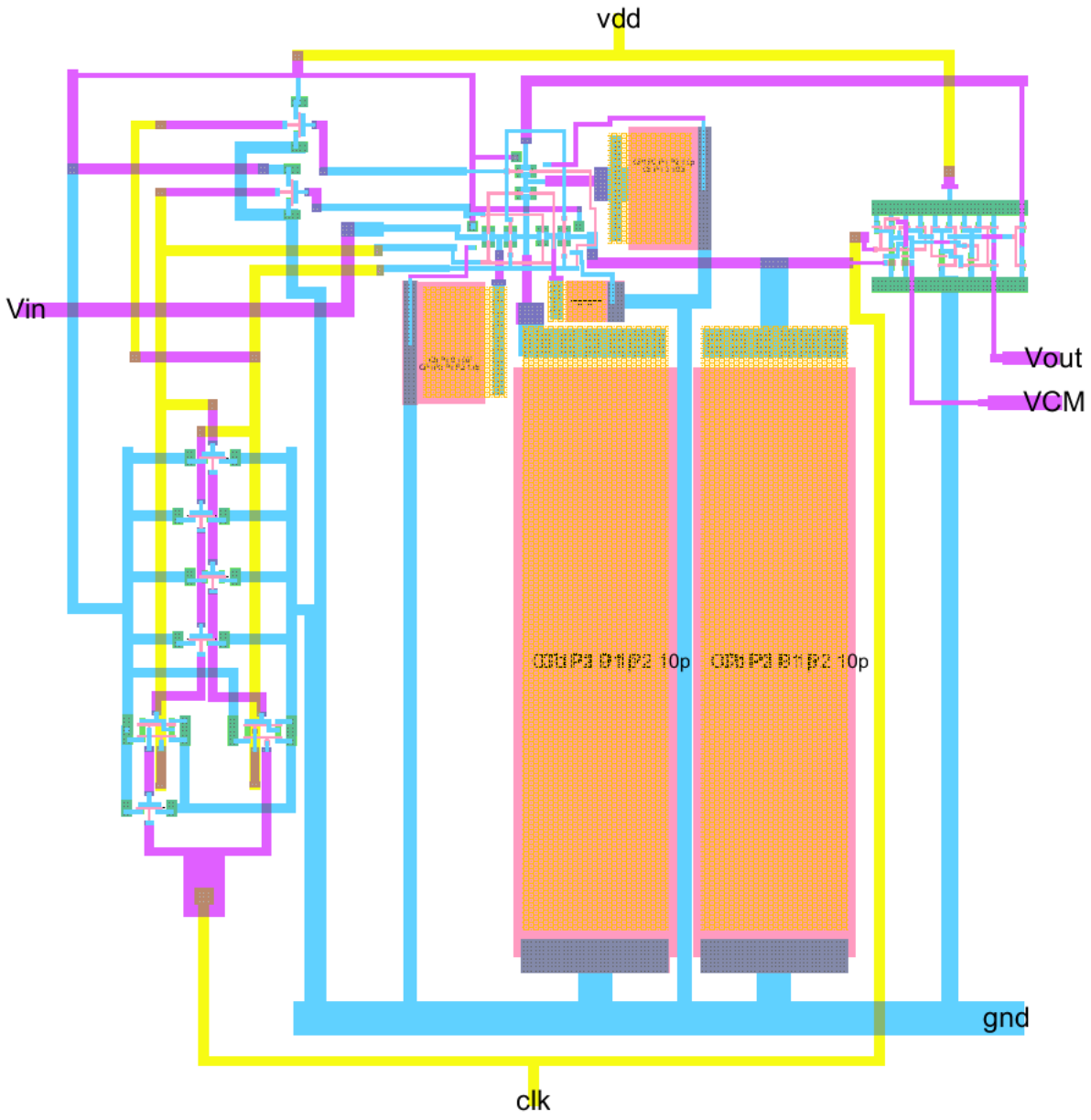


Figure 5.8 – Complete layout of SC-based sigma-delta modulator.

Simulations were performed in LTSpice to verify the functionality of the SC sigma-delta modulator. The most basic simulation of an ADC's performance, the DC transfer curve is shown in Fig. 5.9. For a sigma-delta modulator, this needs to be done by applying a very slow ramp signal and filtering the output. It is apparent from the plot that there is a gain error since the output has a different slope from the input signal. Although some of this

error is due to the time delays resulting from the passive output filter, this SC sigma-delta modulator has more gain error than the equivalent continuous time version described in chapter 4. This large gain error could be due to charge-injection by the MOSFETs into the switched capacitors [19]. This is a trade-off due to the emphasis on simplicity and low power. Despite the gain-error, the output is very linear which indicates good AC performance. Furthermore, gain error can be trimmed in software and some sort of calibration should be used for any application requiring DC precision.

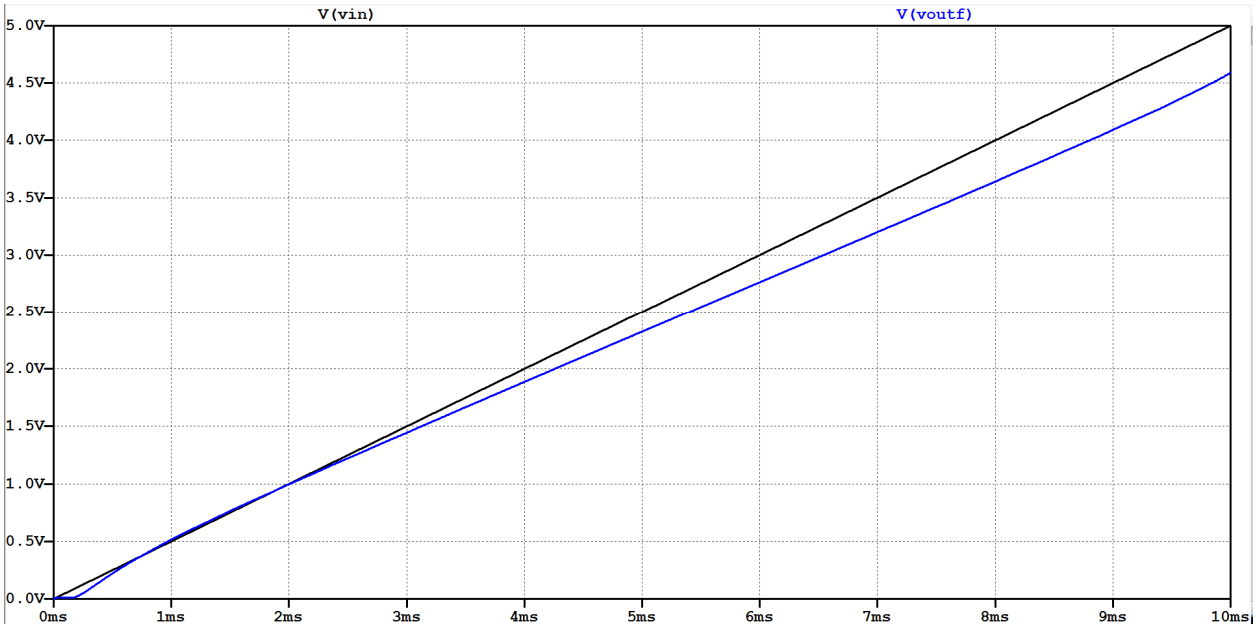


Figure 5.9 – DC transfer curve of SC-sigma-delta modulator.

The AC performance of the SC sigma-delta modulator was simulated by applying a 1 KHz sine wave to the input with a DC offset of 2.5V and amplitude of 2.1V. This ensures that the level of the input signal is within the linear range of the modulator's transfer function. The simulation ran for at least 10 cycles in order to ensure good FFT resolution. A Hann-windowed FFT of the digital output and the output after passing through a 2nd order 16 kHz

filter is displayed in Fig. 5.10. The noise-shaping is clearly visible in the 1-bit output. After filtering the noise floor decreases to below 100 dB and it is clear that most of the non-linearity is due to the remaining harmonics. Due to the time it takes to run these types of simulations, only a few key points were simulated and ultimately measured results are needed get an accurate portrayal of this modulator's performance.

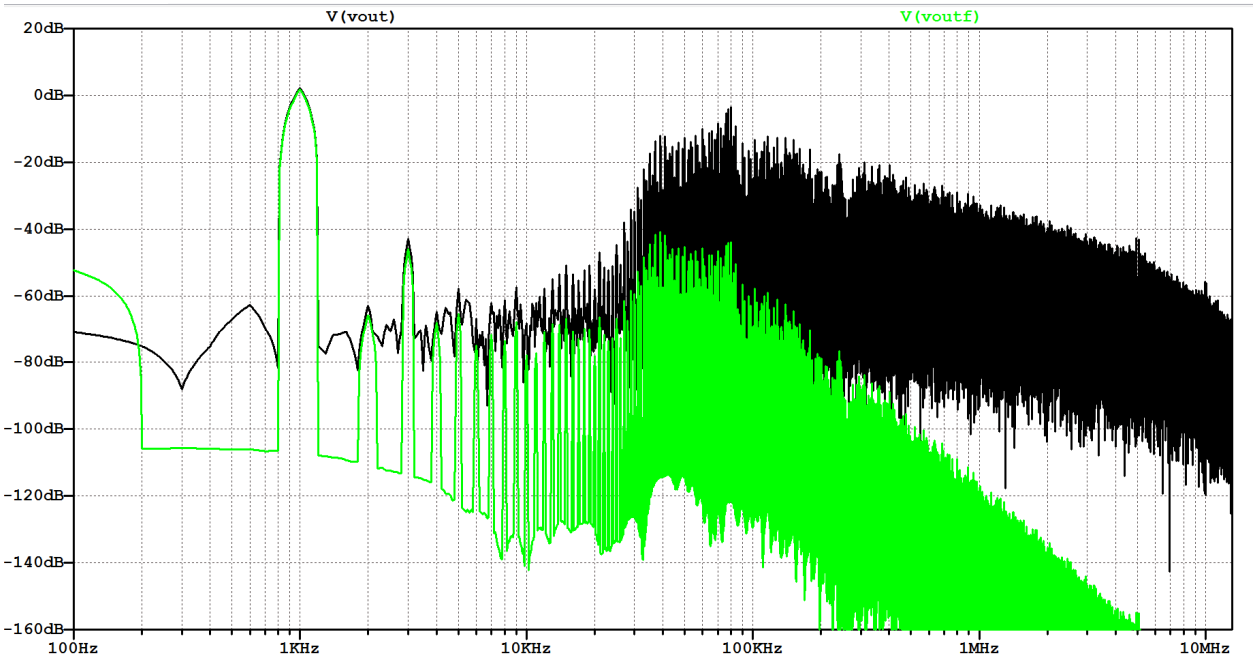


Figure 5.10 – FFT of 1-bit output (Vout) and filtered output (Voutf).

The chip was fabricated by the MOSIS service and packaged into a ceramic 40-DIP package. This package allows for ease of testing. The complete chip is shown below in Fig. 5.11. The SC sigma-delta modulator is in the black box. The other circuits are different sigma-delta modulators. To ensure stable power supply rails, 30 pF of capacitance is located on chip between VDD and ground rails. A photograph of the sigma-delta modulator by itself is shown in Fig. 5.12. Both images were obtained with a metallurgical microscope at a magnification of 40X.

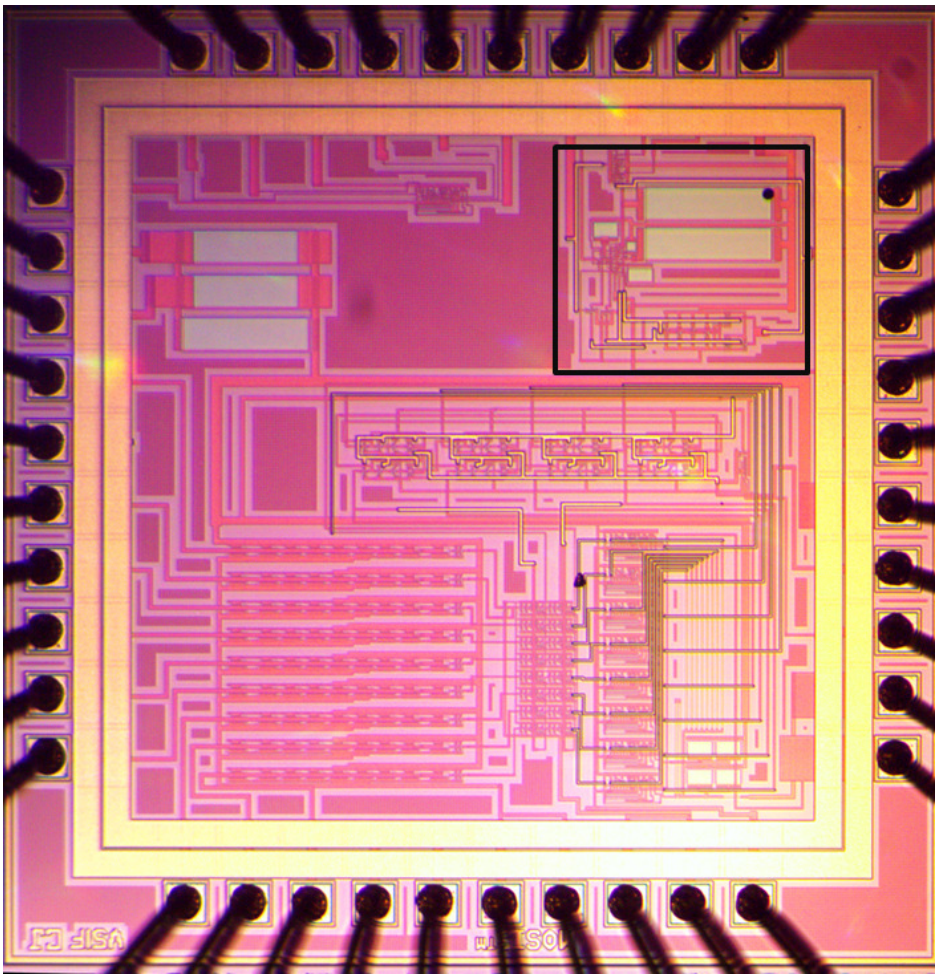


Figure 5.11 – Die photograph of complete chip with ∑-Δ modulator in black box.

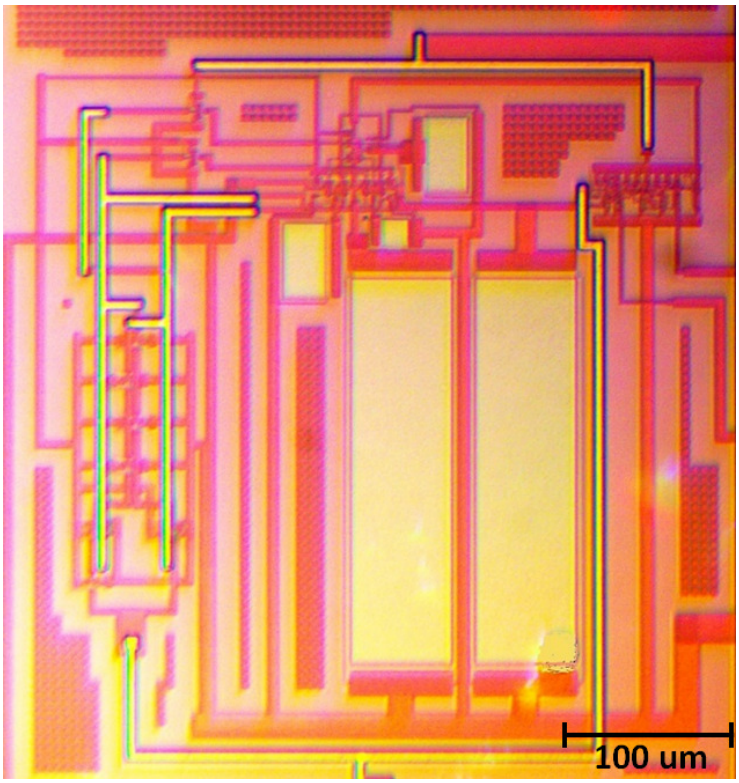


Figure 5.12 – Zoomed view of SC sigma-delta modulator.

Measurements

Measurements were performed on the fabricated chip in order to verify functionality and performance. The test set-up was created by soldering the chip and peripheral components onto a copper-clad board. This style of construction is often referred to as “dead-bug”. For this set-up, a socket was used in order to prevent damage to the chip by directly soldering to its leads. There should be no adverse effects due to the use of a socket because this chip operates at low speeds. This test set-up is shown in Fig. 5.13. The use of the copper ground plane reduces noise and allows for higher speed operation by reducing parasitic inductances. Power is applied to the red and black BNC jacks on the left side. A DIP switch is used to turn on each circuit within the IC individually. Current sense

resistors are used to measure the current in each individual circuit, although measurements were also made by breaking power connections and running them through a high quality digital multimeter. All power connections are locally bypassed with 100 pF capacitors which connect directly to the ground plane. They are not visible in Fig. 5.13 because they are under the chip socket. The common-mode voltage can be precisely set using the 10 turn potentiometer. The other pot is used to set an internal clock generator for a different circuit on the chip. The signal input and output connections are routed through BNC connectors as close as possible to the chip to maintain signal integrity. All inputs are parallel 50 ohm terminated while all outputs are series 50 ohm terminated. A passive output filter made up of discrete components is used to convert the digital bit stream into an analog approximation. The capacitors in this filter use an NPO dielectric which ensures low distortion and stable capacitor value [21]. All these precautions allow for taking sensitive measurements to quantify ADC performance.

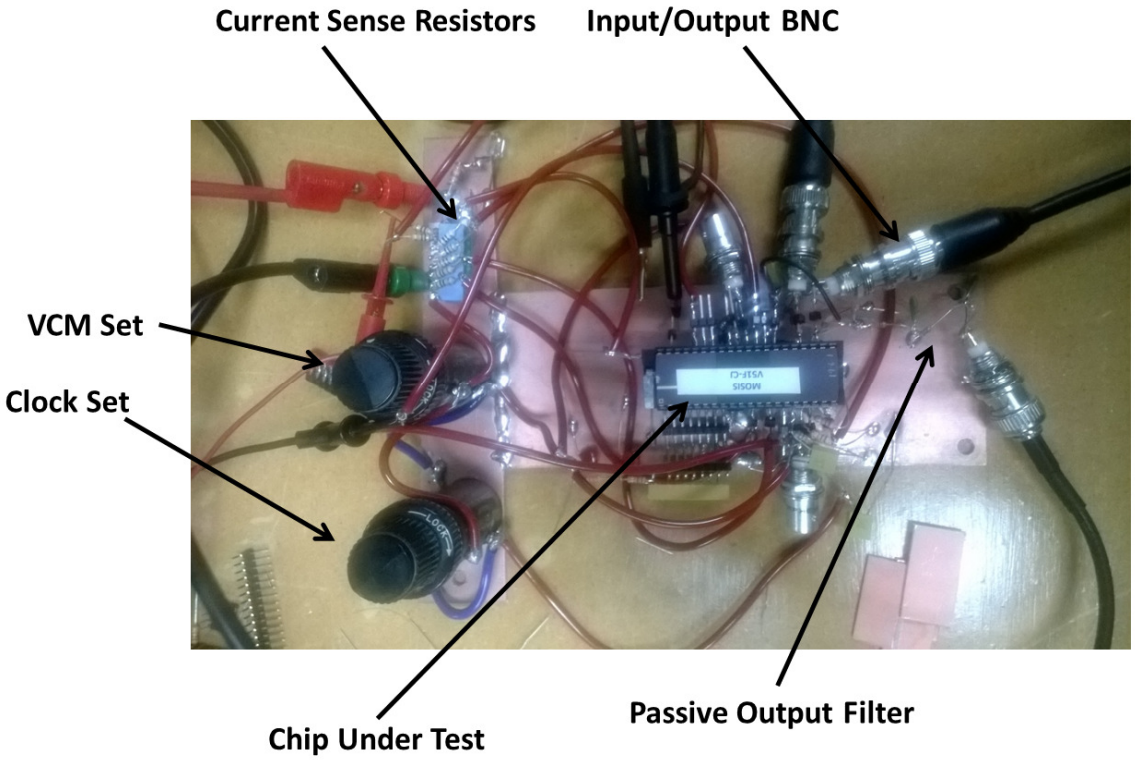


Figure 5.13 – "Deadbug" test set-up.

The best test for the linearity performance of an ADC is the signal-to-noise and distortion ratio (SNDR). SNDR directly gives a measure of the effective number of bits [22]. The raw data for SNDR measurements was obtained using a PC based oscilloscope with 14-bit vertical resolution. This is a much higher resolution than anticipated for the circuit under test and therefore the results will not be limited by the test equipment. Furthermore, the distortion of the input signal source was tested and had a THD of -75 dB. The amplitude of the input signal was 0.75 V peak centered around a 1.25 V DC offset in order to ensure that the signal is within the linear input range. Since low power consumption is one of the main goals, the SNDR testing was done at a 2.5V VDD which is compatible with LVCMOS logic levels.

The use of SC filters in this sigma-delta modulator result in the filter cut-off frequencies being dependent upon the clock frequency. This requires precautions to be taken when creating an SNDR graph so that each data point is equally comparable. The clock frequency needs to be adjusted to ensure that there is no attenuation for the input frequency and also no attenuation of harmonics within the desired bandwidth. Otherwise, this would artificially inflate SNDR numbers for higher frequencies. To prevent this, each data point was obtained under the condition that the SC filter's corner frequency is above the first five harmonics to ensure a realistic SNDR value.

The SNDR in dB as a function of frequency is shown in Fig. 5.14. This data was obtained by summing the 2nd through 5th harmonics and using the THD formula, which is

$$THD_f = \frac{\sqrt{V_2^2+V_3^2+V_4^2+V_5^2}}{V_1} \tag{5.1}$$

Where V_1 is the RMS amplitude of the fundamental and V_2 to V_5 are the RMS amplitudes of the harmonics. The RMS of the sum of the harmonics is taken and divided by the RMS amplitude of the fundamental. This ratio can then be converted into dB to yield a SNDR which is commonly given in dB. Usually the noise power within the bandwidth is added to this measurement, but in this case due to the narrow bandwidth and the observed noise floor at -100 dB, this was not necessary. For passive sigma delta modulators, the noise level is comparable to that predicted by ideal equations. Rather, it is the distortion components that limit performance. The peak SNDR of 57.6 dB occurred for an input frequency of 400 Hz and a clock frequency of 1.024 MHz. This corresponds to an ENOB of 9.3 bits. Under

these conditions, the supply voltage and current were 2.5V and 2.7 uA respectively. From the SNDR plot it is apparent that the SNDR is above 50 dB (corresponding to ENOB of 8 bits) for most of the frequency range.

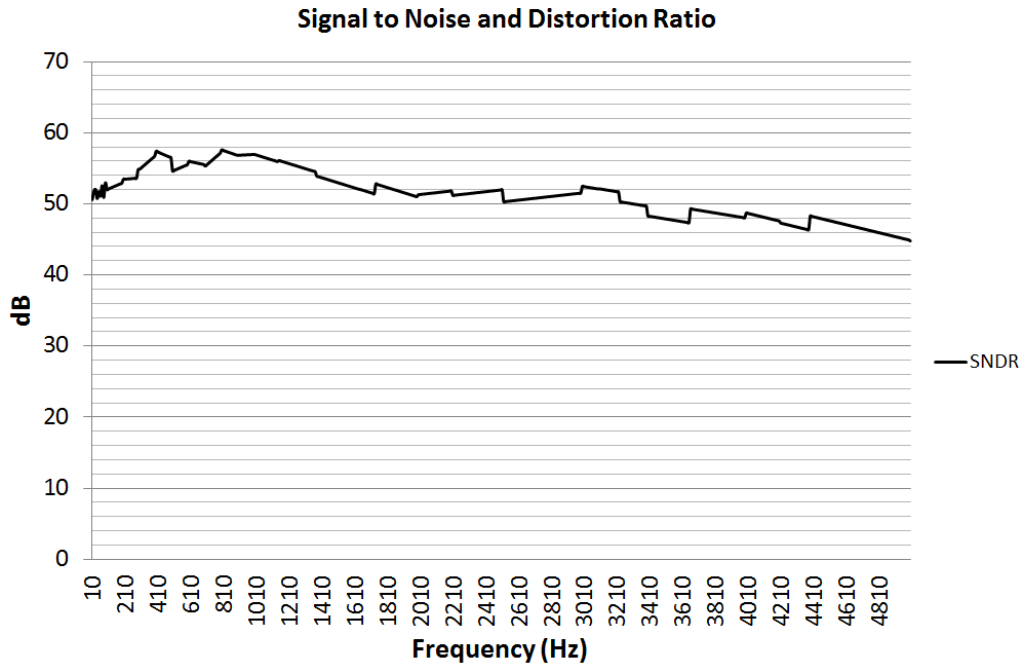


Figure 5.14 – Measured SNDR.

Since low power is the main goal, it is important to see how current consumption changes with supply voltage. The plot in Fig. 5.15 shows current consumption as a function of supply voltage. The clock frequency is kept constant at 1 MHz. The plot shows a parabolic shape which is expected for MOSFETs. To keep current consumption below 10 uA, the supply voltage needs to be restricted to 3.3V. Beyond 3.3V, the current consumption increases sharply. Overall, this circuit will have low power consumption in applications

where it is interfaced to LVCMOS. The circuit can be used for traditional 5V CMOS logic levels but power consumption will significantly increase.

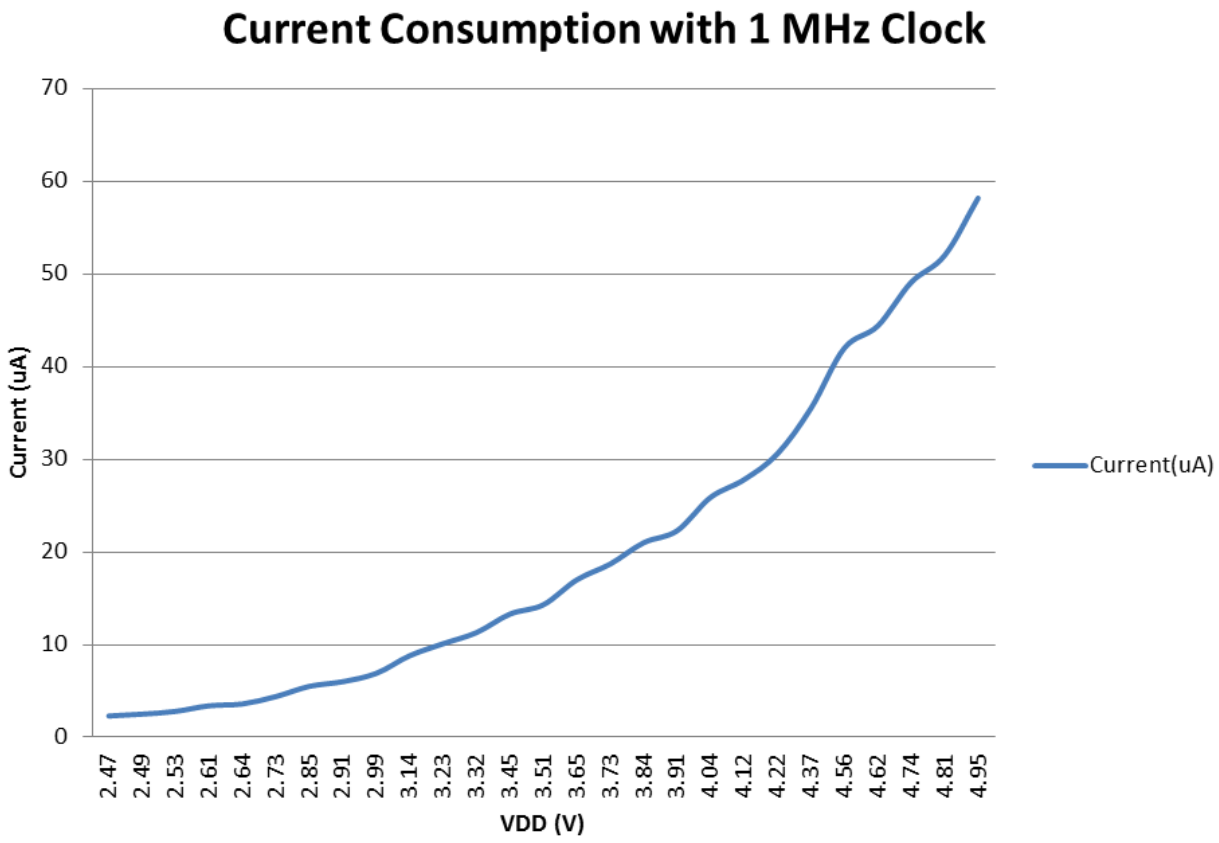


Figure 5.14 – Measured current consumption as a function of VDD.

Performance Parameter	Value	Test Conditions / Comments
Supply Voltage	2.4 V – 5.5 V	
Supply Current	2.47 µA – 58 µA	2.4 V-5 V
Power Consumption	6 µW – 319 µW	6.75 µW @ 2.5 V supply
Input Voltage Range	0.3 V – 4.5 V	Linear Range @ 5 V supply
Tested Frequency Range	10 Hz – 5 kHz	0.75 V peak with 1.25 V DC Offset
Clock Frequency	1 MHz	
Nyquist Rate Bandwidth	3 kHz	At 1 MHz Clock (varies with clock)
Oversampling Ratio	340 as tested	256 or 512 for practical digital filter
SNDR	57.3 dB @ 400 Hz	0.75 V peak with 1.25 V DC Offset
ENOB	9.3 @ 400 Hz	0.75 V peak with 1.25 V DC Offset

Table 5.1 – Summary of Measured Parameters

A summary of measured performance parameters is shown in table 5.1. The measured results show that this design is adaptable for a wide variety of situations. A comparison to other similar works found in the literature is shown in table 5.2. The FOM calculation is done with the equation,

$$FOM = \frac{Power}{2^{ENOB} * f_S * 2 * Bandwidth} \tag{5.2}$$

This equation allows comparisons to be made between ADCs with significantly different power consumption and resolution [23]. The units are in joules per conversion step. This FOM does not indicate that an ADC is suited for any particular purpose but rather is a good synthetic comparison between designs. Due to a lack of passive designs in the literature, the other two modulators compared are active designs. Overall, the proposed modulator offers very good performance when judged by its FOM. Additional details for the presented design are found in [31].

Parameter	Proposed 2nd Order SC ∑-Δ Modulator (this work)	2nd Order SC ∑-Δ Modulator in [29]	2nd Order SC ∑-Δ Modulator in [30]
Process	500 nm	180 nm	350 nm
Resolution (ENOB)	9.3 bits	10.6 bits	12 bits
Signal Bandwidth	3 KHz	20 KHz	1 KHz
Clock Frequency	1.024 MHz	2.56 MHz	320 KHz
Power Consumption	6.75 µW @ 2.5 V	420 µW @ 1.8 V	120 µW @ 2 V
FOM	1.78 pJ/step	6.98 pJ/step	14.6 pJ/step

Table 5.3 Comparison to Other Works

Chapter 6 Passive KD1S Modulators

Introduction to KD1S Modulators

Passive sigma delta principles can be applied to unconventional data converter topologies. One unique type of sigma-delta data converter is the *K-delta 1-sigma* or KD1S ADC. This topology was proposed in 2008. It was a new topology to the mature field of sigma-delta ADCs (24). The main contribution of this design is a significant increase in effective sampling rate while utilizing practical, realizable clock signals. Currently all physically implemented designs in the literature use active integrators. Due to the high unity gain bandwidth requirements of an active integrator in this topology, it is desirable to replace it with a passive integrator. In this case, the purpose of the passive integrator is to enable high-speed operation and ease of design rather than the reduction of power consumption which is the usual reason for adopting a passive sigma delta modulator.

The KD1S ADC is an attempt to achieve the same goal as that of double-sampled and time-interleaved sigma-delta ADCs –a higher effective sampling rate than the clock frequency. A double-sampled ADC samples the signal twice, on both the rising and falling edges of the clock. This allows for an effective sampling frequency that is twice that of the clock [25]. The time-interleaved sigma-delta ADC promises a *K* times increase in sampling rate for a *K-path* modulator. This design utilizes *K* individual sigma delta modulators and clocks them in a time interleaved fashion. For example, an 8-path sigma delta modulator results in an effective sampling rate that is eight times higher than the clock. However, this

design has a flaw; it does not exhibit noise-shaping that corresponds to the increase in effective sampling rate. Rather, it simply spreads the quantization noise power over a wider frequency range. This results in a 3dB increase in SNR for every doubling of *K* which is the same as simple averaging. This is detailed in [26].

The KD1S modulator exhibits proper noise-shaping extending to *K* times the clock frequency. This sets the design apart from time-interleaved and double sampled designs. A simple general 1st-order passive KD1S modulator is shown in Fig. 6.1. In this design, *K* quantizing elements are needed which have their inputs connected in parallel and share the same common-mode voltage, V_{cm}. There is only one integrating element which in this case is the capacitor, *C.* This is the "one-sigma" portion of the topology. The "*K-delta"* portion of the topology is reflected by the RK valued resistors in the circuit. The reason that their values are RK instead of just R is in order to keep the overall gain of the modulator at unity. The parallel combination of K resistors with value of RK is equal to R, which is also the value of the input resistor ensuring that input and feedback currents are equal resulting in unity gain.

In the diagram of Fig. 6.1, there are *K* clocks, one for each comparator which are labeled from Φ_1 to Φ_K. The clocks and their phasing are of paramount importance to this topology. When implemented properly, this allows for analyzing the KD1S modulator as a single comparator that is clocked at a frequency of $K * F_{clk}$. The clocks Φ_1 to Φ_K all have the same frequency but they are phase shifted such that each rising edge is equidistant and sequential. This concept is illustrated in Fig. 6.2 for 8 clock phases. All the clocks are at the same frequency of 10 MHz in this diagram however each clock is phase shifted by 45

degrees from the one before it. This results in eight rising edges within one clock period, T_s. Since the comparators respond to a rising clock edge, this has the effect of sampling the input signal eight times within a clock period.

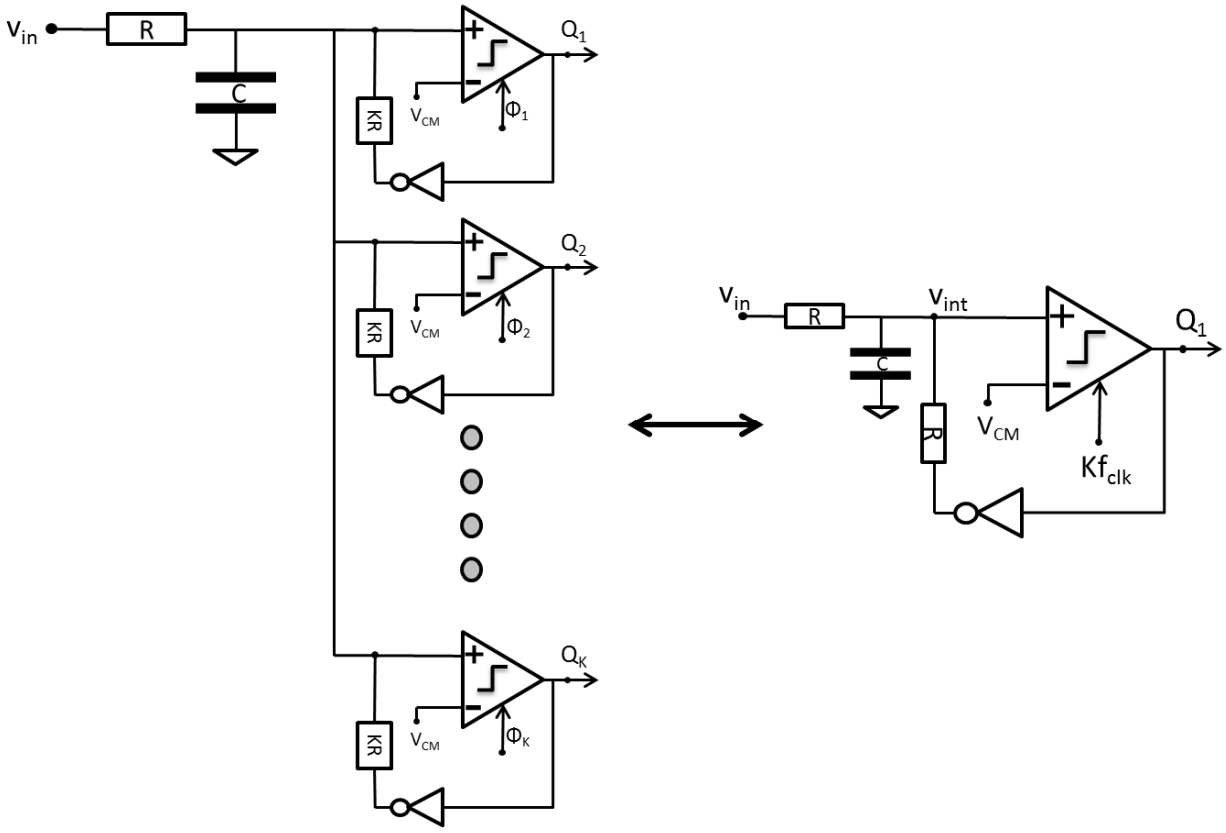


Figure 6.1 – General structure of KD1S ∑-Δ modulator and equivalent circuit.

The leading edge of each clock is demarcated by a dashed line in Fig. 6.2. There are eight edges within the clock period interval of 100 ns denoted by T_s. As a result of this, an effective clock period can be defined as $T_s/8$. This is equivalent to the distance between sequential clock edges as shown in Fig. 6.2. It is also important to note that each clock signal pair that is 180 degrees apart are complementary. For example, Φ_5 is an inverted

version of Φ_1. This is convenient because for any KD1S modulator with K clocks, only half the clocks actually need to be generated; the remaining clocks can be derived with inverters.

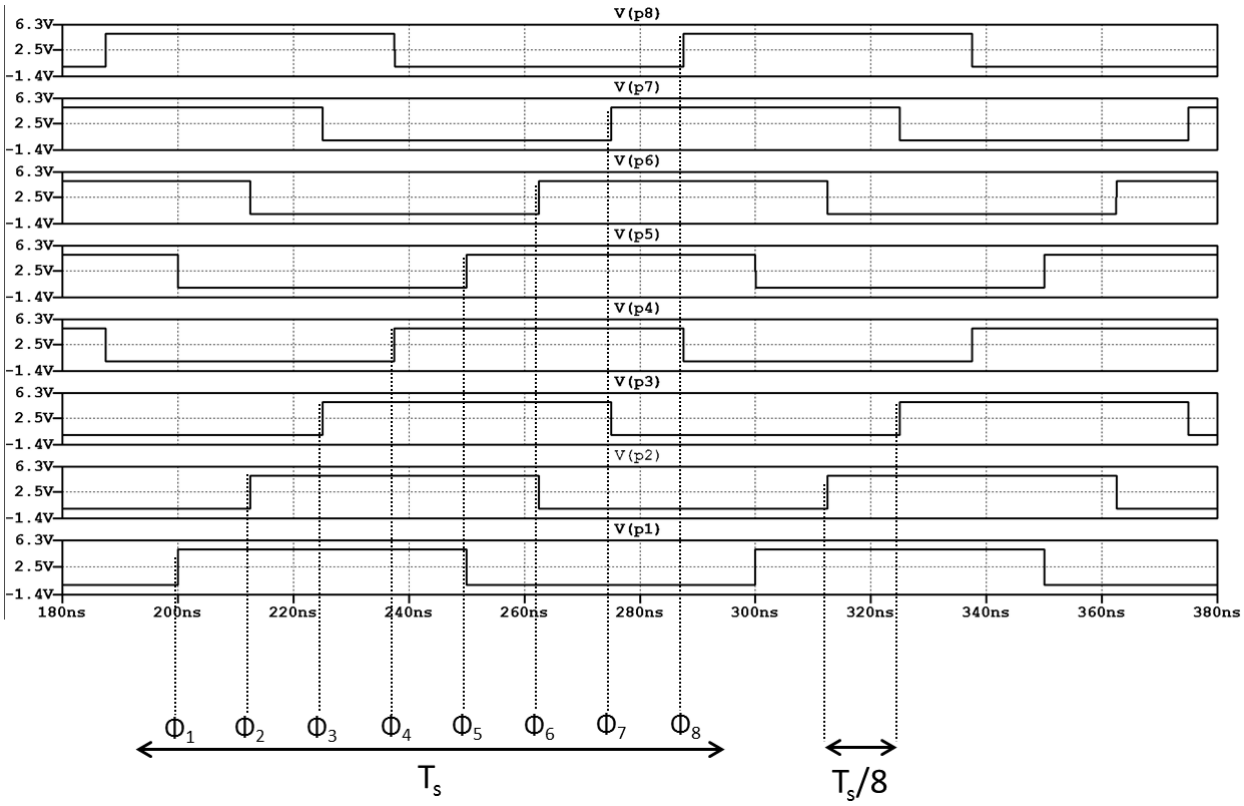


Figure 6.2 – Example of clock phasing for an 8-path KD1S.

At first glance, it would appear to be difficult to derive the quantization noise transfer function of a KD1S modulator, but it is actually identical to a conventional sigma-delta modulator with the quantization noise power extended over an interval, Kf_s. This is illustrated in Fig. 6.3. This has been both theoretically and practically proven with a

physical IC implementation in [15]. The middle point of the diagram $Kf_s/2$ represents the oversampled nyquist rate and consequently the maximum possible bandwidth for this data converter. Beyond this point, there would be aliasing of the input signal. It is important to note that K in this case does not represent the oversampling ratio as in previous chapters. Rather K is the number of feedback paths, quantizing elements and clock phases. Figure 6.3 is simply an illustration how the quantization noise is distributed over an interval of Kf_s

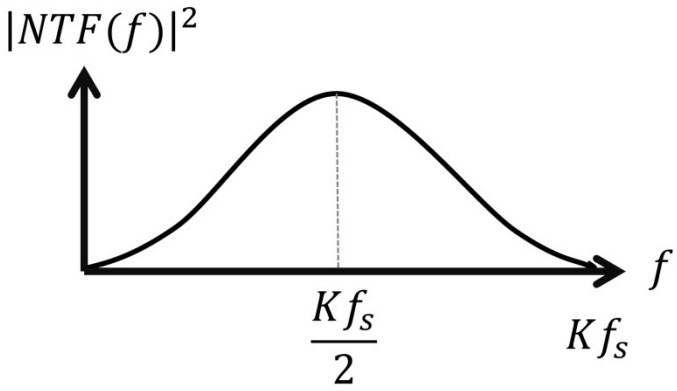


Figure 6.3 – Theoretical noise transfer function of KD1S modulator.

For actual analysis with a given signal bandwidth, the OSR needs to be taken into account. This can be done with the same methods as outlined in chapter 1 but with substituting the new effective clock frequency,

$$f_{s,new} = K_{path*} f_s \tag{6.1}$$

Circuit Design

The block diagram of the KD1S modulator implemented in the C5 process is shown in Fig. 6.4. There are four main components in this diagram, the KD1S modulator entitled "k_path_mod"; the output logic; the buffer array; and the voltage controlled oscillator (VCO).

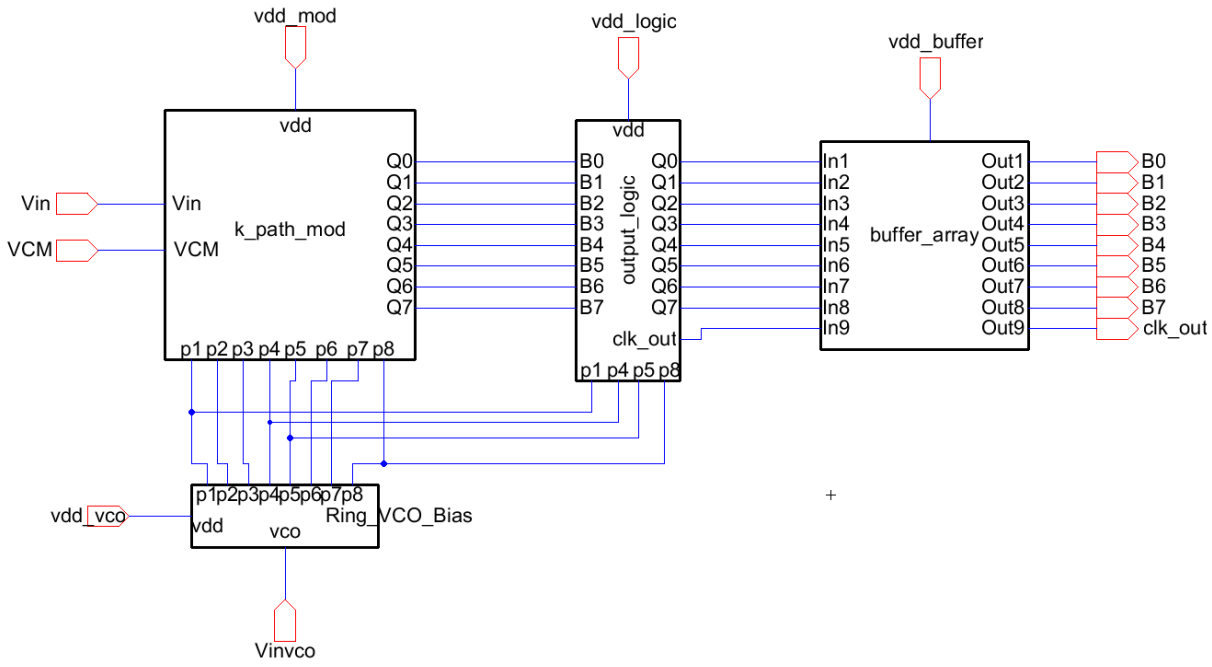


Figure 6.4 – Block diagram of KD1S modulator.

The additional components are required for the K1DS modulator to operate correctly. The output logic is used to reclock and synchronize the data for further processing. The buffer array is used to drive off-chip loads and reduce loading on the output logic block. The VCO is needed to create the proper 8 clock phases.

The VCO is composed of two main blocks, a biasing circuit and a ring oscillator. This is shown in the diagram of Fig. 6.5. The ground and VDD connections are implied and omitted for clarity. A voltage applied to the input pin “Vinvco” controls the clock frequency. The outputs p1-p8 are eight phase shifted clocks which are like those displayed in Fig. 6.2.

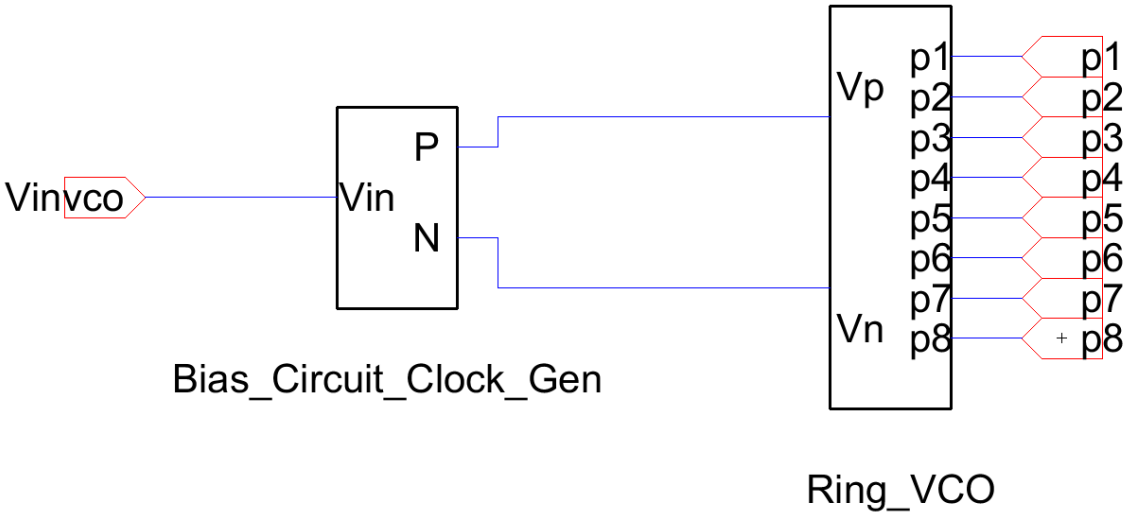


Figure 6.5 – Block diagram of VCO.

The bias circuit is shown in Fig. 6.6 and is a simple beta-multiplier voltage reference. The operation of this circuit is detailed in [27]. This circuit derives two reference voltages, “VbiasN” and “VbiasP” from the input voltage. These references are used to set the current that flows in the inverter starved ring oscillator.

The schematic of the ring oscillator is shown in Fig. 6.7. This ring oscillates uses four complementary delay elements with output of the last stage connected to the input of the first stage which ensures instability and oscillation. The detailed procedure for designing ring oscillators of this type is detailed in [28]. The schematic of an individual delay unit is displayed in Fig. 6.8. This circuit is a non-overlapping clock generator similar to that used

in Fig. 5.3. In this application it is not used as an NL clock generator, but as a delay unit with complementary outputs.

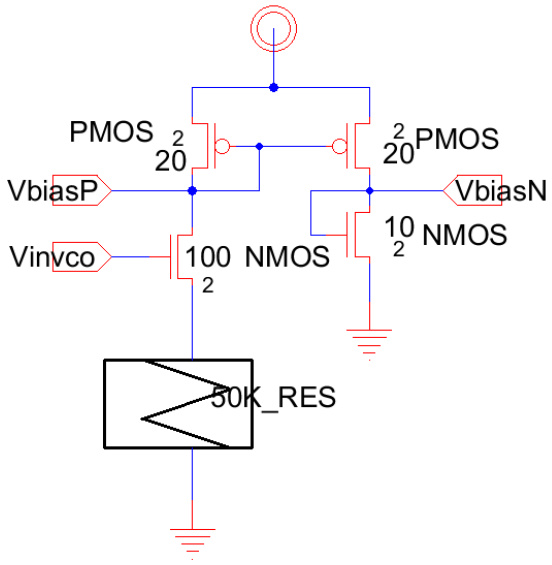


Figure 6.6 – Bias circuit.

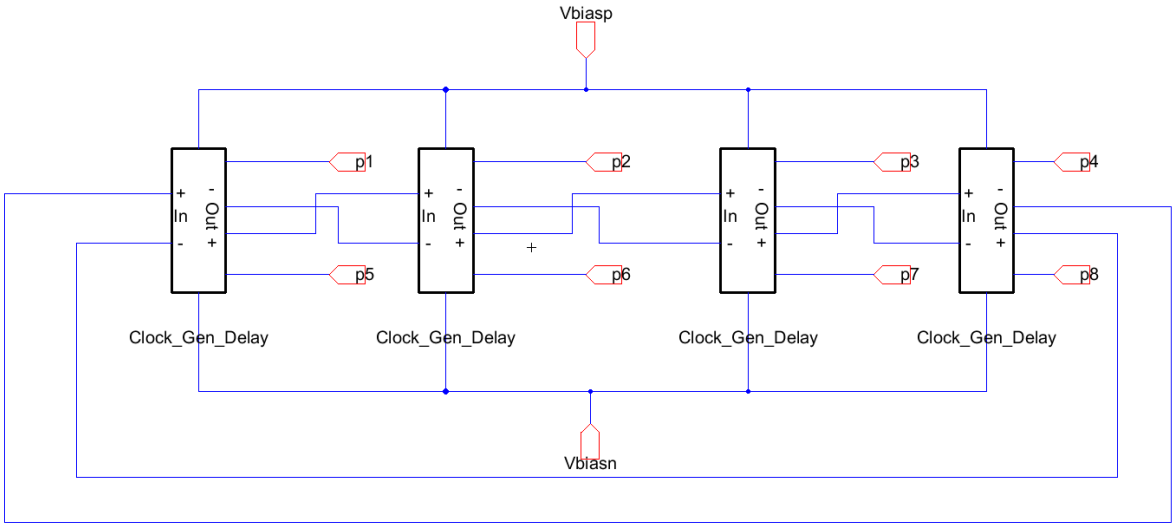


Figure 6.7 – Ring oscillator comprised of differential delay units.

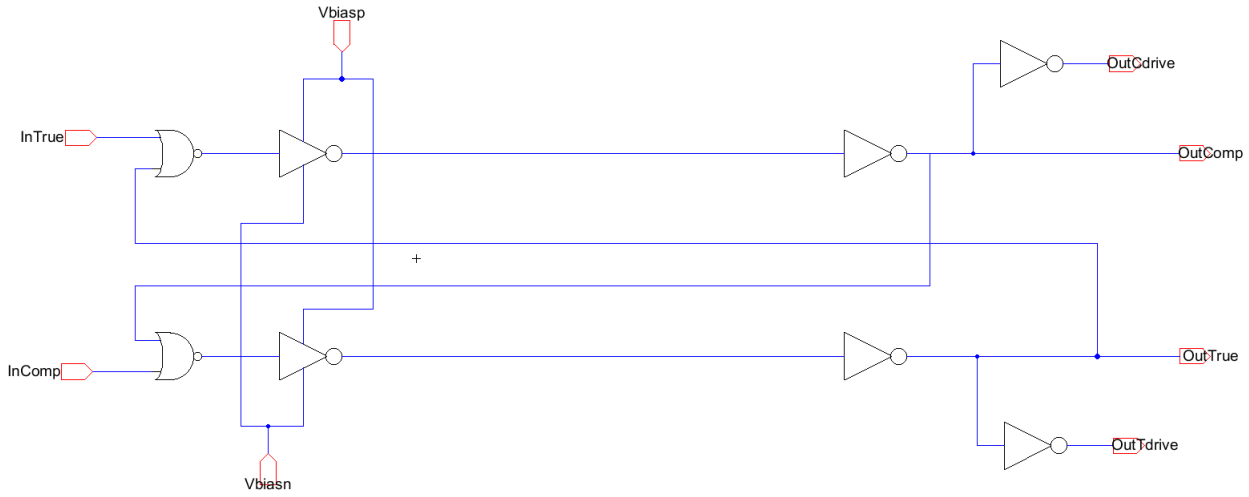


Figure 6.8 – Schematic of individual delay unit.

The delay in this element can be controlled by the voltage applied to the “Vbiasp” and “Vbiasn” inputs. These voltages control the transconductance of a current-starved inverter. Varying the transconductance of an inverter affects its switching speed and its delay. The schematic of the current-starved inverter is shown in Fig. 6.9. The top PMOS and bottom NMOS restrict the current that can be sourced or sunk by the inverter that is between them. This reduces the speed at which the output can change states. Due to the plethora of sub-circuits in this chapter, schematics of the remaining logic blocks and inverters are detailed in A.6.

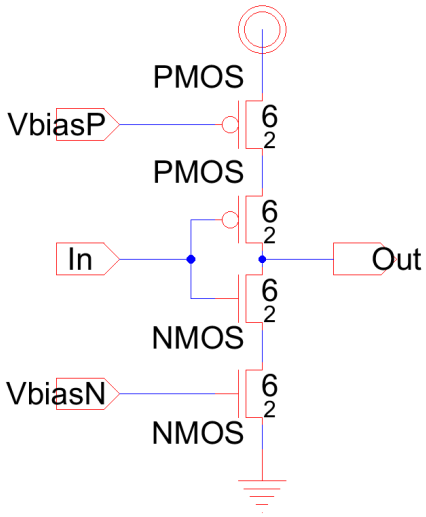


Figure 6.9 – Schematic of current-starved inverter.

The output from the K1DS modulator is sporadic and needs to be timed properly for processing by either internal or external DSP. This is achieved with the use of an 8-bit register as shown in Fig. 6.10. Each bit of the register is comprised of two D-FFs in series. For bits B0-B3, the D-FFs are clocked on the P1 and P4 clock phases. The D-FFs are clocked on the P5 and P8 phases for bits B4-B7. The output clock is derived from inverting B7. The final output from the register is 8 data bits and 1 clock bit. These outputs can then be sent to DSP processors for digital filtering. The output buffer shown in Fig 6.11 is simply 8 large inverter arrays which can drive off-chip loads. Layouts and detailed schematics of the D-FFs as well as the output buffer are found in A.6.

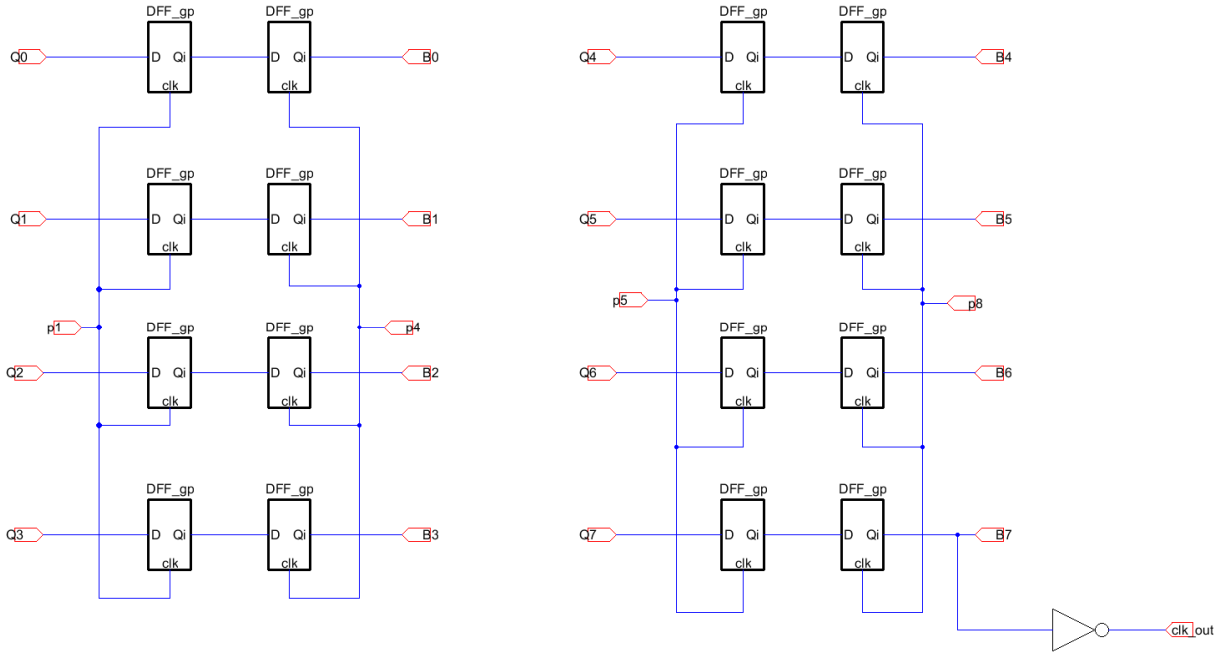


Figure 6.10 – Schematic of 8-bit register.

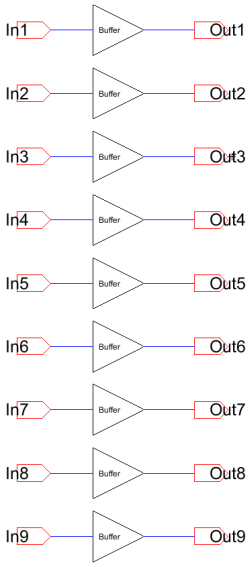


Figure 6.11 – Output buffer.

The heart of this circuit is the passive 2nd order KD1S modulator itself. The schematic of this is shown in Fig. 6.12. The same type of passive noise-shaping network as shown in Fig. 4.1 and detailed in chapter 4 is utilized. The filtering capacitors are 2 pF and are at the same location in the circuit as shown in Fig. 4.1. R1 is 10k and R2 is 100k. R2 is made from two 50k resistors in series for ease of layout reasons. This is also the reason why C1 and C2 are made from two 1 pF capacitors in parallel. The feedback resistors are 80k which is eight times the value of the input resistor R1. This is done to ensure that the gain of the modulator remains at unity since the parallel combination of these feedback resistors is equal to R1.

There are eight comparators in this modulator and their positive inputs are all connected to the same point at the node of the 2nd RC filter. The common mode signal, VCM is applied to their negative inputs. Each comparator is clocked by its respective clock phase generated by the circuit in Fig. 6.5. The complementary output from each comparator is used to apply the negative feedback "delta" signal to the integration capacitor. Finally, the raw modulator output is made up from the positive comparator outputs and is 8-bits wide. This data is then sent to the register in Fig. 6.10 for reclocking and synchronization.

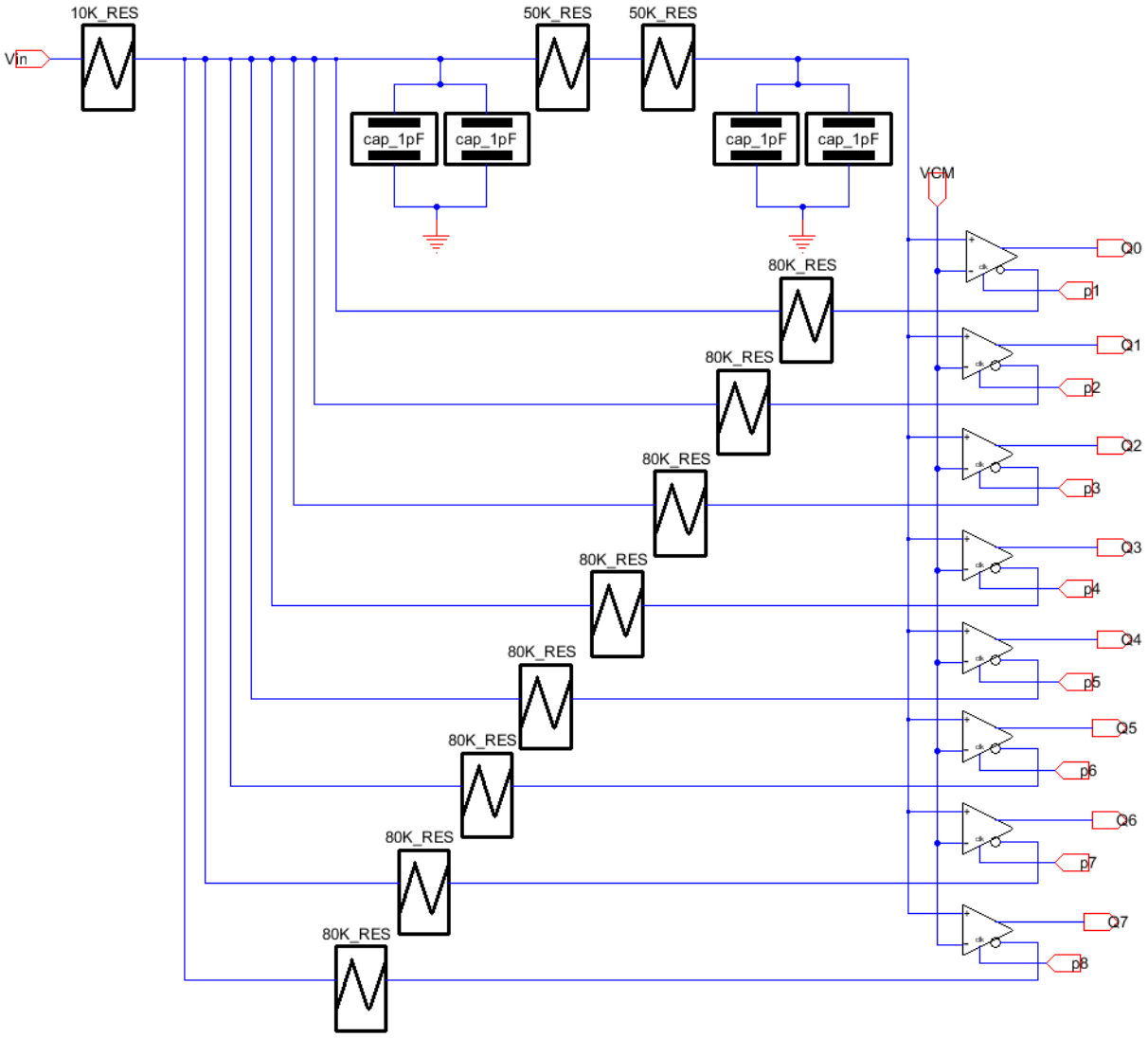


Figure 6.12 – Passive KD1S modulator.

The design of the comparator is a modified version of the one in Fig. 4.6. A low power pre-amp stage was added to the design in Fig. 4.6. This was done to increase the resolution of the comparator in Fig. 6.13. It was discovered through simulations that the resolution of the sigma-delta ADCs in previous chapters was limited by the ability of the comparator's ability to resolve small input signal differences. The addition of a simple pre-amp increases the resolution by about 20, which is also the gain of the pre-amp. The

penalty is an additional 1 uA of bias current for the pre-amp. While this deviates from the goal of low-power, in this design exploration it is justified since the K1DS modulator may be used in high speed passive topologies which dispense with an active integrator but still need to maximize resolution. Additional layouts of this circuit are found in A.6.

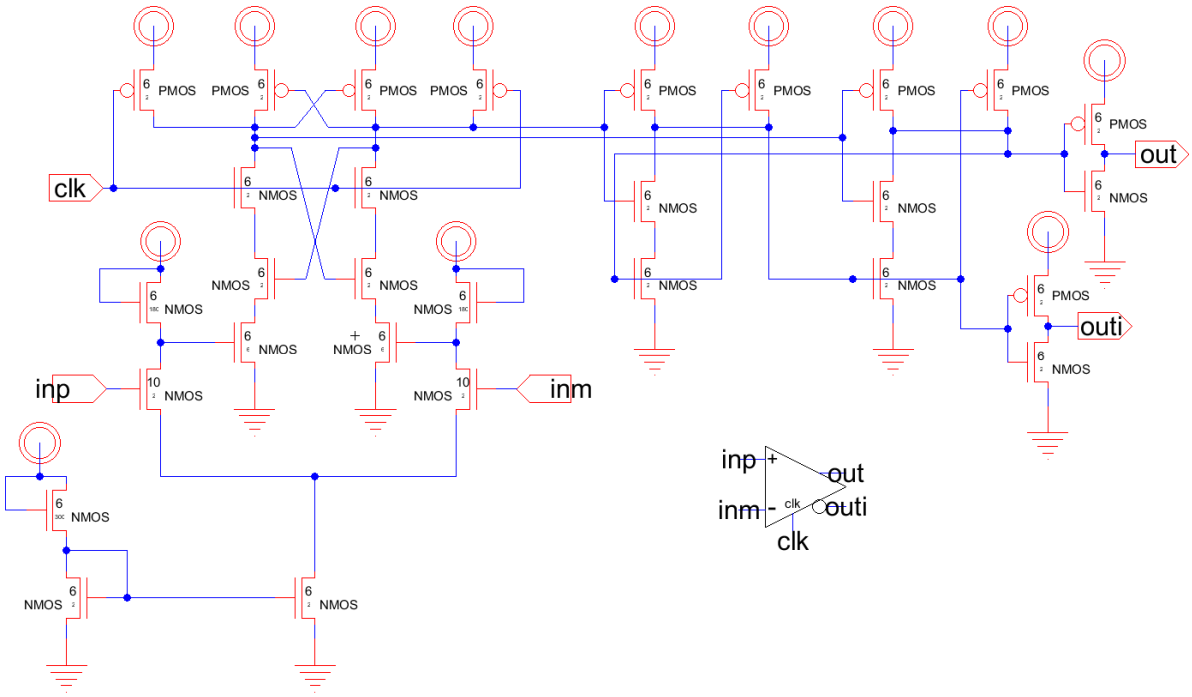


Figure 6.13 – Schematic of comparator with pre-amplifier.

Measurements

The modulator's input range; power consumption and SNDR were measured and quantified. The 8 outputs of the modulator were summed together using 8 1 k resistors and then connecting this junction to a 2nd order low-pass filter made up of two 12.6 k resistors and two 70 pF capacitors resulting in a corner frequency of 180 KHz. The clock frequency was set to 4.473 MHz and verified with a frequency counter as shown in Fig.6.14. This results in an effective sampling frequency of 35.784 MHz. Since output buffers are used in this circuit, the rise-time was verified to ensure that they have the expected load driving ability. The output of one of the buffers while driving a 10k load in parallel with 1.2 pF is shown in Fig. 6.15. The rise time of the waveform is 3 ns which corresponds to a bandwidth of 116 MHz. The spike is due to the sharp transitions and capacitive feedthrough effects within the chip. The supply current to the chip was measured using a multimeter and was 10 mA under these test conditions.

Figure 6.14 – Verifying internal VCO frequency.

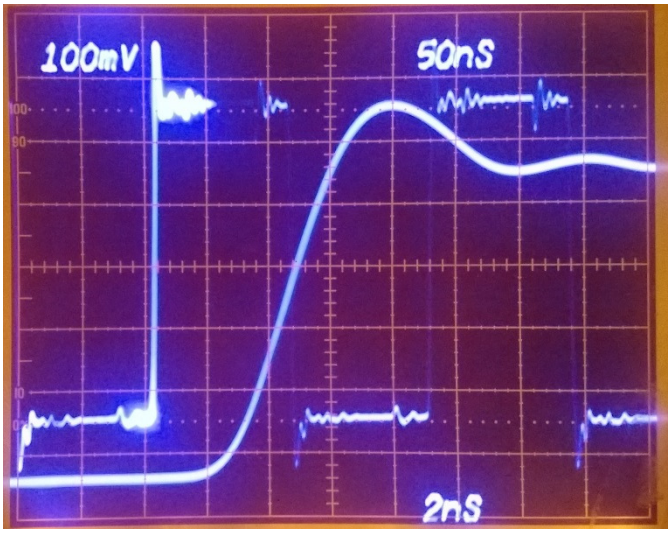


Figure 6.15 – Verifying output buffer driving ability.

The SNDR was calculated from the FFT of a 20 MHz 14-bit PC based oscilloscope. The same procedures as outlined in chapters 3 and 4 were used to harvest data. A sine wave with an offset of 2.5 V and amplitude of 0.75 V was applied to the input of the KD1S modulator. This input signal and the filtered modulator output is shown in Fig. 6.16. The SNDR values were converted to ENOB and are displayed in Fig. 6.16. The ENOB remains above 7.5 bits for frequencies of 10 kHz to 110 kHz. There are multiple peaks in the ENOB data which each have a different explanation for their peak. The first peak with 9 bits of ENOB is at 10 KHz. This rise in resolution is due to high OSR at low frequencies. ENOBs of around 9 bits were observed at low frequencies, but were omitted since the switched capacitor modulator of chapter 5 would be better for this frequency range. The second peak at 30 kHz represents the area of highest resolution for this modulator. The final rise in ENOB after 80 kHz is due to the fixed output filter with a corner frequency of 180 kHz used during testing. This filter artificially inflates ENOB for high frequencies since it attenuates the harmonics.

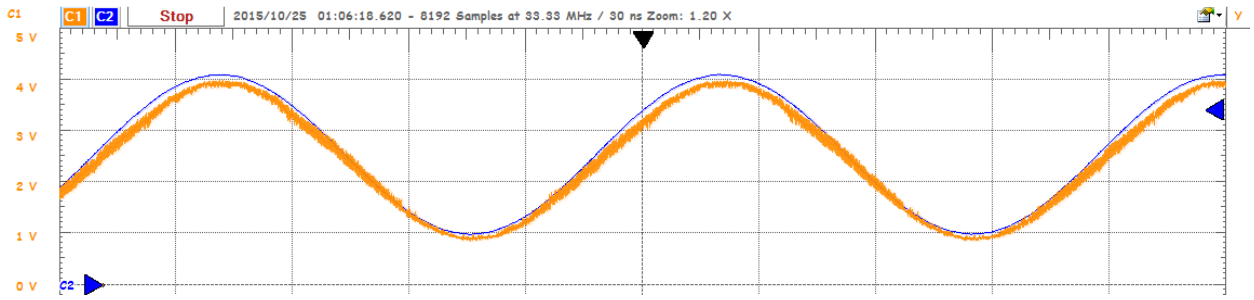


Figure 6.16 – Input signal (blue) and filtered output (yellow).

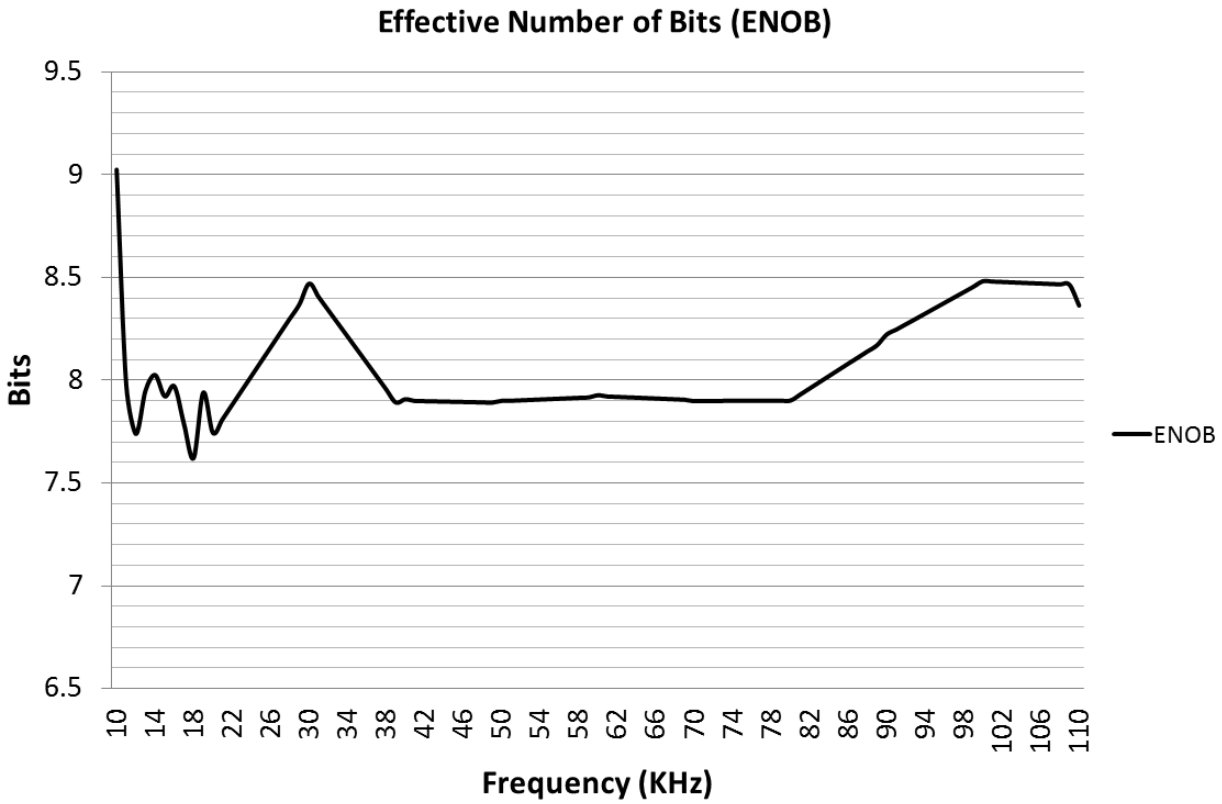


Figure 6.17 – ENOB as function of input frequency.

Next the input signal range was verified using a 0-5 V input triangle wave. The input range span should be almost all of 0 V to 5 V since feedback will cause the comparator to switch for any voltage difference greater than its minimum resolvable voltage. However, the speed at which it switches decreases and consequently the modulator can be not characterized as having a full rail-to-rail input for the expected input frequencies. Applying a 0-5V 1 kHz ramp signal to the input results in an input range from 0.4 V to 4.5 V as displayed in Fig. 6.17.

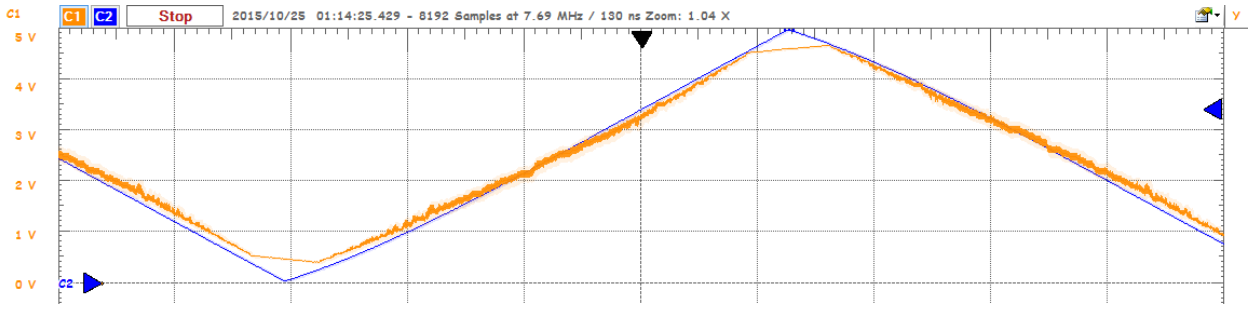


Figure 6.18 – Input ramp signal (blue) and output (yellow).

There are many “dead-zones” present which likely explain the low resolution of the modulator. These dead-zones are visible in Fig. 6.17 as areas where the output stops following the input. There is a prominent dead-zone in the middle of the input range at 2.5 V. Finally it is worth noting that the noise shaping in this example does not follow Fig. 6.3. The noise shaping should extend to 35 MHz in this example (beyond the bandwidth of this oscilloscope) but it instead extends to only 4.4 MHz. The reason for this is because combining the outputs with resistors results in comb filtering with peaks at integer

multiples of the clock frequency. This comb filtering is also exhibited in the FPGA based KD1S modulator in [32].

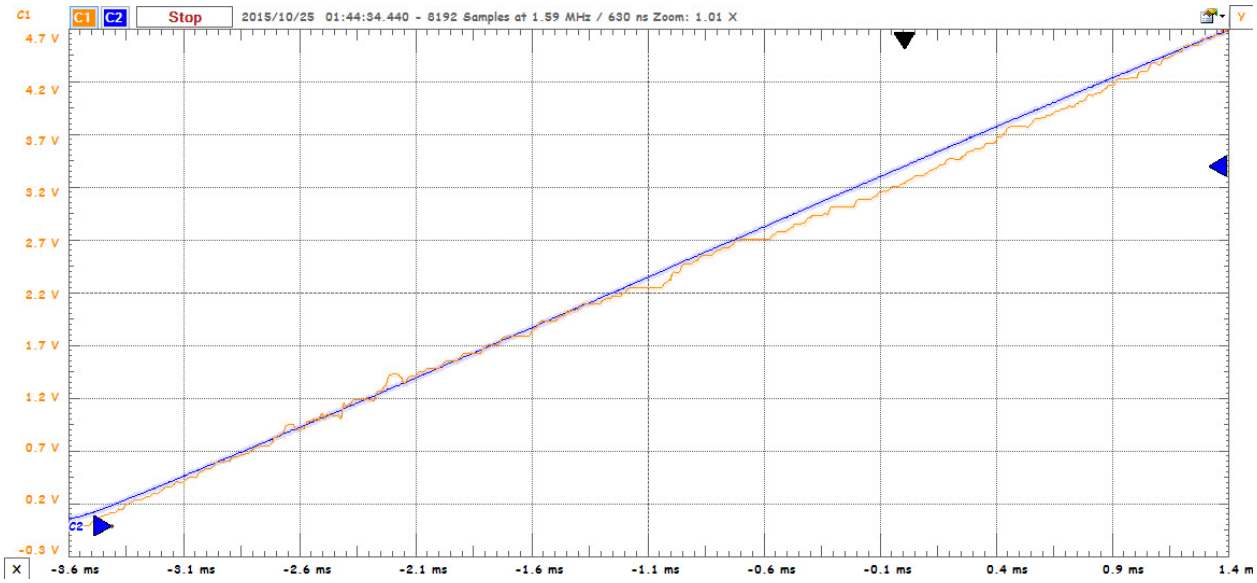


Figure 6.19 – Input ramp signal (blue) and output (yellow) showing dead-zones.

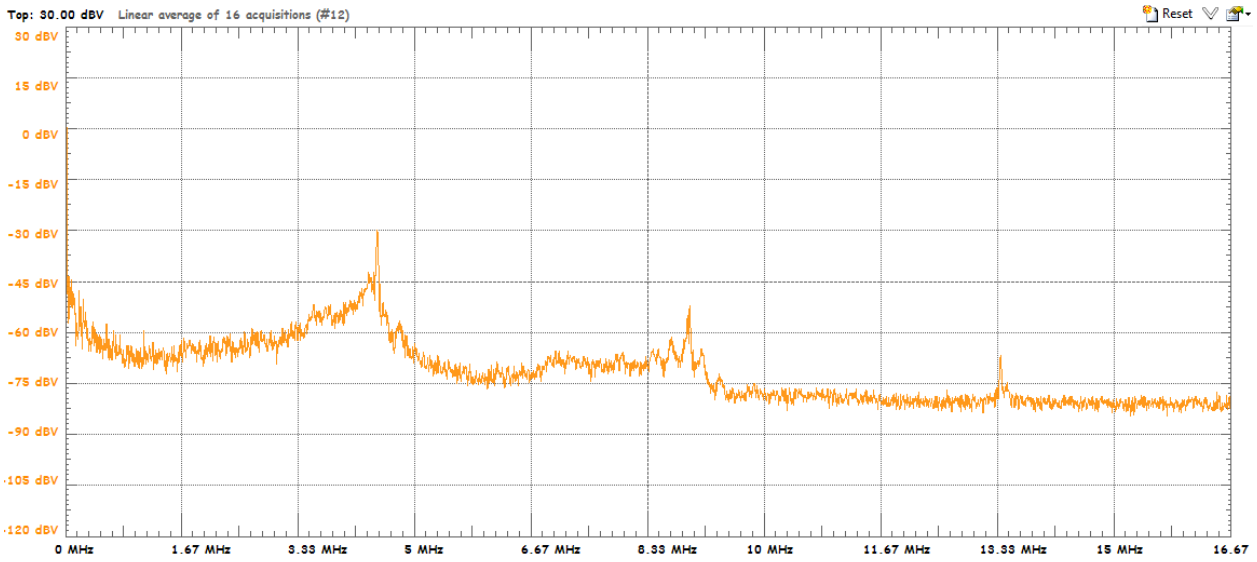


Figure 6.20 – Noise shaping with comb filtering.

Performance Parameter	Value	Test Conditions / Comments
Supply Voltage	2.4 V – 5.5 V	
Supply Current	10 mA	@5 V
Power Consumption	50 mW	@5 V
Input Voltage Range	0.3 V – 4.5 V	Tested with 1 kHz 0-5 V Ramp
Tested Frequency Range	10 kHz – 110 kHz	0.75 V peak with 1.25 V DC Offset
Clock Frequency	4.47 MHz base 35.76 MHz effective	Effective clock is base clock multiplied by 8
Nyquist Rate Bandwidth	180 kHz	2nd order passive filter
Oversampling Ratio	198 as tested	128 or 256 for practical digital filter
SNDR	51 dB @ 30 kHz	0.75V peak with 2.5 V DC Offset
ENOB	8.5 @ 400 Hz	0.75V peak with 2.5 V DC Offset
FOM	1.2 pJ/step @ 35.78 MHz Effective Clock 9.6 pJ/step @ 4.47 MHz Base Clock	Not clear yet whether base or effective clock is appropriate for FOM calculation using Eq. 5.2.

Table 6.1 Summary of Measured Parameters

Conclusion

As semiconductor technologies continue to advance, it is important to revisit topics that were written off in the past as they may offer solutions to new challenges that arise. Passive sigma-delta ADCs are one such topic. This category of data converters has been used to teach basic sigma delta concepts but they are rarely used in implemented designs. The main reason for this is due to limited resolution due to distortion arising from voltage swing at the integrator input. The proposed 2nd order topology introduced here offers an improvement over traditional passive sigma-delta modulator topologies. This has been verified through the use of transfer functions, simulations and measurements.

The most prominent benefit of the proposed topology is the reduction in power consumption. The switched-capacitor modulator presented here exhibits very low power consumption in both absolute and relative terms when taking its 500 nm process technology into account. The proposed topology is especially attractive for portable medical applications which tend to use older processes due to increased reliability. These applications can reduce power consumption through design changes instead of process scaling.

Although all the IC implementations of the proposed 2nd order modulator have been implemented in a mature 500 nm CMOS process, this topology is well suited for scaling to newer processes with feature sizes of 45 nm and smaller. The problem with these processes is that the limited performance of analog components makes it difficult to create

active integrators with the necessary performance. Using passive integrators allows for implementing high speed sigma-delta modulators in these processes albeit with a sacrifice in resolution. Another application for the proposed topology is for implementing data converters in systems made up of purely digital components such as FPGAs and microcontrollers. The addition of a few passive components to these digital systems to create sigma-delta ADCs can mitigate the need for external ADC chips. As designers take these aspects into account, it is highly likely that there will be a significant increase in the proliferation of passive sigma-delta ADCs in the future.

References

[1] W.R. Bennett, "Spectra of Quantized Signals," *Bell System Technical Journal,* Vol. 27, pp. 446-472, July 1948.

[2] Engineering Staff Analog Devices Inc., *Sigma-Delta ADCs and DACs,* 1992, pp 1-3.

[3] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 168-172. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[4] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 173-178. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[5] Engineering Staff Analog Devices Inc., *Data Conversion Handbook (Analog Devices),* Newnes, 2005. ISBN 978-0750678414 pp. 3.120-3.122.

[6] Engineering Staff Analog Devices Inc., *Data Conversion Handbook (Analog Devices),* Newnes, 2005. ISBN 978-0750678414 pp. 3.116-3.118.

[7] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 199-209. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[8] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 216-217. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[9] Roy, A., Baker, R. J., "A Passive 2nd-order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion," *Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on* , vol., no., pp.595,598, 3-6 Aug. 2014.

[10] Engineering Staff Linear Technology Corp., *LT1672/LT1673/LT1674,* 2001.

[11] M. Dabacan, "Analog Discovery Technical Reference Manual," *Digilent Inc.*, Oct-2013.

[12] "C5: 0.5 µm Process Technology," *On Semiconductor*. [Online]. Available at: http://www.onsemi.com/powersolutions/content.do?id=16693. [Accessed: 2015].

[13] S. Rubin, "Electric User's Manual, version 9.06," *Static Free Software*, 2015. [Online]. Available at: http://www.staticfreesoft.com/documentsuser.html.

[14] Baker, R. J, *CMOS Circuit Design, Layout, and Simulation, Third Edition,* John Wiley and Sons, Inc. , 2010. pp. 452-455.

[15] Saxena, Vishal, "K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion", Ph.D. dissertation, ECE, Boise State University, Boise, ID, 2010.

[16] Engineering Staff Linear Technology Corp., *LTC1799,* 2001.

[17] J. Williams, "High Speed Amplifier Techniques," *Linear Technology*, Jan-1991. [Online]. Available at: http://cds.linear.com/docs/en/application-note/an47fa.pdf. [Accessed: 2015].

[18] "Agilent 34405A 5 ½ Digit Multimeter," *Keysight Technologies*, 2006. [Online]. Available at: http://cp.literature.agilent.com/litweb/pdf/34405-91000.pdf. [Accessed: 2015].

[19] T. C. Carusone and D. Johns, “Switched Capacitor Circuits,” in *Analog integrated circuit design*, 2nd ed., Hoboken, NJ: John Wiley & Sons, 2012, pp. 557–565.

[20] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 316-317. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[21] R. Elliot, “Capacitor Characteristics,” *Elliot Sound Products*, 2005. [Online]. Available at: http://sound.westhost.com/articles/capacitors.htm#s24. [Accessed: 2015].

[22] W. Kester, “Understand SINAD, ENOB, SNR, THD, THD N, and SFDR so You Don't Get Lost in the Noise Floor ,” *Analog Devices Inc.*, 2009. [Online]. Available at: http://www.analog.com/media/en/training-seminars/tutorials/mt-003.pdf. [Accessed: 2015].

[23] B. Jonsson, “Using Figures-of-Merit to Evaluate Measured A/D-Converter Performance,” *International Workshop on ADC Modeling, Testing and Data Converter Analysis and Design*, 2011.

[24] Saxena, V., Li, K., Zheng, G., and Baker, R.J., “A_K_Delta_1_Sigma_Modulator_for_Wideband_Analog_to_Digital_Conversion,” *P roceedings of the IEEE 52nd International Midwest Symposium on Circuits and Systems*, pp. 411-415, August 2-5, 2009.

[25] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 59-60. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[26] Baker, R. Jacob, *CMOS Mixed-Signal Circuit Design, Second Edition*, John Wiley and Sons, Inc., 2009. pp 312-313. Wiley-IEEE Press, ISBN 978-0-470-29026-2

[27] Baker, R. J, *CMOS Circuit Design, Layout, and Simulation, Third Edition,* John Wiley and Sons, Inc. , 2010. pp. 624-625.

[28] Baker, R. J, *CMOS Circuit Design, Layout, and Simulation, Third Edition,* John Wiley and Sons, Inc. , 2010. pp. 401-402, 1082-1085.

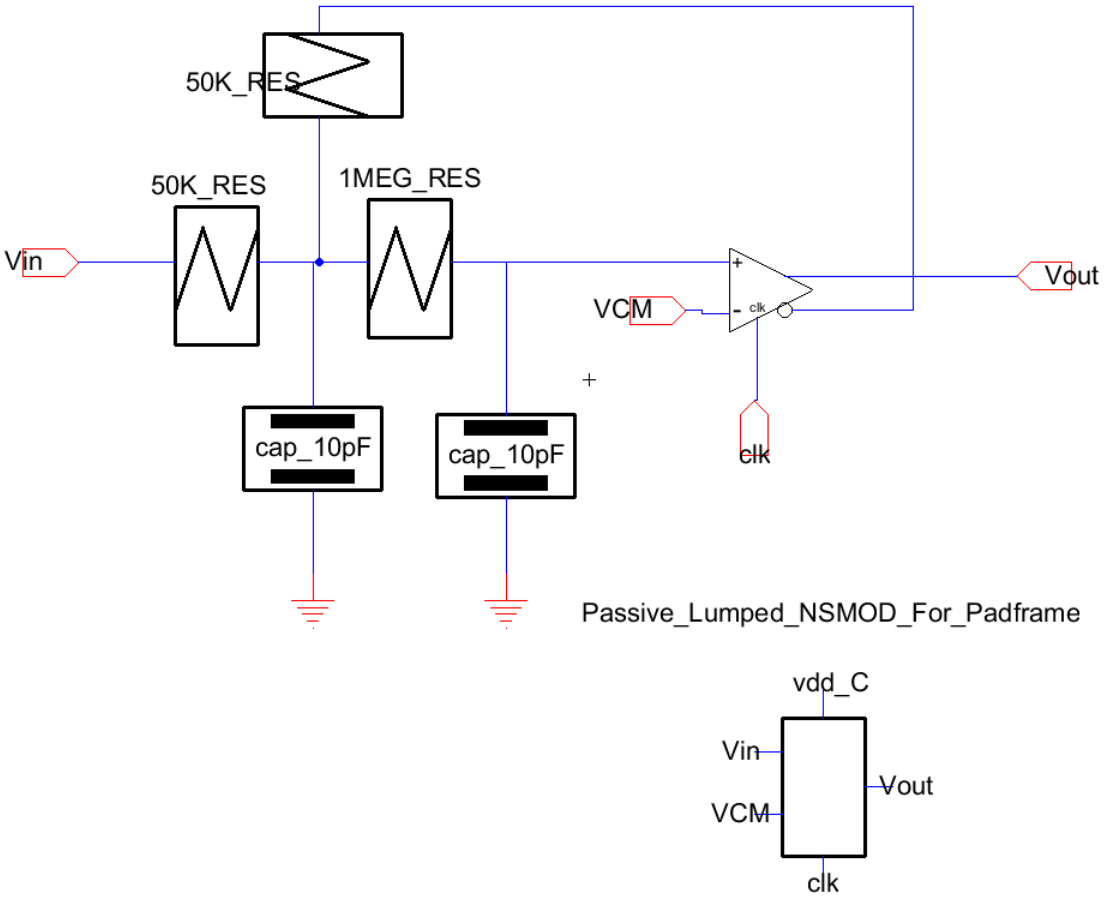
[29] Huang, M. C., Liu, S. I.,"A Fully Differential Comparator-Based Switched Capacitor Modulator," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.56, no.5, pp.369,373, May 2009

[30] Gundel, Adnan, and Carr, William N. "A Micro Power SigmaDelta A/D Converter in 0.35μm CMOS for Low Frequency Applications," LISAT 2007. (2007): 1-7.

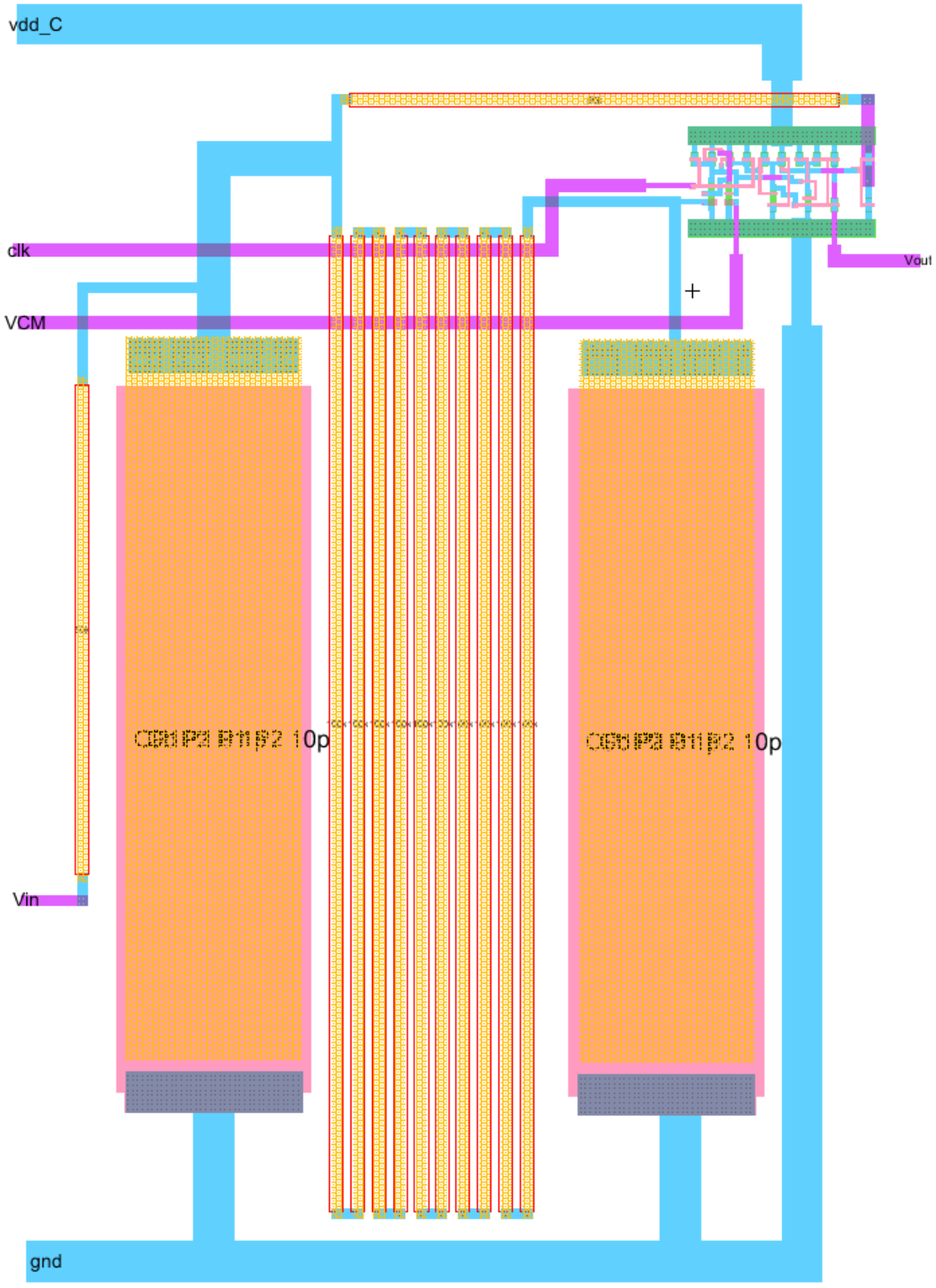
[31] Roy, A. and Baker, R. J., "A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.

[32] Roy, A., Meza, M., Yurgelon, J., and Baker, R. J., "An FPGA Based Passive K-Delta-1-Sigma Modulator," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 121-124, August 2-5, 2015.

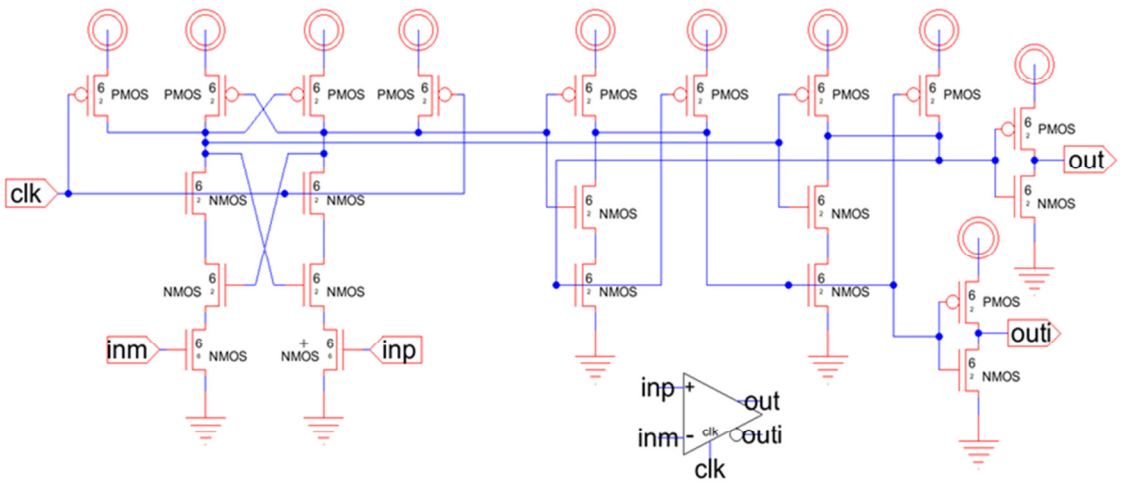
Appendix A.4 Schematics and Layouts for in Chapter 4



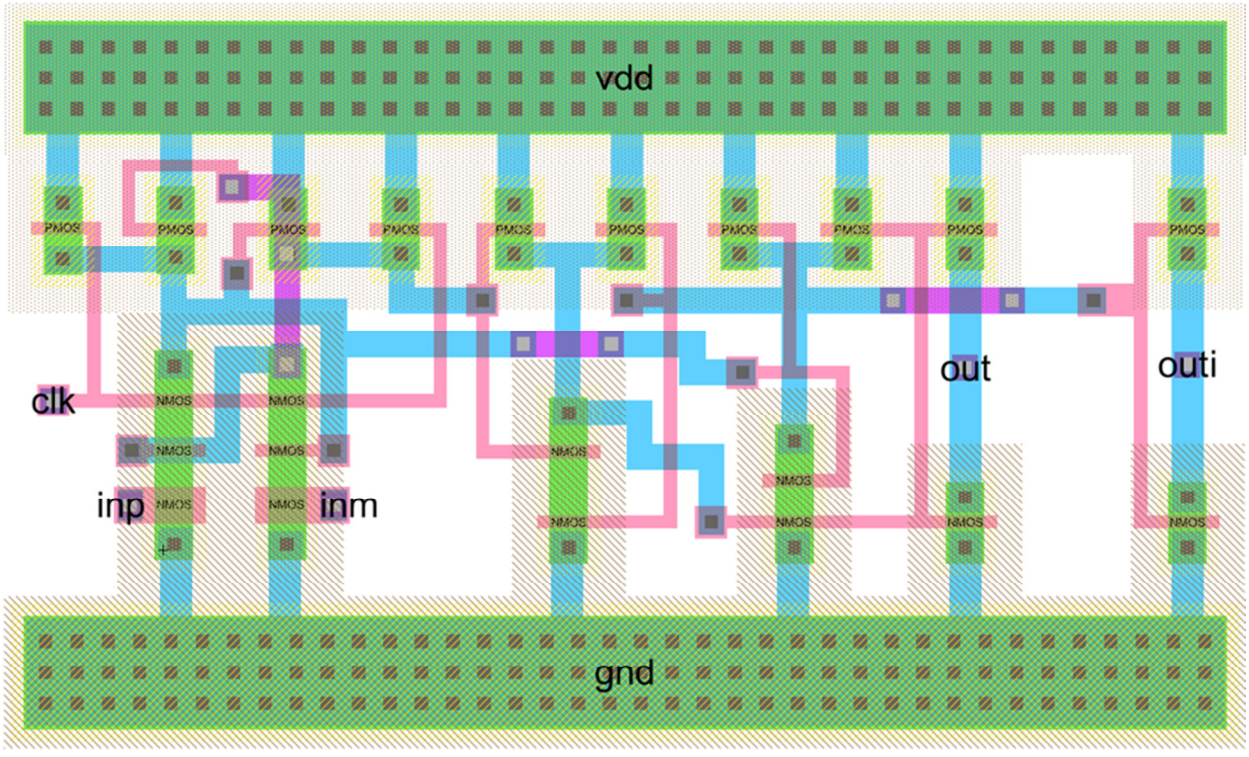
A.4.1 – Schematic of passive sigma-delta modulator.



A.4.2 – Layout of passive sigma-delta modulator.

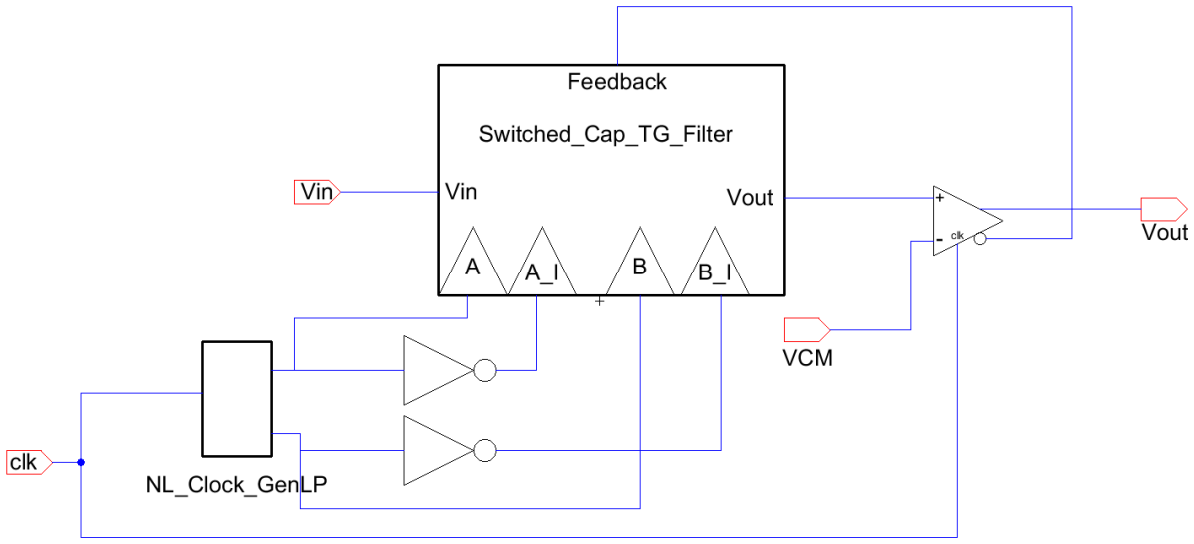


A.4.3 – Schematic of comparator.

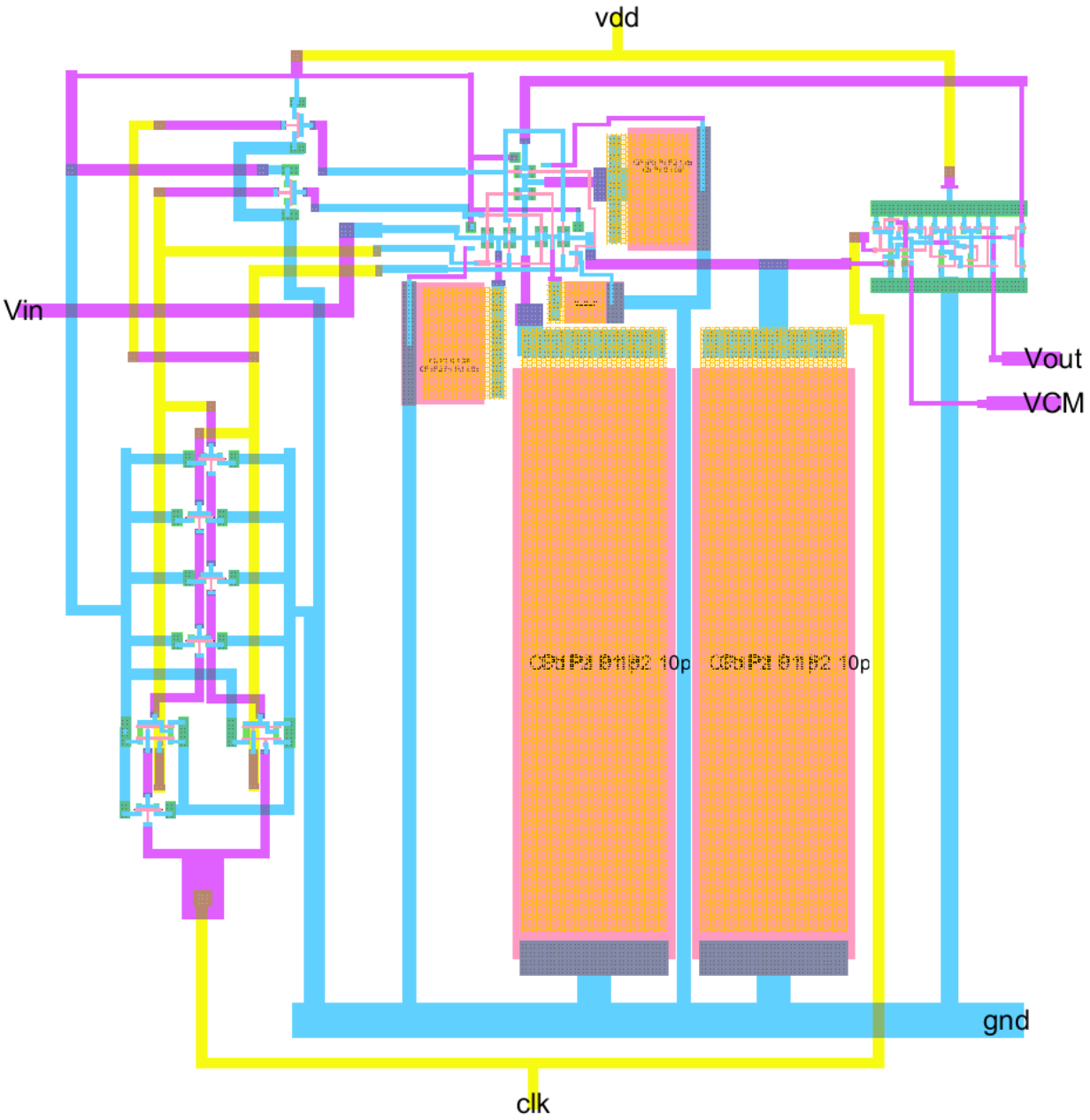


A.4.4 – Layout of comparator.

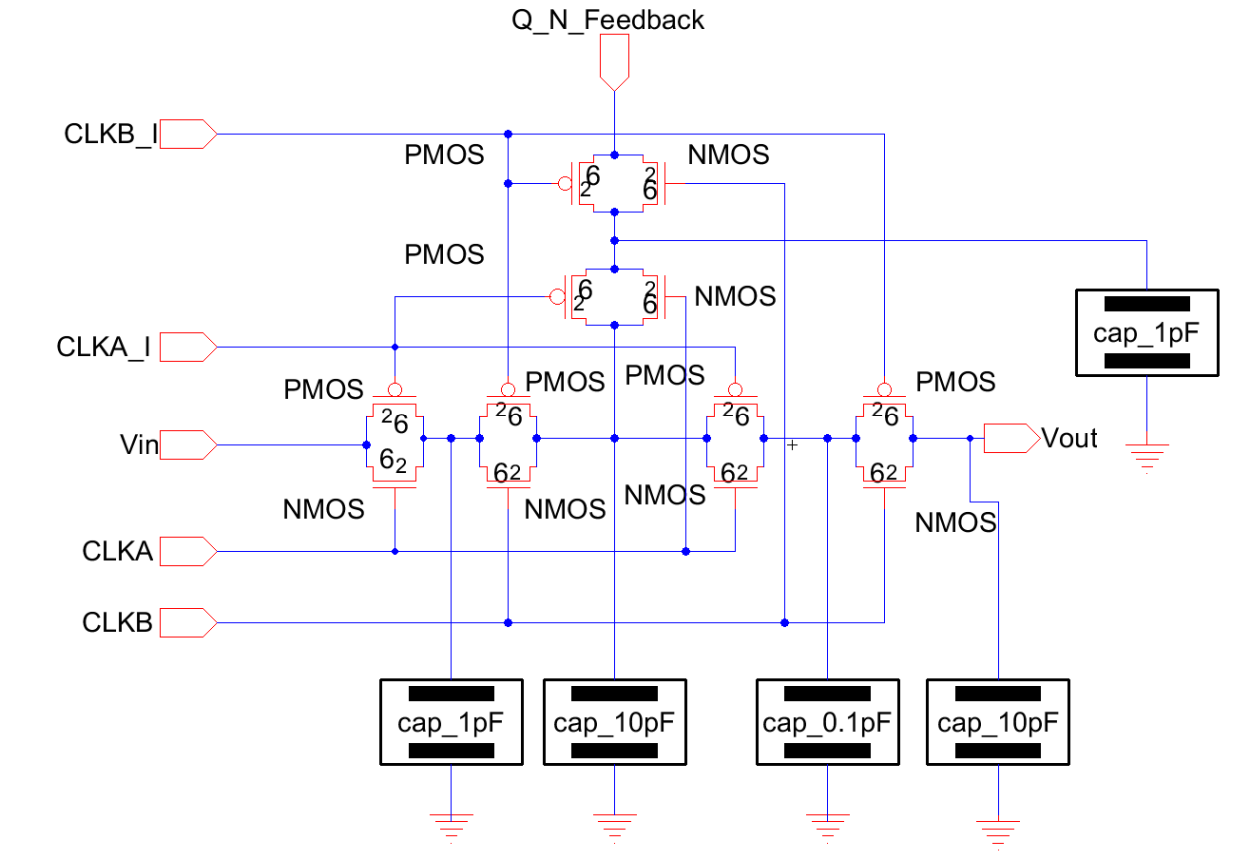
Appendix A.5 Schematics and Layouts for Chapter 5



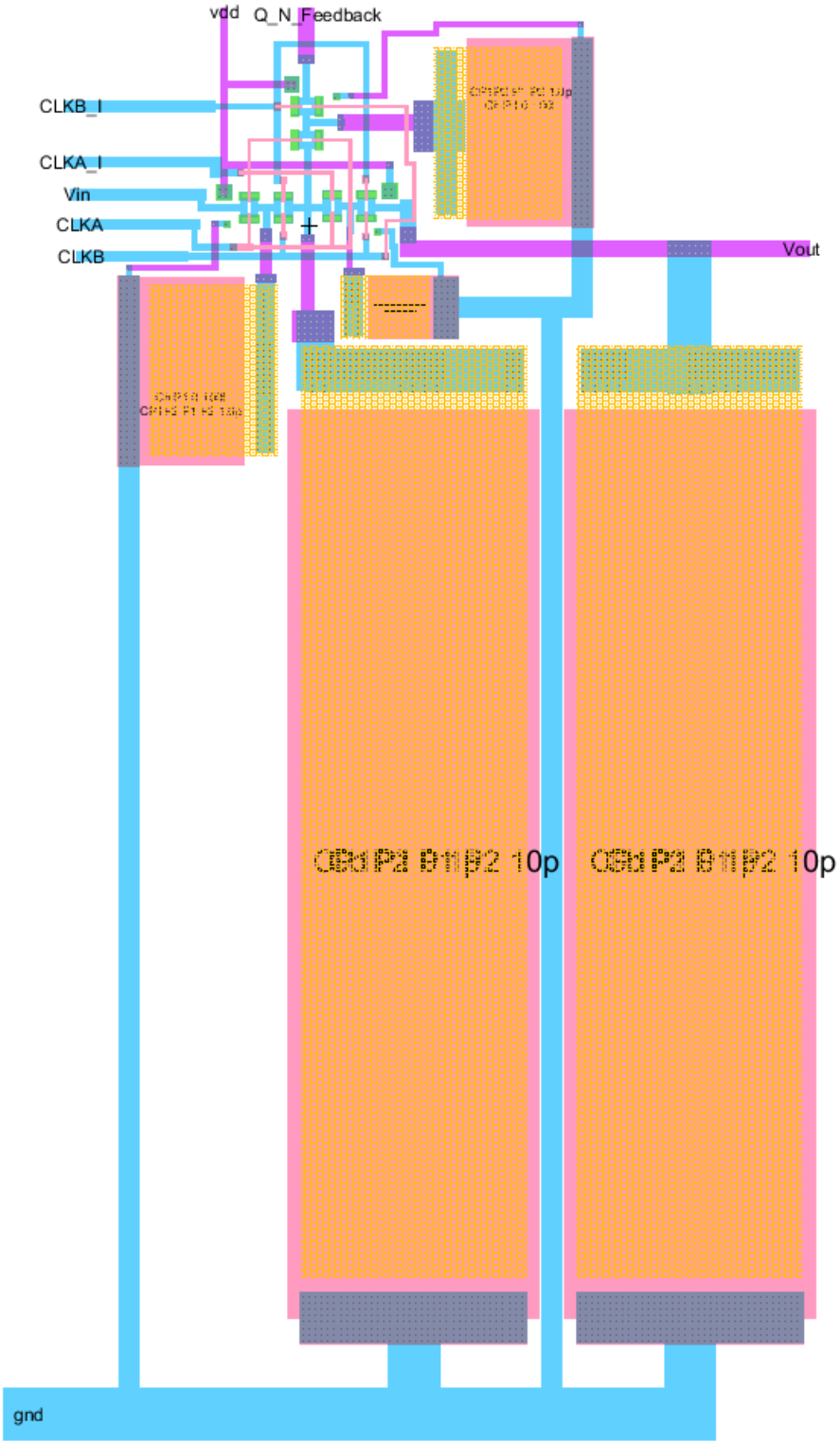
A.5.1 – Schematic of switched capacitor sigma-delta modulator.



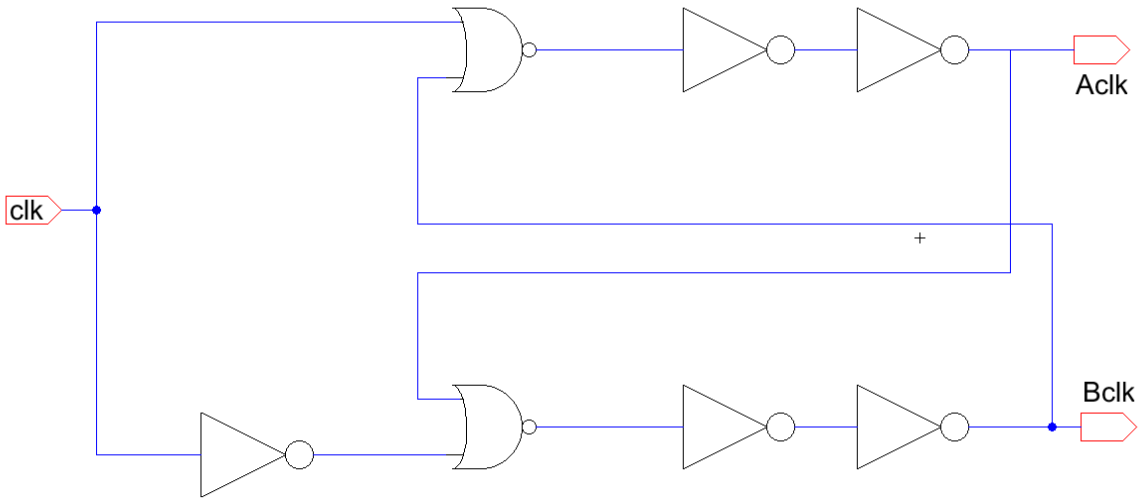
A.5.2 – Layout of switched capacitor sigma-delta modulator.



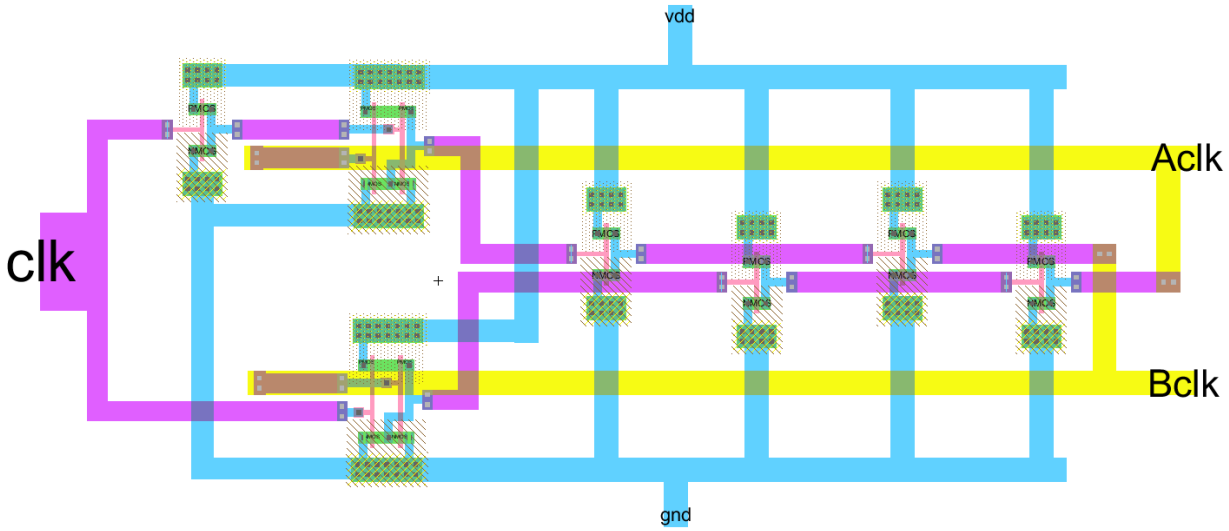
A.5.3 – Schematic of switched capacitor filter network.



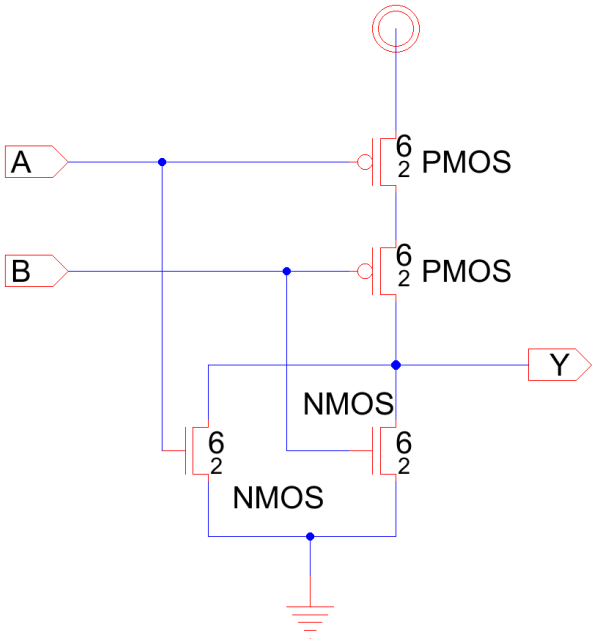
A.5.4 – Layout of switched capacitor filter network.



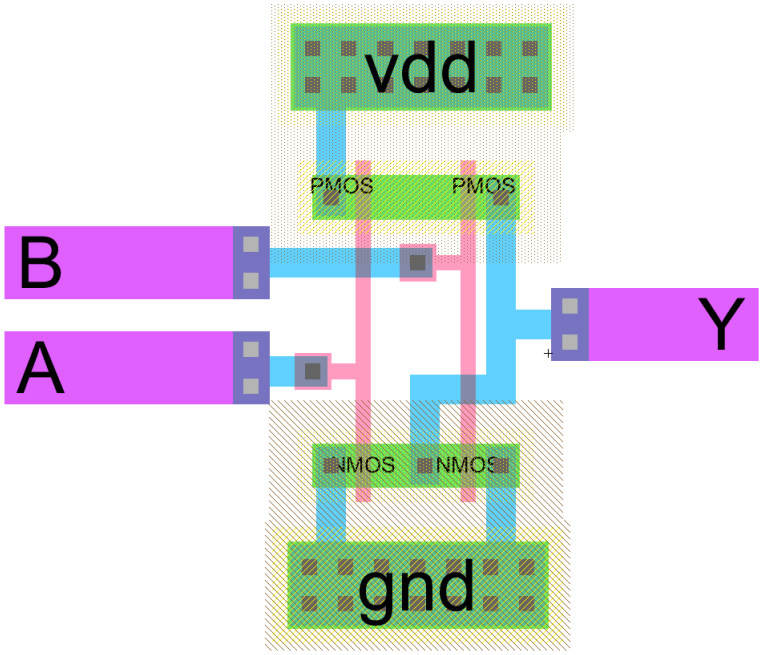
A.5.5 – Schematic of non-overlapping clock generator.



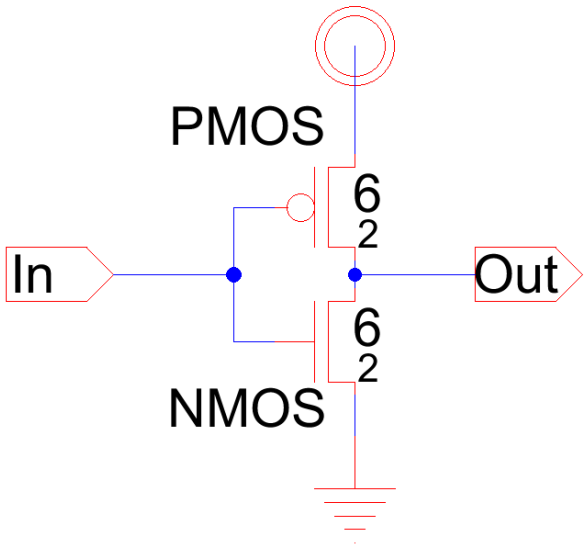
A.5.6 – Layout of non-overlapping clock generator.



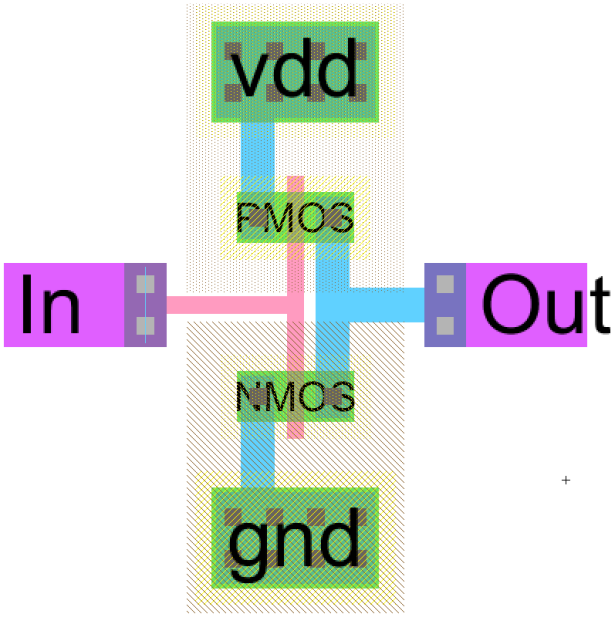
A.5.7 – Schematic of NOR gate.



A.5.8 – Layout of NOR gate.

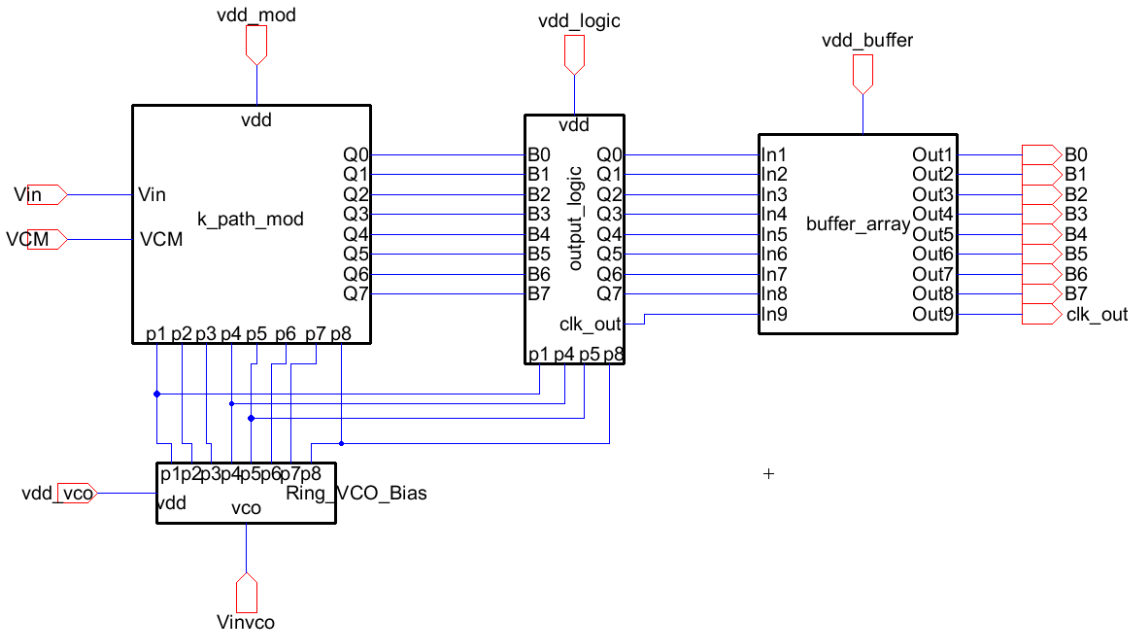


A.5.9 – Schematic of minimum size inverter.

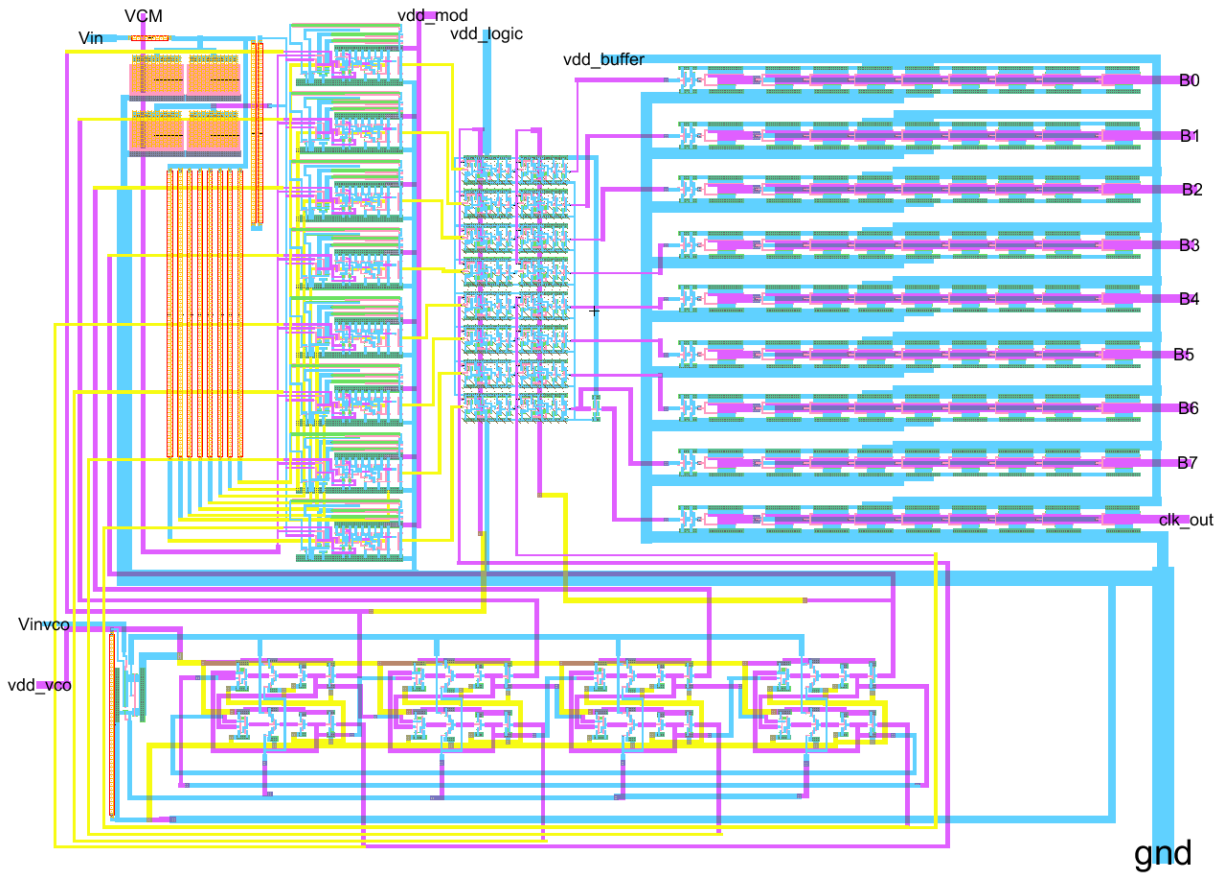


A.5.10 –Layout of minimum size inverter.

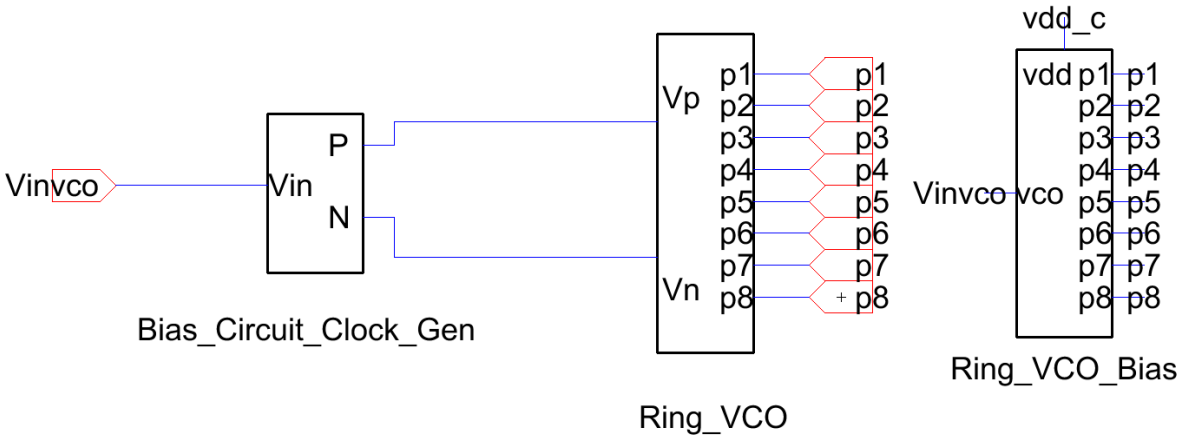
Appendix A.6 Schematics and Layouts for KD1S Described in Chapter 6



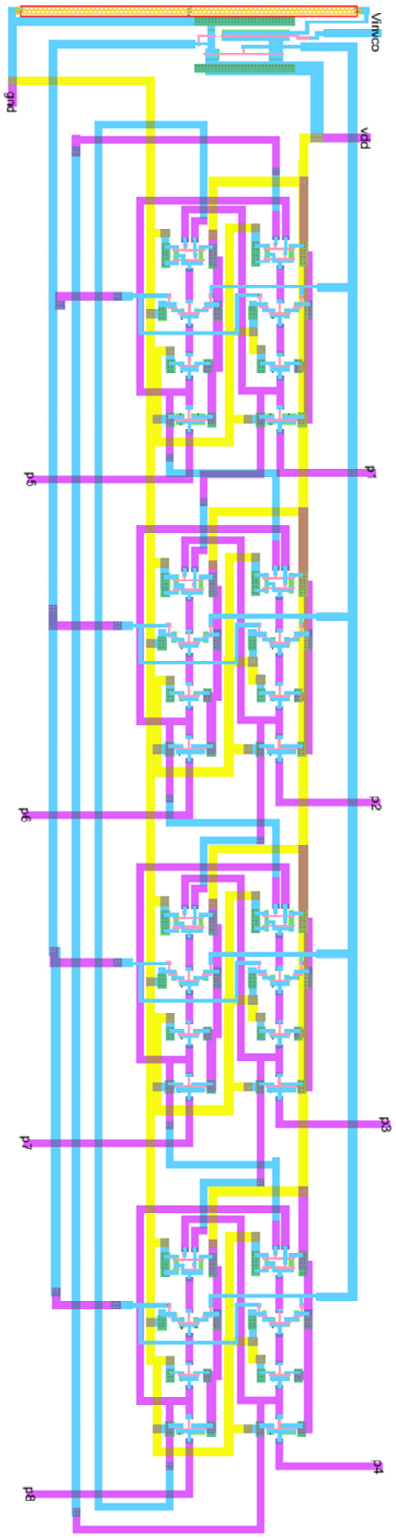
A.6.1 – Schematic of complete KD1S modulator.



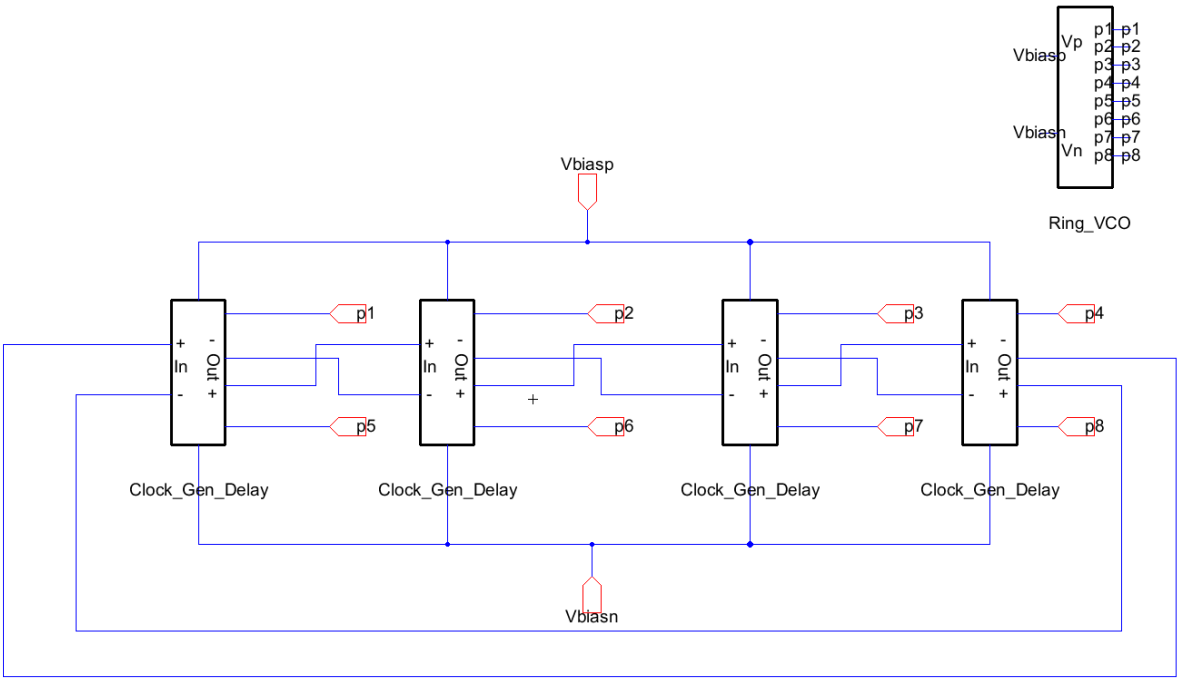
A.6.2 – Layout of complete KD1S modulator.



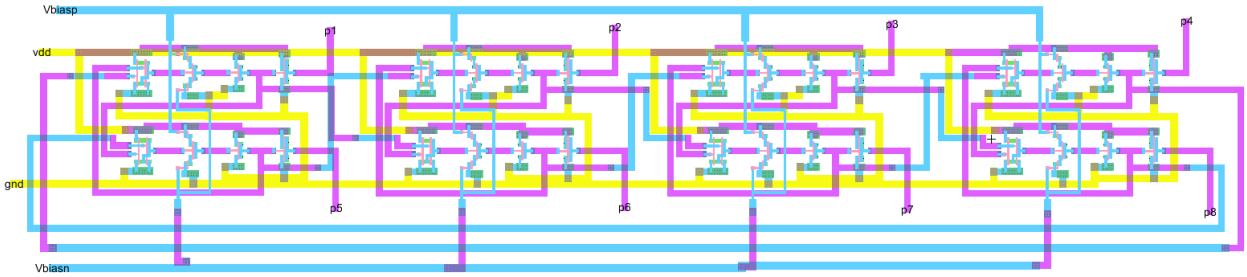
A.6.3 – Schematic of complete 8 phase VCO.



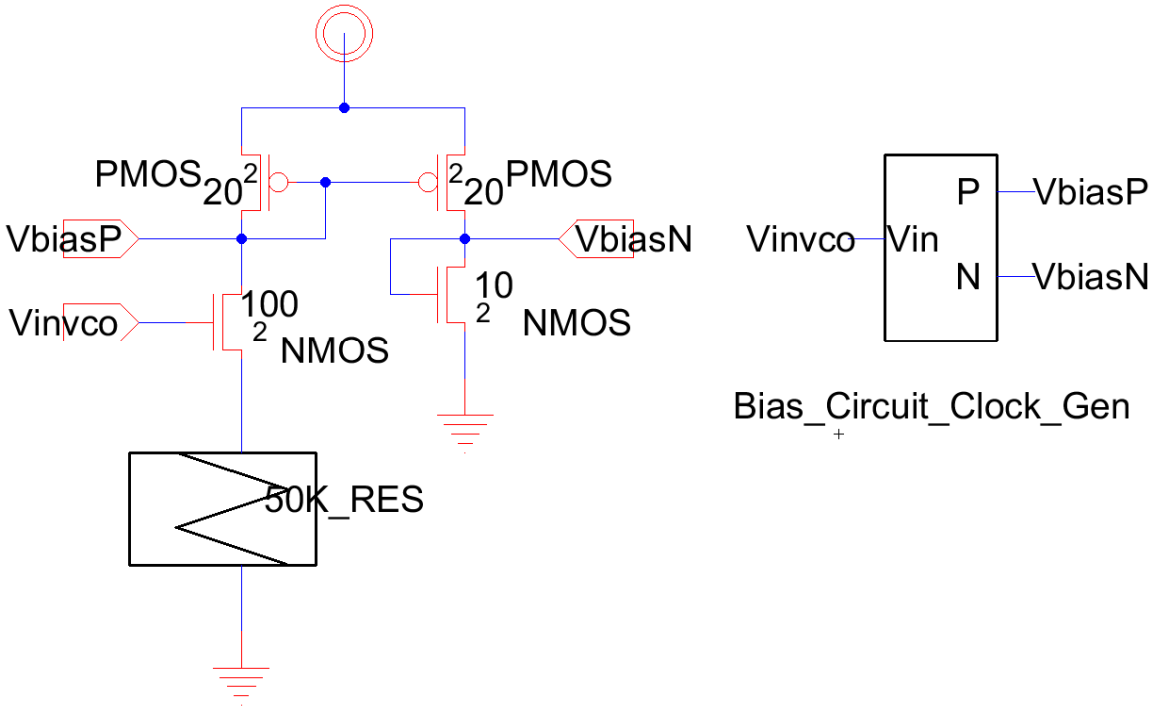
A.6.4 – Layout of 8 phase VCO (rotated 90 deg for clarity).



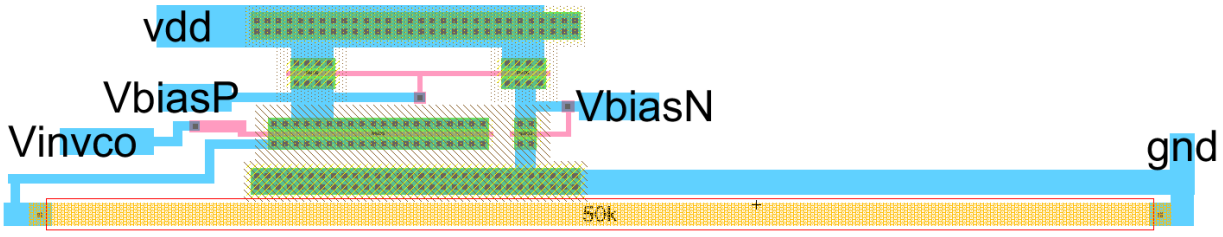
A.6.5 – Schematic of 8 phase VCO without biasing circuitry.



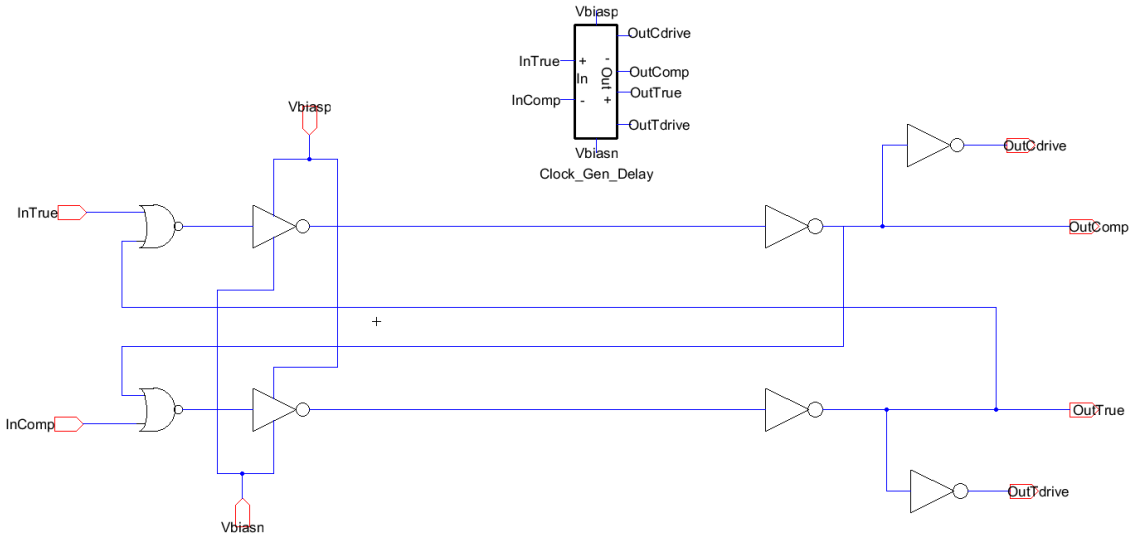
A.6.6 – Layout of 8 phase VCO without biasing circuitry.



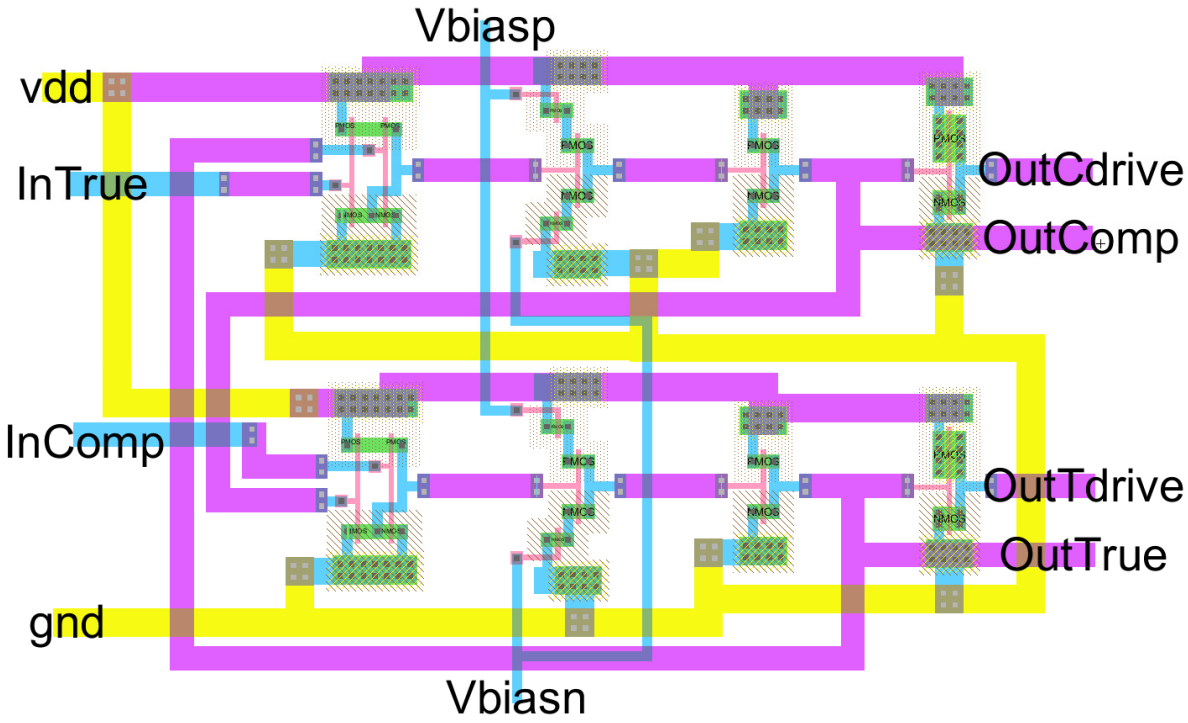
A.6.7 – Schematic of VCO biasing circuitry.



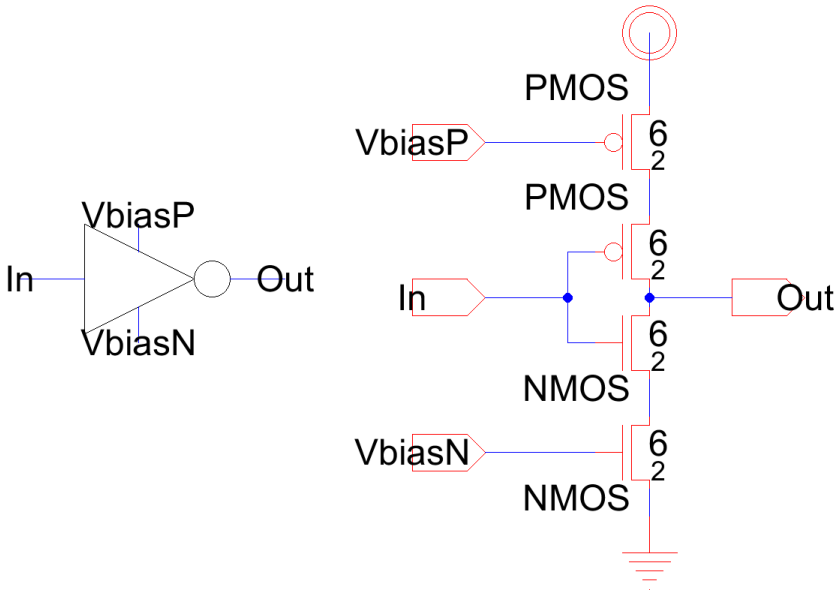
A.6.8 –Layout of VCO biasing circuitry.



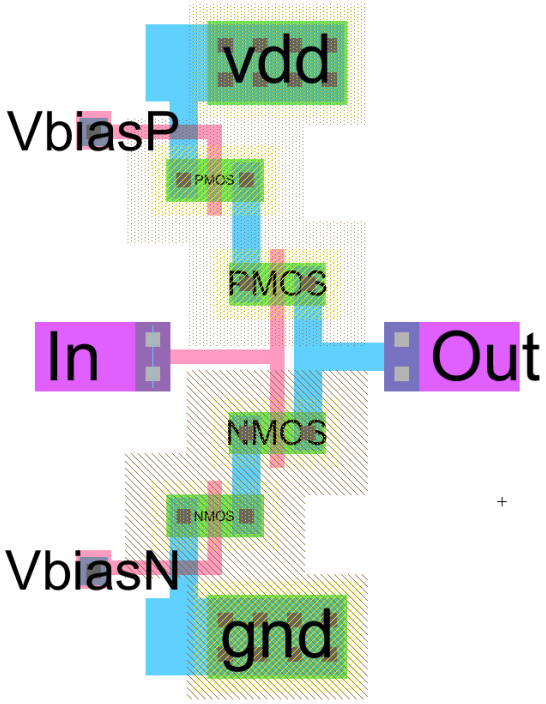
A.6.9 – Schematic of delay unit.



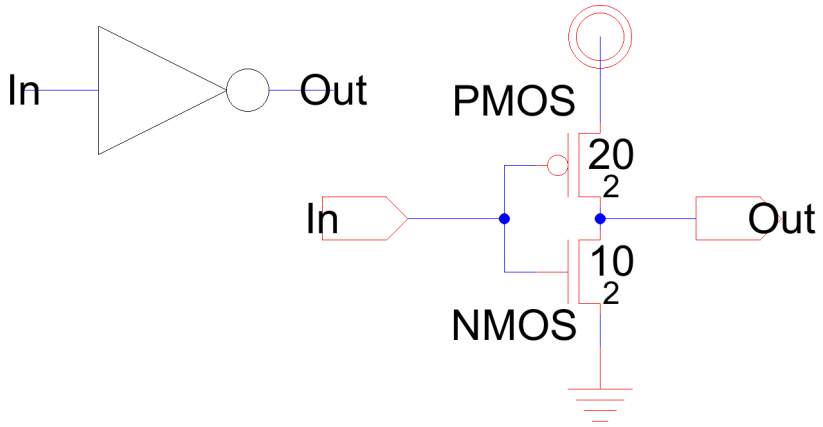
A.6.10 – Layout of delay unit.



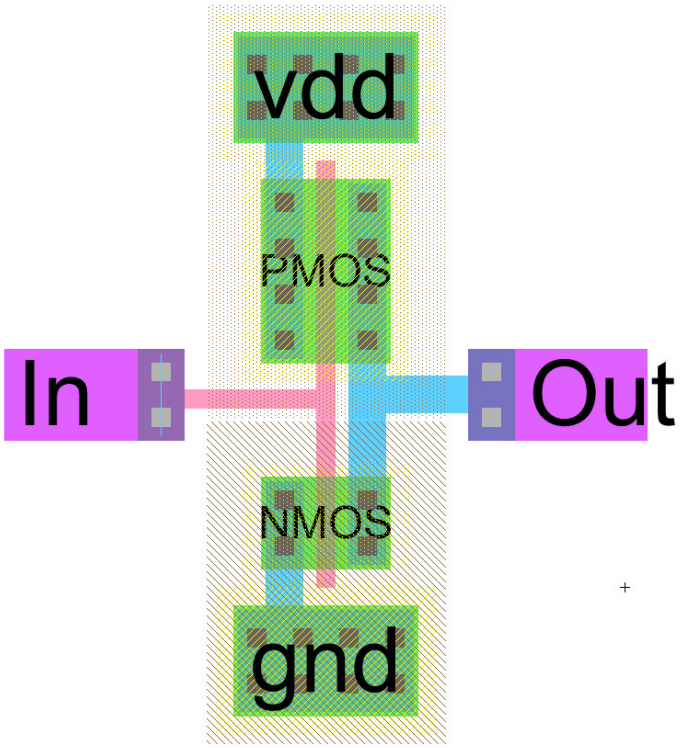
A.6.11 – Schematic of current-starved inverter.



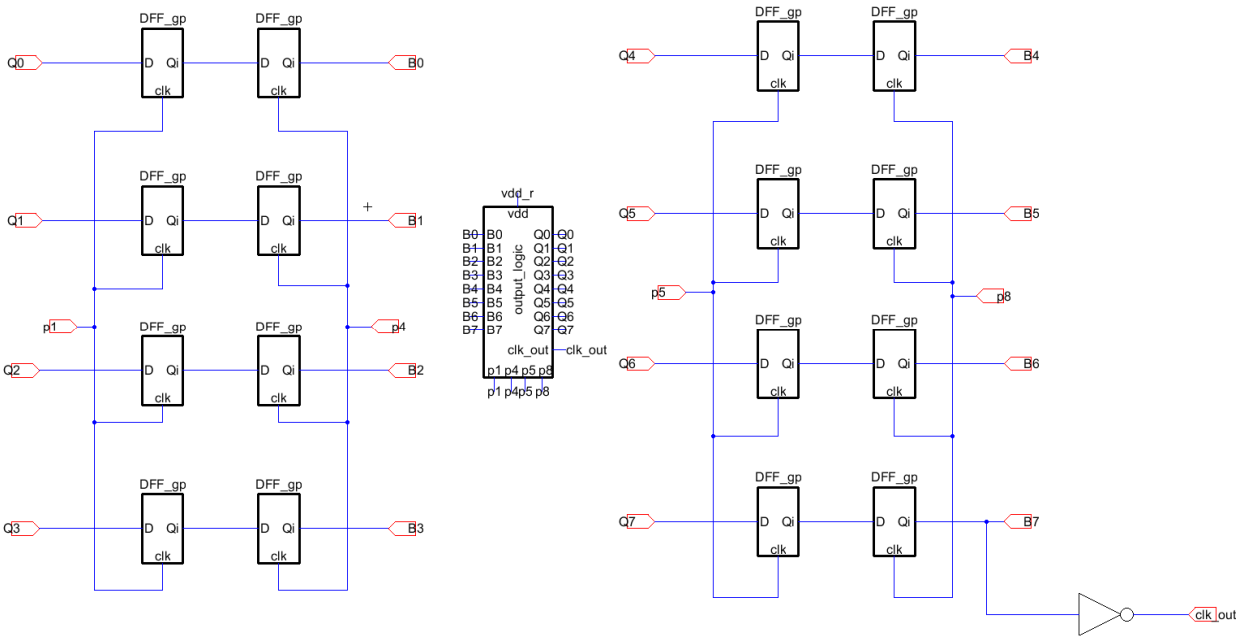
A.6.12 – Layout of current-starved inverter.



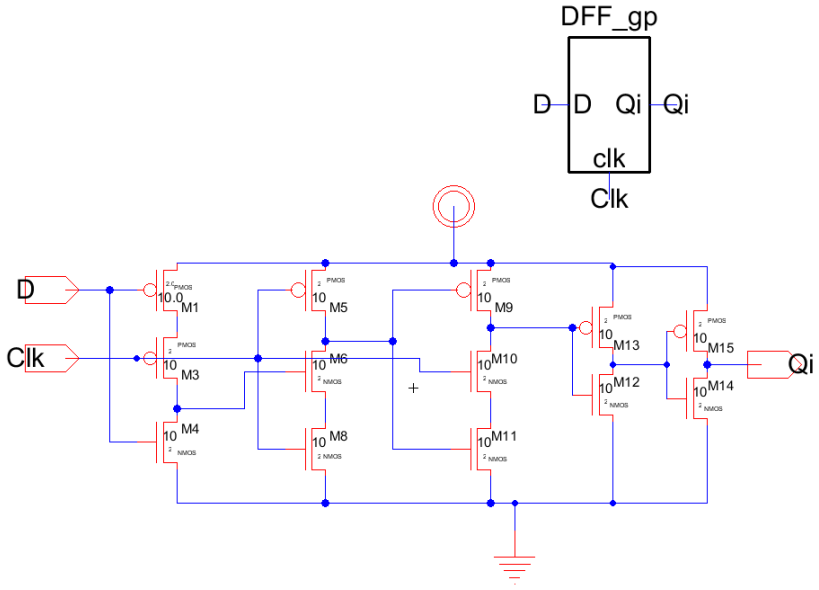
A.6.13 – Schematic of output drive inverter found in delay unit.



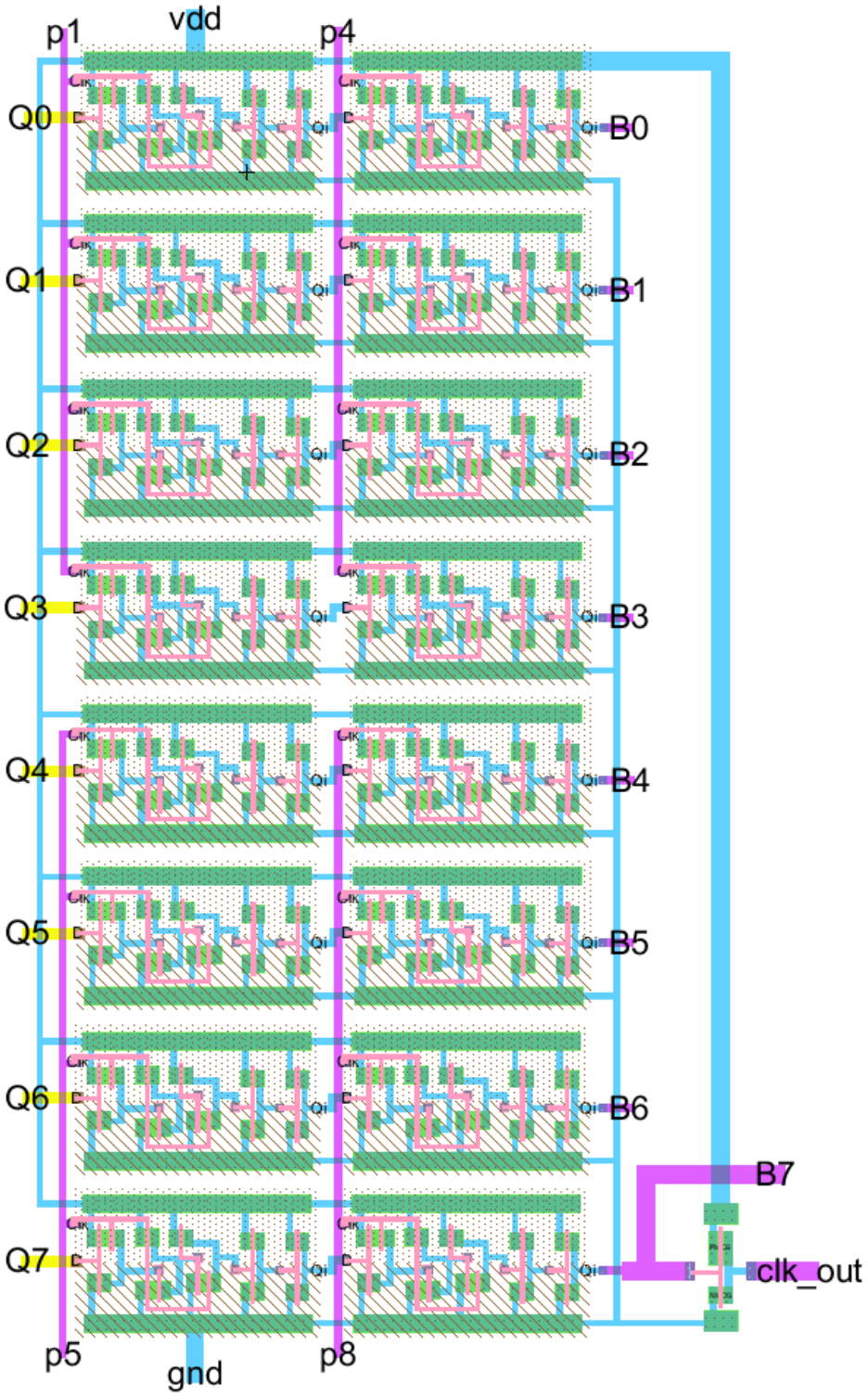
A.6.13 – Layout of output drive inverter found in delay unit.



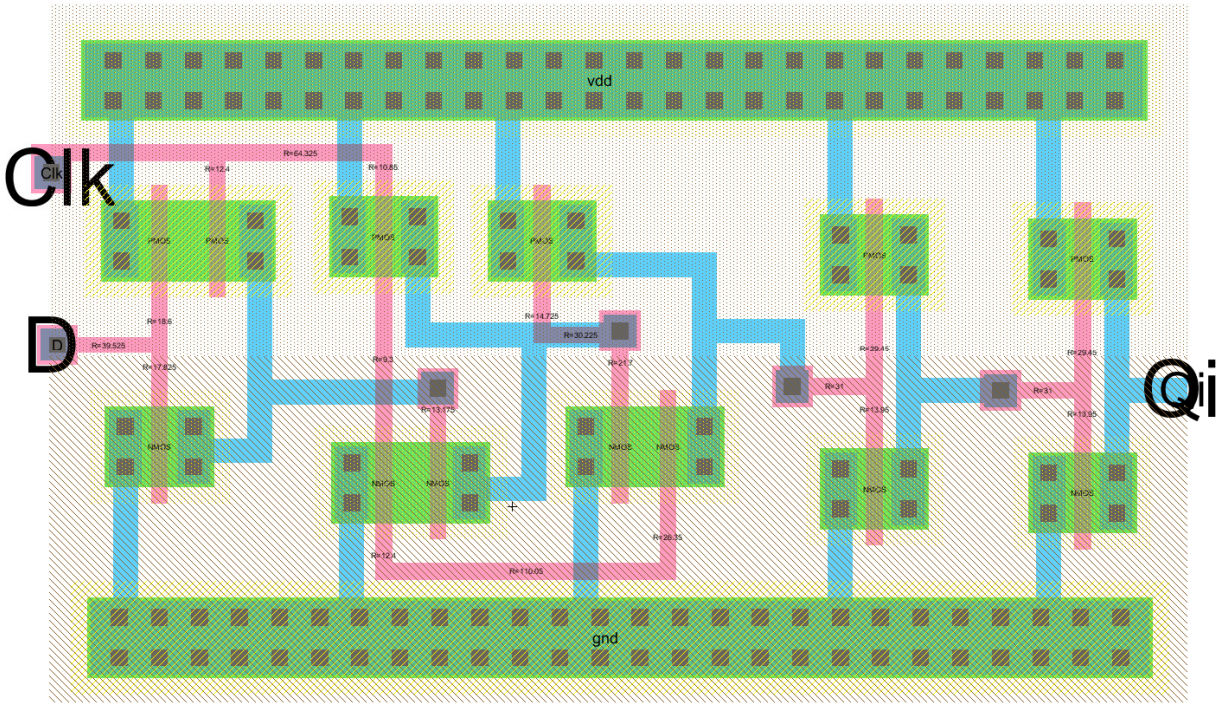
A.6.14 – Schematic of 8-bit register.



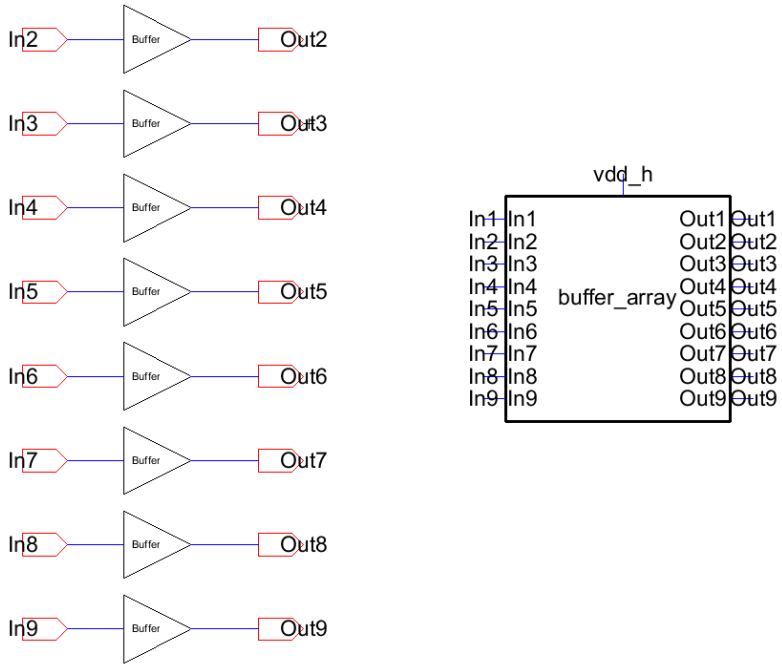
A.6.15 – Schematic of D flip-flop.



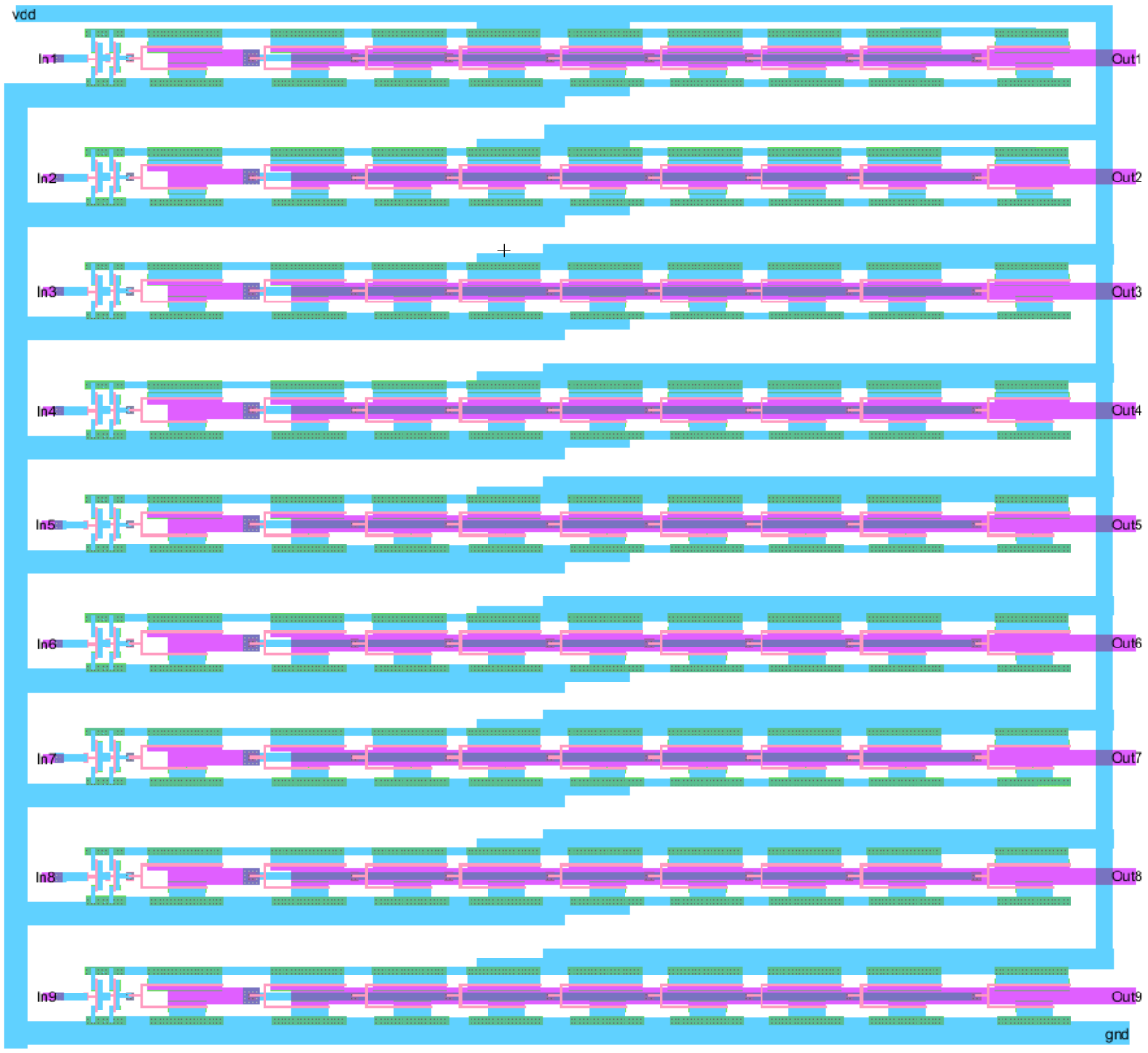
A.6.16 – Layout of 8-bit register.



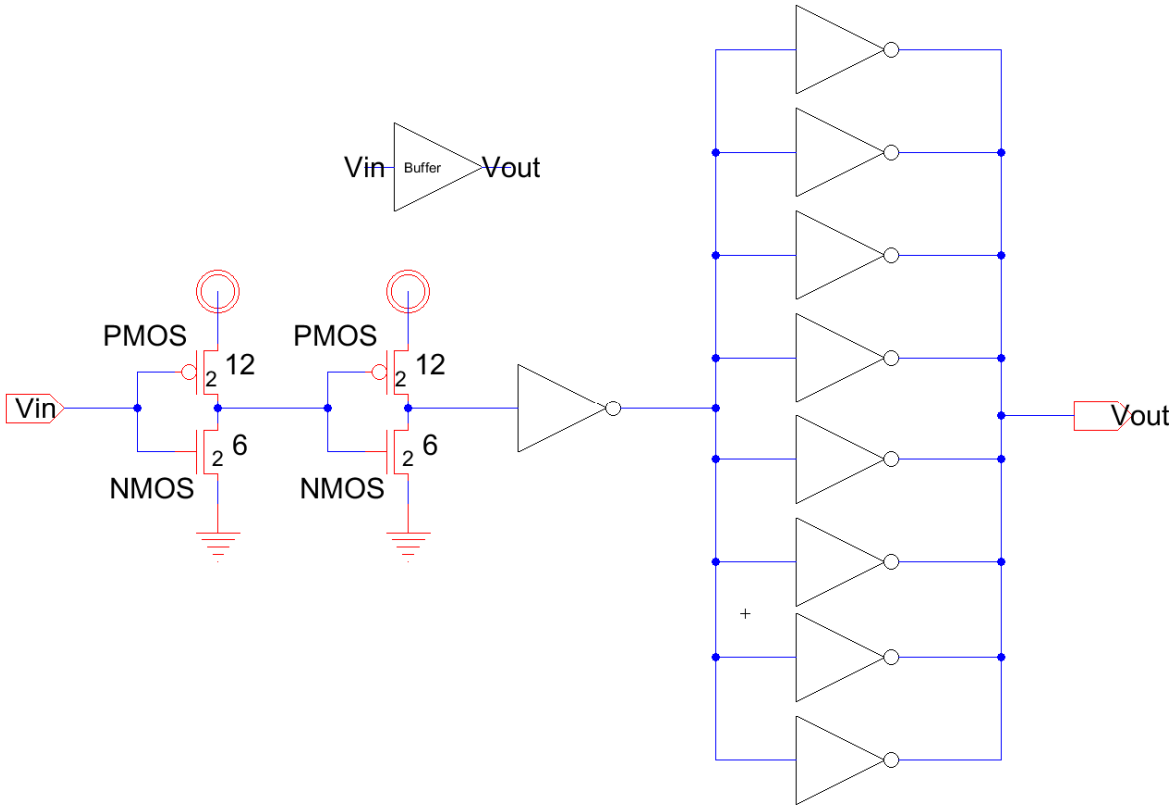
A.6.17 – Layout of D flip-flop.



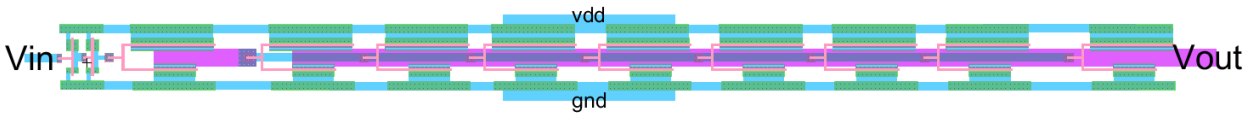
A.6.18 – Schematic of buffer array.



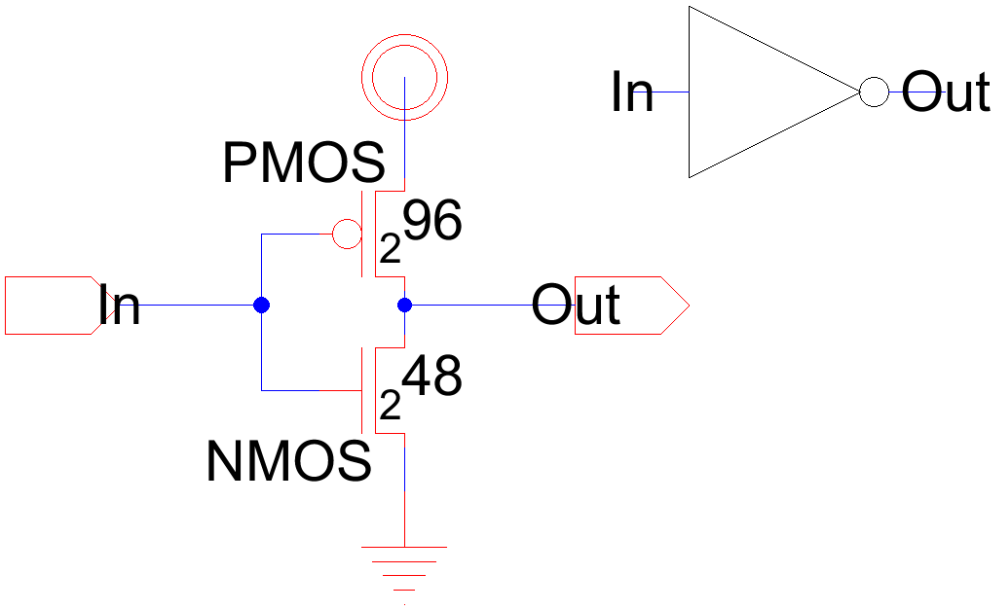
A.6.19 – Layout of buffer array.



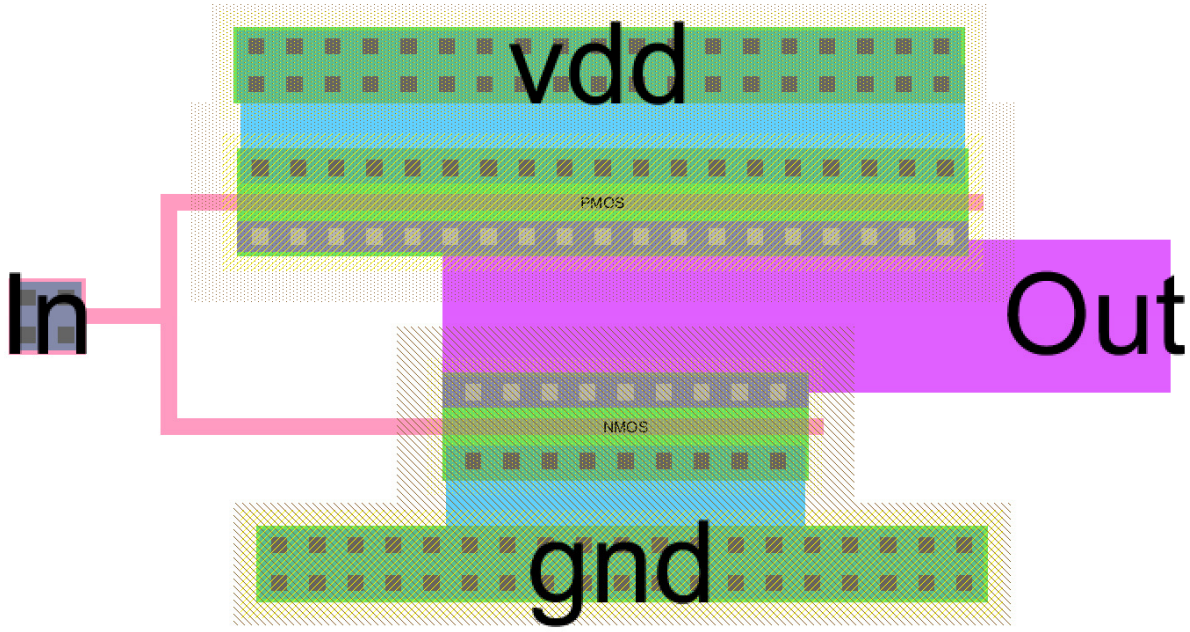
A.6.20 – Schematic of buffer.



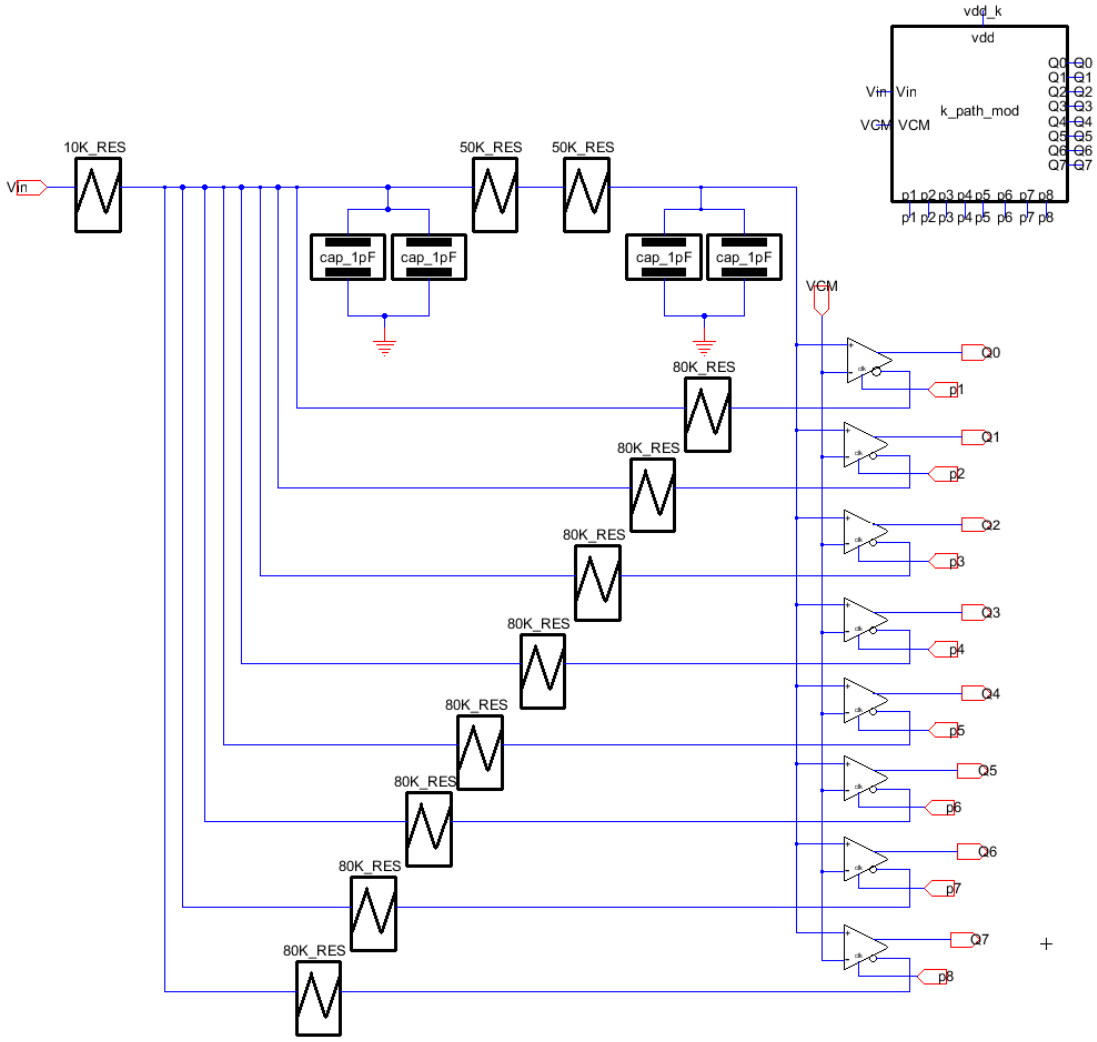
A.6.21 – Layout of buffer.



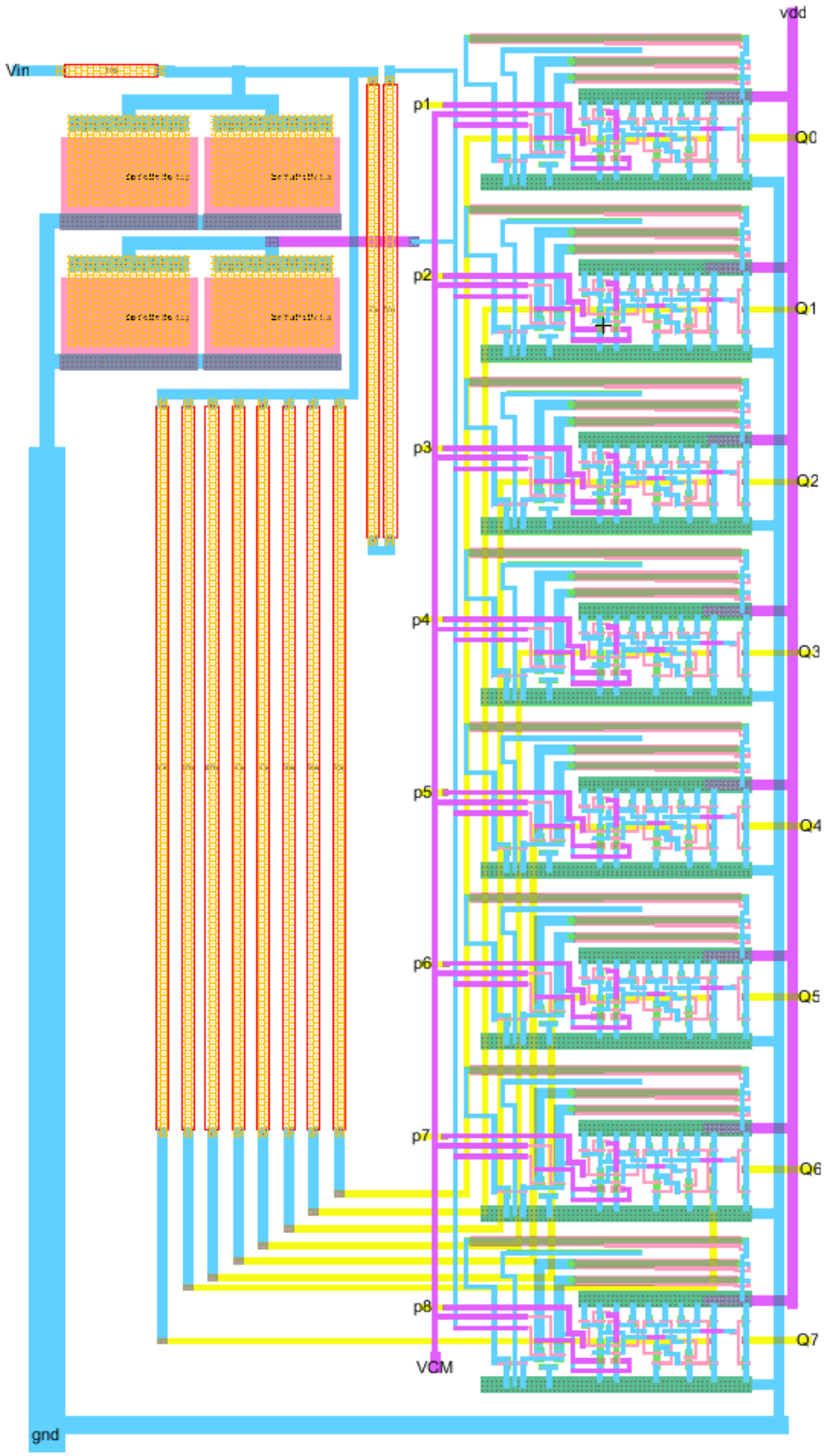
A.6.22 – Schematic of large inverter found in buffer.



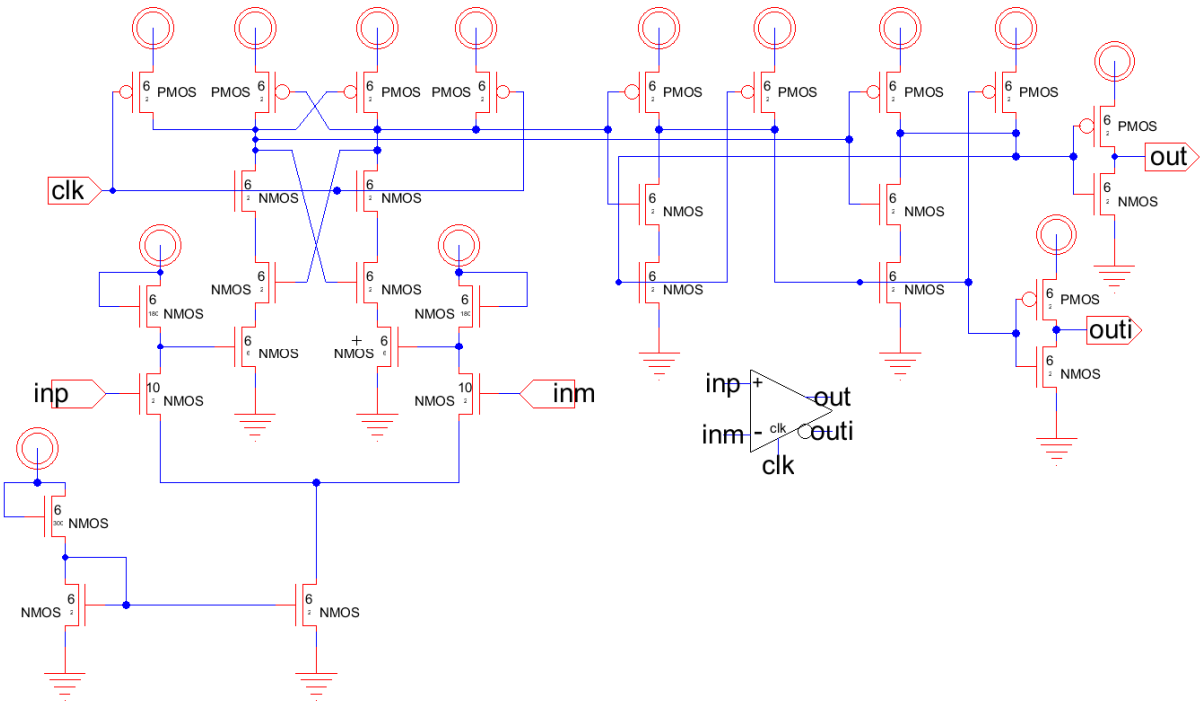
A.6.23 – Layout of large inverter found in buffer.



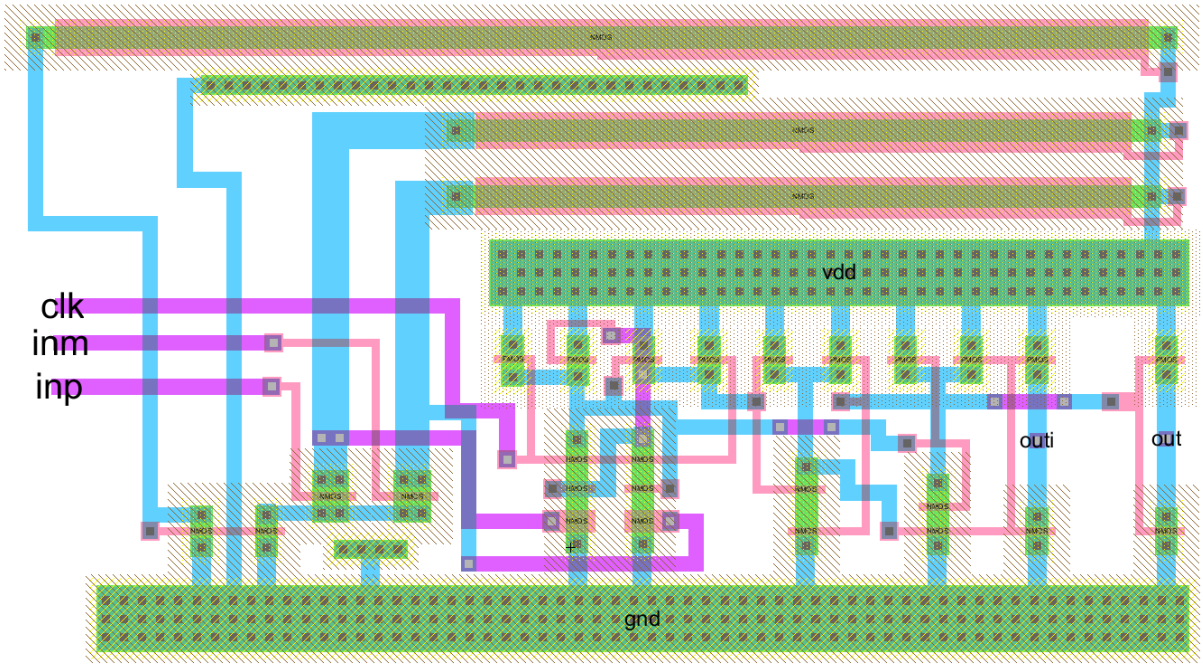
A.6.24 – Schematic of KD1S modulator.



A.6.25 – Layout of KD1S modulator.



A.6.26 – Schematic of comparator with preamplifier.



A.6.28 – Layout of comparator with preamplifier.