Study On Fault Tolerant Control Of Cascaded H Bridge Multilevel Inverter

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Abstract: In this study, the state-of-art of the multilevel inverters and the modulation techniques were done to understand the system research better. Although there are a large number of multilevel inverter topologies, in this literature H-Bridge Cascaded multilevel inverters is discussed. Modulation techniques and the general strategy for fault-tolerant control of H-Bridge Cascaded multilevel inverters are reviewed. Intensive studies have been performed on space vector PWM methods in open loop control of inverters and on different types of fault that occurs in the cell, line.switchs, etc.

Key Words: *Cascaded H-bridge rectifier, Fault diagnosis and protection, Fault-tolerant design, Redundancy and reliability*

I. Introduction

With the advancement of power electronics and the emergence of new multilevel converter topologies, it is possible to work at voltages beyond the level of individual power devices. Multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the rating of the individual power devices [1], [2]. Moreover, the cascaded H-bridge converter (CHB) is the most attractive topology as far as front-end applications are concerned. In fact, it allows both fewer components to be used and a simple layout because of its modular structure. As the number of power electronic switches increases, the inverter's cost rises proportionately. Additionally, the possibility of fault occurrence in the inverter surges, leading to degraded reliability of the power electronic system. Since interruption of operation in the commercial and industrial power applications is not acceptable, high reliability is one of the vital desired characteristics of an inverter [6, 8]. Therefore, investigating the sources of fault and the effects of a certain type of fault on the operation of multilevel inverters through study of fault-tolerant control schemes is imperative.

II. TOPOLOGY OF MULTILEVEL INVERTERS

Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

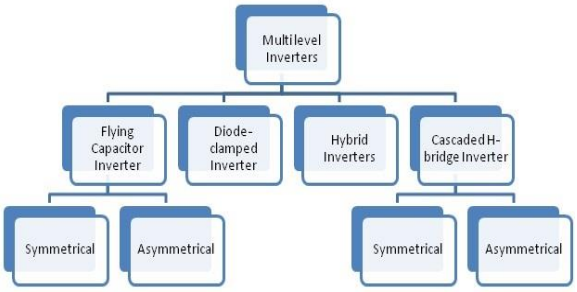

Fig:1 Multilevel inverters

There are essentially three types of multilevel inverters:

- **Cascaded H-Bridges:**

H-Bridge Cascaded multilevel inverters circuit consists of diodes and switches. This is the most common type of inverter and usually uses Separate DC sources (SDCs). However, due to recent advancements, single DC source H-Bridge Cascaded inverters can also be formed.

- **Diode Clamped:**

This type of inverter uses capacitors and diodes for inversion. The aim is to convert DC voltage into capacitor voltage. Proper precautionary measures should be taken in order to avoid over charging of capacitors.

- **Flying Capacitor:**

This is a relatively complicated way of inversion, because the capacitors need to be pre charged, and is somewhat similar to diode clamped method. The difference is that clamping is done through capacitors instead of diodes

III. CASCADEDH-BRIDGE INVERTER

The cascaded H-bridge inverter has drawn tremendous interest due to the greater demand of medium-voltage high-power inverters. The cascaded inverter uses series strings of single-phase full-bridge inverters to construct multilevel phase legs with separate dc sources.

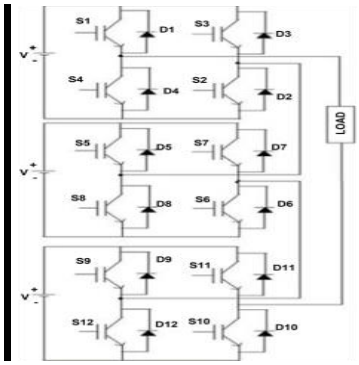

Fig2. Cascaded H-Bridge Multilevel Inverter

A single phase three level H-bridge Multilevel Inverter is shown in Figure 2. The output of each H-bridge can have three discrete levels, results in a staircase waveform that is nearly sinusoidal even without filtering. A single H-bridge is a three-level inverter. Each single-phase full-bridge inverter generates three voltages at the output: 0, $+V_{dc}$ and $-V_{dc}$. Their Switch States and the Output Voltages are shown in fig 3

The advantages for cascaded multilevel H-bridge inverter are the following: The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge and no extra clamping diodes or voltage balancing capacitors are necessary. Switching redundancy for inner voltage levels is possible because the phase voltage is the sum of the output of each bridge. The disadvantage for cascaded multilevel H-bridge inverter is it needs separate DC sources.

S_{a1}	S_{a2}	S_{a1}'	S_{a2}'	S_{b1}	S_{b2}	S_{b1}'	S_{b2}'	V_{ao}	V_{bo}	V_{ab}
0	0	1	1	1	1	0	0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-V_{dc}$
0	0	1	1	0	1	1	0	$-\frac{V_{dc}}{2}$	0	$-\frac{V_{dc}}{2}$
1	1	0	0	1	1	0	0	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	0
0	0	1	1	0	0	1	1	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0
0	1	1	0	0	0	1	1	0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
1	1	0	0	0	0	1	1	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	V_{dc}

Fig 3.Switch States and the Output Voltages for Diode-Clamped Multilevel Inverter

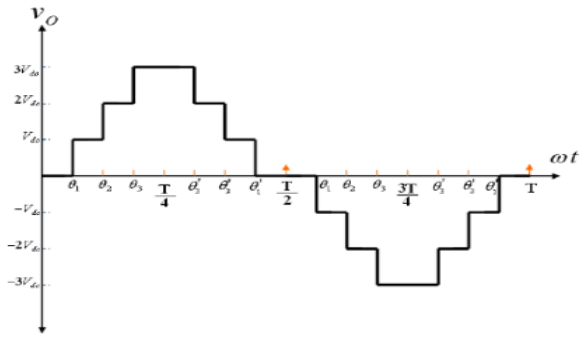

Fig.4 Staircase Sinusoidal Waveform Generated by Cascaded H-Bridge Multilevel Inverter

IV. CONTROL AND MODULATION TECHNIQUES OF MULTILEVEL INVERTERS

Classification of Modulation Strategies

The modulation methods used in multilevel inverters can be classified according to the switching frequency Modulation techniques that work with high switching frequencies have many commutations for the power semiconductors in a cycle of the fundamental output voltage. Multilevel inverters generate sinusoidal voltages from discrete

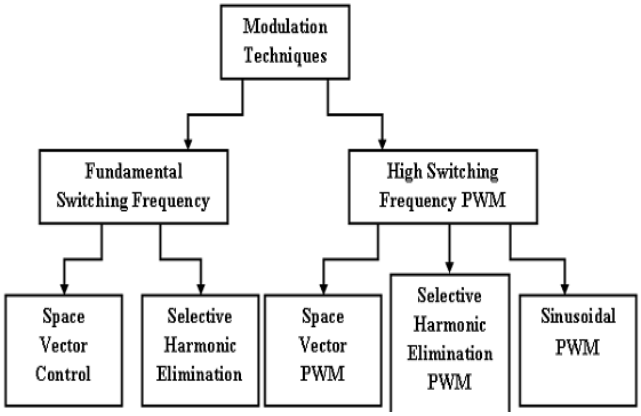

Fig.4 Control and modulation techniques

voltage levels, and Pulse Width-Modulation (PWM) strategies accomplish this task.Three multilevel modulation methods most discussed are multilevel carrier-based sinusoidal PWM, selective harmonic elimination, and multilevel space vector PWM.

Benefits

- It has more flexibility to alter the number of voltage levels and also Can be extended to higher level by adding/deleting the H-bridge units
- Easy to design and extend to higher level
- It has minimized gate drive circuits
- Additional H-bridge is not required
- symmetrical configurations
- Equal load sharing is possible

- Lesser conduction losses
- Minimized switching losses
- It can operate at fundamental switching
- The most economical converter version
- It offers very least count of devices to obtain more levels
- Number of redundant states are more
- Equal load sharing is possible

Limits

- Not suitable for fault tolerant applications
- Voltage balancing problem happen
- Input DC sources were sharing Load unequally
- The higher rating switches are not functioned at fundamental switching frequency
- High count of input DC sources are required
- Semiconductor switches with higher voltage ratings are essential
- Semiconductor switches experience multiple voltage stresses
- Not possible to get all levels of the output voltage (only few odd levels can achieve 5, 9, 13, 17…etc.)
- The inverter demands additional DC source to generate all levels of output of proposed topology.
- Following papers have discussed this limits and have overcome these limits.

V. Fault analysis

This structure is capable of reaching medium output voltage levels using only standard w-voltage mature technology components. The cascaded multilevel inverters can be divided into two groups from the view point of the value of the voltage sources used. If the values of the dc voltage sources are equal, the multilevel inverter is usually called the symmetric topology unless it is called asymmetric topology. The symmetric CHB multilevel inverters have good modularity but they use higher number of switches.Since several H-bridge converters are required in a CHB multilevel converter, a large number of power switching devices will be used which will reduce the reliability of the system. It is important to maintain normal operation under fault conditions because failed operation of a converter could cause tremendous losses for consumers, especially when the CHB converter is feeding critical loads. It is, therefore, a key issue to design a fault-tolerant system to improve system reliability.

Inverter Operating with Bypassed Cells

Faults in square wave inverter are a big concern. Since a square wave with dc voltage source of 100 volts having a square waveform of +100 to -100 and its RMS(Root Mean Square) value is 100 but when a fault occurs in any of the 4 switches like open circuit or short circuit fault there are two possibilities in the voltage waveform i.e. 0 to +100 or 0 to -100. In both cases the RMS value is (100/sqrt(2)) or 70 (approx). to identify the fault occurs the RMS value of the signal is taken continuously over a period of 0.02 seconds and passed through a relational operator of (<=80). If there is a fault occurs in the system the output signal of the relational operator is 1. This signal can be utilised for fault diagnosis i.e. for turning off the dc supply. Therefore fault analysis of inverter is necessary. The faulty element needs to be isolated from the system and make the system perform its task under compromised conditions.

There are mainly two kinds of faults which need to be identified.

- Switch faults and
- phase faults.

The former is based on faults like open circuit and short circuit faults in IGBTs and can be judged using two different ways. The first one is to connect the voltage or current sensor in each IGBT and the second one is to observe the output waveform and classify the faults by taking its THD values using Neural Network. The neural network has the output ports that govern the gate input signals of IGBTs by modifying them according to the type of fault. Neural Network is a network that updates itself according to the situation and adapts itself by checking the difference between the desired input and actual input and making it zero by changing the weights and biases inside the neurons. The inspiration of neural network is taken from animal nervous system which adapts itself by connecting and disconnecting connections among themselves. Neural network consist of weighted function that multiplies with the input signal to give the output signal, bias for constant addition purpose, summer for addition of addition of two or more inputs and an activation function like pure linear, tangent sigmoid, and sigmoid function. Neural Network after setting its no of layers, number of neurons and activation function has its random outputgenerate some certain signals to open and close some switches which allow the inverter to operate under low level and low power conditions.. The neural network output is of 1 digit which tell us about the faulty switch which then decoded into three binary digits. The first digit represents the cell number. For a five level inverter their are two cells so if the first digit is zero then cell 1 is faulty, if 1 then cell 2 is faulty. The next two digits represent the IGBT number i.e. 1(00) ,2(01) ,3(10), 4(11)

In paper (2)Only two types of fault have been taken into account in semiconductor power devices.

- short circuit fault
- open circuit fault

Open circuit fault type

This type of fault appears when a switch remains off (even when the gate signal has been turned on); this situation avoids energy transfer to the load shows a diagram of this kind of fault). The failure probability of this type of fault is 18% regarding total converter faults. When a fault is produced in any converter cell, voltage level is lost (positive or negative) according to the failed switch. However, two voltage levels are lost regarding the failed cell once a failure has been isolated with the auxiliary.

Short-circuit fault type

This type of fault is presented when a switch is turned on and the complementary switch of an inverter leg or a short circuit in a DC power supply. Energy transfer to the load is thus not possible; the consequence is an over current in the power supply and the corresponding transistors. Depending on fault time duration, system protection can be activated (the whole system may become shut down). The probability of this kind of fault is 15% of total Similar to the above, two output voltage levels are lost Different situations can produce both types of failure, probably due to faulty gate control modulation an internal fail.

Fault-tolerant scheme

Fault detection and isolation (FDI) analysis must do before implementing any system converter failures switch.

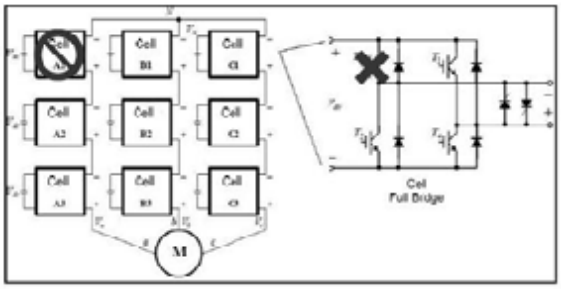

Fig.5 Open circuit fault in one cell

. Several methods can be used for FDI: sensing resistance, transformation of the output current and sensing V_{CE} The actuator as sensor method is used in this work for fault detection through V_{CE} and V_{GE}.

In-phase pulse width modulation (IPDPWM) reconfiguration

This paper analyses the fault-tolerant technique in a cascade multilevel inverter without physical component replacement; this method involved the in-phase pulse width modulation (IPDPWM) technique assigning six phase carrier signals (triangles) at different voltage levels compared to a reference (sine wave) for determining the switching pattern. The signals generated from comparing them were assigned to the six pairs of switches (keeping symmetrical waveform).The idea was to analyse modulation index limits and use the semiconductor power devices' symmetry for reconfiguration purposes; material redundancy (modification of components) is necessary for the fault-tolerant technique, in other words, the modulation software (gate signals) implies hardware reconfiguration (semiconductor power devices), but there is no material redundancy.

Reconfiguration for only one faulty cell

When any fault occurs (in a semiconductor power device) the switch to the corresponding cell must be isolated and stopped. For example, considered that cell A1 was faulty then the signals corresponding to the fault cell are those at the upper and lower ends The carrier signal must thus be modified for a waveform to avoid carrying out the comparison and thus leave cell The other two cells (phase B and C) must compensate for the energy delivered by the faulty cell. it can be seen that the modulation index in the other phases was forced to increase just when the faulty cell stopped transferring energy to the load.It does not matter which cell has switch failure with this reconfiguration, provided that gate signals are properly reassigned since the carriers in the top and bottom cell are assigned to the fault.So far, the solution has been presented with only one faulty cell; however the system can keep running with this method even if the fault is present in two-cell stage,

Reconfiguration for a cell having two faults

In this case, when two cells are faulty (in the same phase), the reference waveform becomes modified and does not compare with the four corresponding carriers, so phase voltage now has only three levels (only one cell working). The other references should compensate for a longer period Expressions describing waveforms for references based on modulation index limits are presented in

Voltage level was maintained even when a fault occurred, having minimum degradation of phase A voltage (6% reduction), while the other phases were compensated for, so that line voltage remained unchanged (22% increase). In other words, the power remained constant because the energy which was not provided by the faulty phase was compensated for by the other phases (lacking faults).

Fault in bridge

In two full bridges when only one was faulty presents three phase signals, before and after the occurrence of two failures (two failures occurred at the same time and in different cells of only one phase). The voltage of phase A having a 4- level degradation regarding waveform without fault is also presented; in this case, output waveform was the classic case of a 3- level inverter converter. The diagram shows that introducing the fault led to degradation of 2 output voltage levels, in the same way that voltage became degraded. It is interesting to know whether a system still remains balanced, i.e. if energy failing to provide a phase with failure is compensated for by energy supplying other stages which are not faulty has strong voltage phase degradation (49% reduction), while the other phases compensated for it so that line voltages remained unchanged and the system was balanced 20% increase).

As can be seen, the effect of loss of levels was only displayed during phase A and voltages between phases had no visible changes the advantage of maintaining balanced line to line voltage even after a fault happens in a switch with one or two cells in a particular system. This is important regarding charges requiring operation with balanced line voltages, such as induction motors. The reconfiguration strategy allowed the system to become repaired without having to suspend operation.

(2) In paper a fault-tolerant control strategy for cascaded H-bridge rectifier is presented. The proposed strategy for the fault-tolerant system is redundancy. In fact, the modularized

CHB converter is very suitable for achieving this goal because all H-bridge cells are identical. One H-bridge is added to the CHB converter as a backup to maintain operation even when one of them fails. The redundancy is achieved if we can bypass the H-bridge cell that contains the failed device, so that a cascade failure is prevented and normal operation is maintained. Compared with previous solutions, this strategy saves bypasses and isolated switches and keeps the same input voltage level. The control strategy and fault-tolerant design are explained in detail and confirmed with simulation results.. The redundant H-bridge concept helps to deal with device failures and to increase system reliability.

In Fig. 6 the basic block diagram of the utilized controller is shown. This diagram consists of analog and digital controllers. The analog controller generates the pulse width modulated (PWM) signal, Q, and the digital controller determines the appropriate switching functions h1 to h_N. The digital controller also generates a synchronized square-wave signal to control both the active and active powers. Investigation of different fault situations Commercial IGBTs can be categorized into plastic-pack (module type) and press-pack in terms of packaging. Plastic pack IGBTs have single-sided cooling and act as open-circuits in failure mode with the possibility of case rupture and an arc flash event .Press-pack IGBTs act as short-circuits in the event of a failure. When the chip fails, the silicon is metallurgical alloyed with an optimized contact partner and a permanent conductive path is formed through the chip [15]. Devices operating in this so called "circuit failure mode (SCFM)" will remain in a low impedance state under all possible load conditions for a certain period of time. Reference [16] calculates analytically the short circuit failure mode endurance and estimates an appropriate service interval, after which the failed devices have to be removed and replaced with new ones. In this paper, it is assumed that the semiconductor devices are based on press-pack technology and have SCFM capability. Our goal is to show how to improve system reliability by using additional features in the control system. When one of the power semiconductor devices fails, the key to achieving redundancy is to bypass the failed. switch. In fact, we use the failed state of a device to bypass the corresponding H-bridge without any additional bypass power switch. This requires that the failed H-bridge DC side is opened and that the AC side is shorted [17]. To achieve this goal, if one top/bottom switch fails another top/bottom switch is turned on and the other two complementary switches are turned off. Sensing a device short and bypassing the failed H-bridge in time and correctly are very important to prevent failure propagation. Therefore, to diagnose the faults, an arbitrary H-bridge cell (from N H-bridge cells) is investigated under different operating conditions. For this study, it is assumed that only one switch fails short, during operation. Figures 5 to 8 illustrate different fault-free conditions and Tables II to V show the corresponding AC terminal voltages under faulty conditions.

Case 1: Vin > 0 and Iin > 0

Case 1: Vin > 0 and Iin > 0

Case 2: Vin > 0 and Iin < 0

Case 3: Vin < 0 and Iin > 0

Case 4: Vin < 0 and Iin < 0

When a ML-type fault is detected, depending on the input voltage and current signs, the failed switch is diagnosed. For example, in cases 2 and 3 only one switch could generate the ML-type fault, so it is

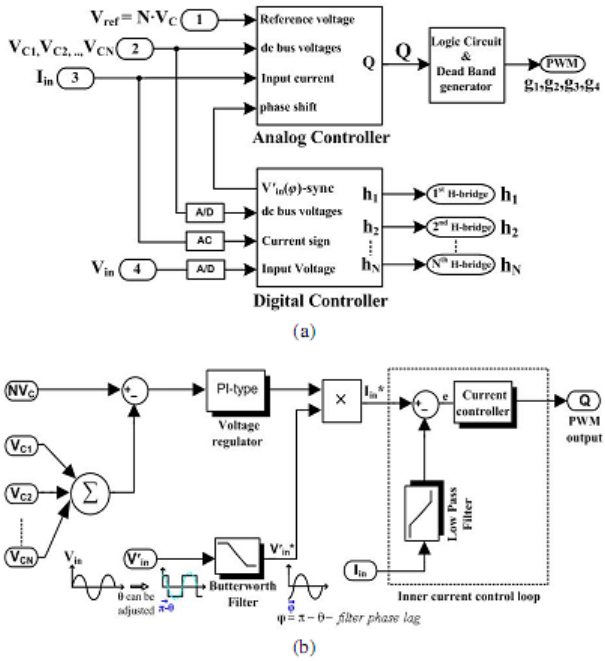

Fig.6 Basic block diagram of analog and digital controllers.

To detect. But, in cases 1 and 4 two switches could generate the ML-type faults. In case 1, switch S3 is permanently off while switch S2 has switching actions. So, the failure probability of S2 is much more than S3. Similarly, in case 4, the failure probability of S4 is much more than S1. In these cases, the protection circuit will turn on the bottom switches S2 and S4. However, if the failed switch is S1 or S3, it will cause a SC condition and a SC fault is generated. The SC fault is then used to correct the previous decision. After the fault is detected and the failure location is diagnosed, the protection algorithm should bypass the failed cell using the strategy shown.

Conclusion

The results from this study represent a beneficial basis for matching of inverter topology and the best control scheme according to different Fault conditions to implement in the fault tolerent control for multilevel inverters.

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