A 4 bit Ripple Carry Adder using High Speed Low Power Hybrid Full adder Tested at Various Technology

Rohit Sharma[1], Rakesh Kumar[2], Manish Verma[3], Ravindra Chejara[4]
[14]*Research scholar, ECE, Sobhasria Group of Institution, Sikar*
[23]*Assistant Professor, ECE, Sobhasria Group of Institution, Sikar*

Abstract- In this paper, we have designed a 4 bit Ripple Carry Adder using a 1-bit full adder hybrid design utilizing both complementary-metal–oxide–semiconductor (CMOS) logic and transmission gate logic. The adder is first simulated and compared with traditional results at 180nm and 90nm for 1 bit and can be extended as required. We have used the Tanner EDA Tool with version 14.11 in 180nm and 90 nm technologies. After that we have utilized this adder to implement the Ripplle Carry Adder and then calculated the various parameters, such as, power, delay and power delay product (PDP), and compared with the existing adder circuits. For 1.8-V supply at 180-nm technology, the normal power utilization was observed to be to a great degree low with reasonably low delay were reported. The power and delay is calculated as 681.01 nW and 5.53 ps at 180-nm innovation working at 1.8-V supply voltage and 160.65 nW and 14.897 ps at 1.2-V supply voltage at 90nm. The multiplier too was simulated and the results were verified.

Index Terms- Hybrid Technology, Low Power, Complementary MOS, Tanner tool, High Speed

I. INTRODUCTION

Increased usage of the battery-operated portable devices, like cellular phones, personal digital assistants (PDAs), and notebooks demand VLSI, and ultra large-scale integration designs with an improved power delay characteristics. Full adders, being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years . Different logic styles, each having its own merits and bottlenecks, was investigated to implement 1-bit full adder cells. The designs, reported so far, may be broadly classified into two categories: 1) static style and 2) dynamic style. Static full adders are generally more reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart. Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS) , dynamic CMOS logic [4], complementary pass-transistor logic (CPL) , and transmission gate full adder (TGA) are the most important logic design styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation [9]. These designs exploit the features of different logic styles to improve the overall performance of the full adder. The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers [3]. Another complementary type smart design is the mirror adder with almost same power consumption and transistor count (as that of [3]) but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing 32 transistors . However, CPL is not an appropriate choice for low-power applications. Because of its high switching activity of intermediate nodes (increased switching power), high transistor count, static inverters, and overloading of its inputs are the bottleneck of this approach. The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation. However, the other drawbacks of CPL like slow-speed and high-power consumption remain an area of concern for the researchers. Later, researchers focused on the hybrid logic approach which exploited the features of different logic styles in order to improve the overall performance. Vesterbacka reported a 14-transistor full adder employing more than one logic style for their implementation. Similarly, the hybrid pass logic with static CMOS output drive full adder (HPSC) was proposed by Zhang *et al*. . In such HPSC circuit, XOR, and XNOR functions were simultaneously generated by pass transistor logic module by using only six transistors, and employed in CMOS module to produce full swing outputs of the full adder but at the cost of increased transistor count and decreased speed.

II. HYBRID 1-BIT FULL ADDER CIRCUIT

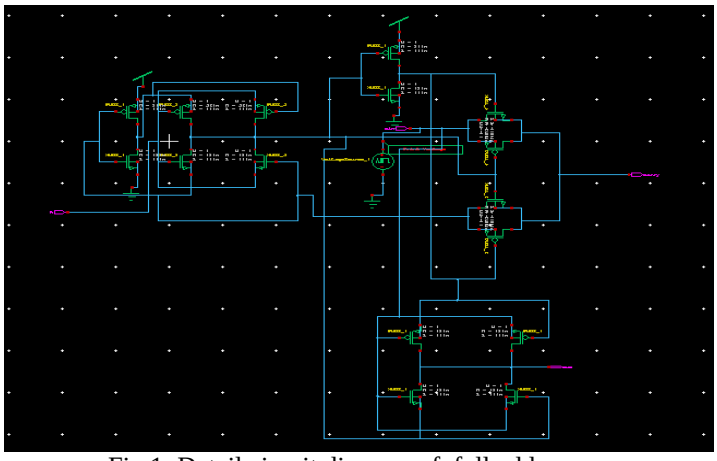

Fig.1: Detail circuit diagram of full adder.

The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem, which has been removed using two pass transistors Mp3 and Mn3. pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6) realize the second stage XNOR module to implement the complete SUM function. Analyzing the truth table of a full adder, the condition for *C*out generation has been deducted as follows:

If, $A = B$, then *C*out = *B*; else,*C*out = *C*in.

The parity between inputs A and B is checked by $A \_ B$ function. If they are same, then *C*out is same as B, which is implemented using the transmission gate realized by transistors Mp8 and Mn8. Otherwise, the input carry signal (*C*in*)* is reflected as *C*out which is implemented by another transmission gate consisting of transistors Mp7 and Mn7. It is likely that a single bit adder cell designed for optimum performance may not perform well under deployment to real-time conditions. This is because when connected in cascaded form, the driver adder cells may not provide proper input signal level to the driven cells. The cumulative degradation in signal level may lead to faulty output and the circuit may malfunction under low supply voltages. To analyze the success of the proposed full adder during its actual use in VLSI applications, a practical simulation environment is setup as shown . To provide a realistic environment, buffers are added at the input and the output of the test bench . The inputs to the adder cell, are fed through the buffers to incorporate the effect of input capacitance and the outputs are also loaded with buffers to ensure proper loading condition. The proposed full adder is simulated using several test bench setups. These test benches are having the common prototype of three buffers at the input and two buffers at the output. They only differed in the number of stages of adder cells used in between the input and output of the simulation setup. The number of stages varied starting from two and increased gradually. It was observed that the carry propagation delay from the input to the output started rising significantly in the order of two after the third stage. Therefore, the three-stage simulation test bench is selected for simulation purpose. Further, the behavior of performance parameters (power and delay) could be measured from the second adder cell by using this test bench. This offered the tested adder cell to have the output and input capacitances of adjacent adder cells as its input and output capacitance; allowing a real time simulation environment for cascaded approach. Numerous random signal patterns were applied at the inputs and the worst case simulation results of the second full adder cell was accounted for analysis and comparison. The performance analysis of the proposed full adder was performed with variation in supply voltage both for 180- and 90-nm technology.

III. RESULT

The proposed Adder also dissipates less static power during mode transitions due to charge recycling. Low leakage currents and the voltage sources provide better stability. Simulation has been done for power dissipations, access time, leakage current and power delay product for the proposed Adder and the results of the proposed Adder are compared with those of other reported existing adder. Result is carried out in 90nm and 180nm.

Table 1 Results Comparison at 180nm Technology

Parameters	Base Designs	Modified Designs
Technology	180nm	180nm
Supply Voltage	1.8 V	1.8 V
Power	4.1563 uW	0.68101 uW
Delay	224 ps	5.5312 ps
PDP	0.931 fJ	3.7668 aJ

Table 2 Results Comparison at 90nm Technology

Parameters	Base Designs	Modified Designs
Technology	90nm	90nm
Supply Voltage	1.8 V	1.2 V
Power	1.17664 uW	0.16065 uW
Delay	0.0913 ns	0.014897 ns
PDP	0.107427 fJ	2.3933 aJ

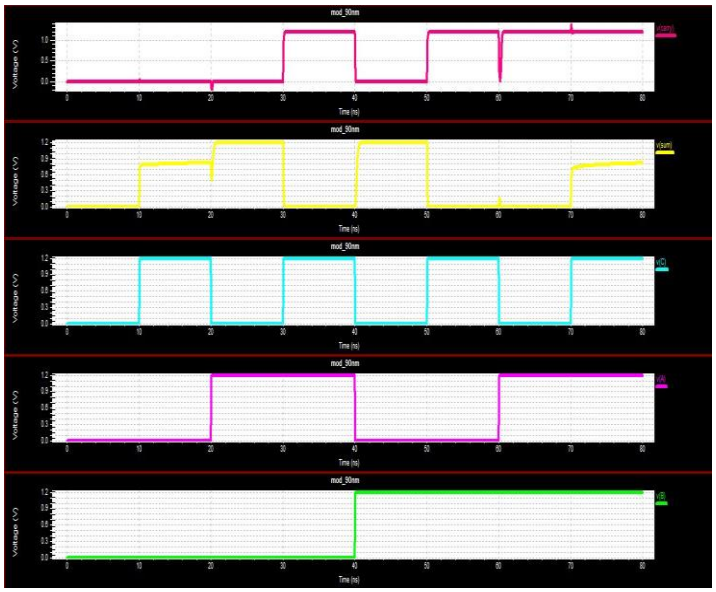

Fig.3: Schematic Waveform at 90nm technology

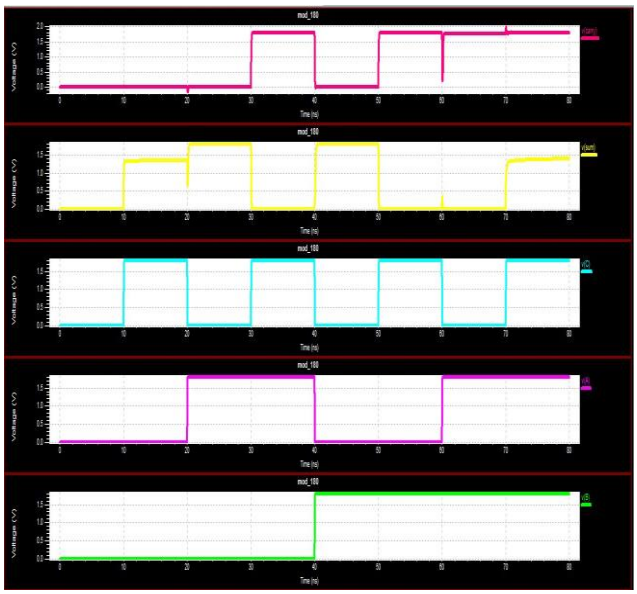

Fig.4: Schematic Waveform at 180nm technology

IV. RIPPLE CARRY ADDER

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.

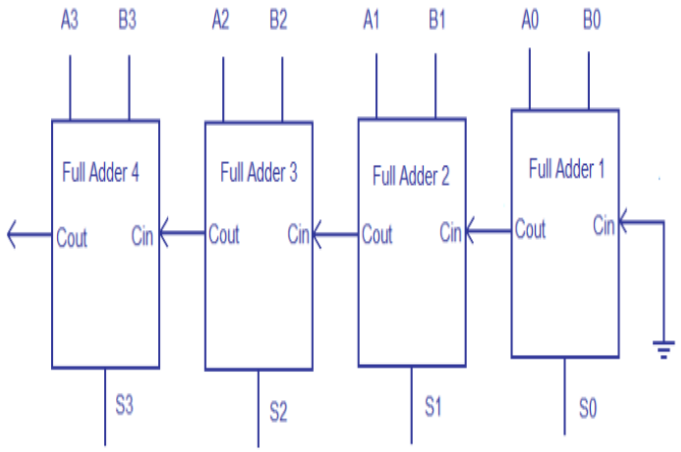

Fig.5: Block diagram of 4-bit Ripple Carry Adder

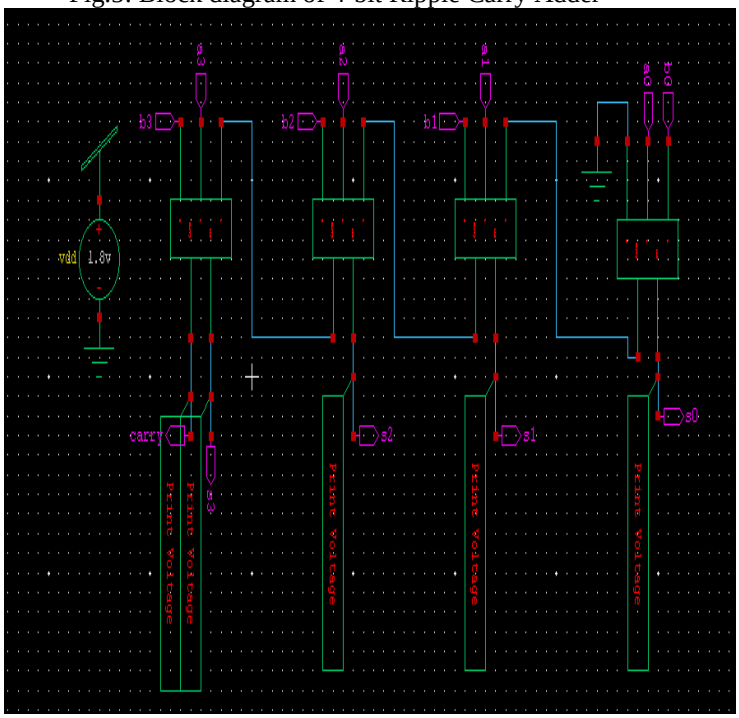

Fig.6: Schematic diagram of proposed 4 bit Ripple Carry Adder

The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder.

For the simulation of 4 bit Ripple Carry Adder, we have used two inputs as

A = 6 & 2 (in decimal) for 40ns each

B = 15 & 8 (in decimal) for 40ns each

so the Sum output would be

Sum = 21 & 10 (in decimal) for 40ns each

We can verify the results with the simulated waveforms

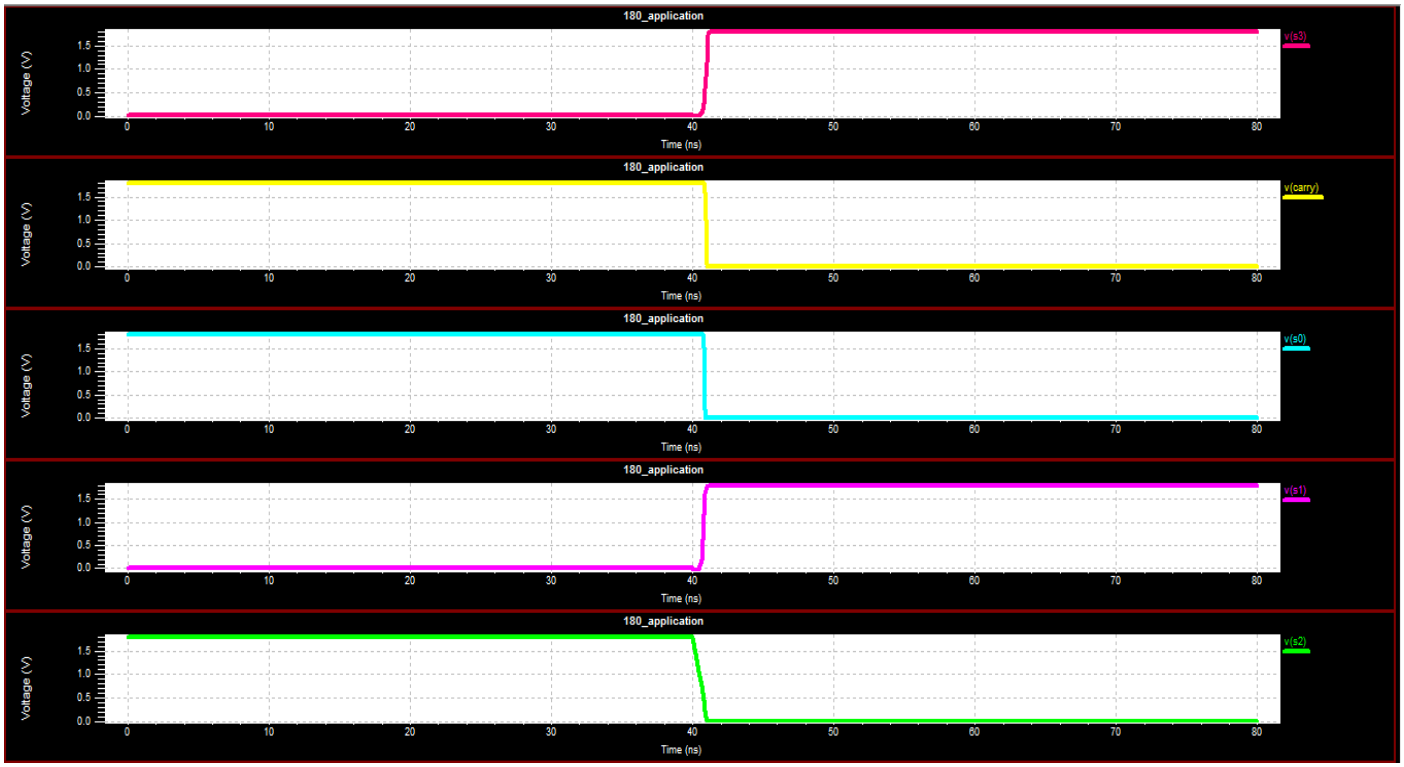

Fig.7: Waveform of proposed 4 bit Ripple Carry Adder at 180nm technology

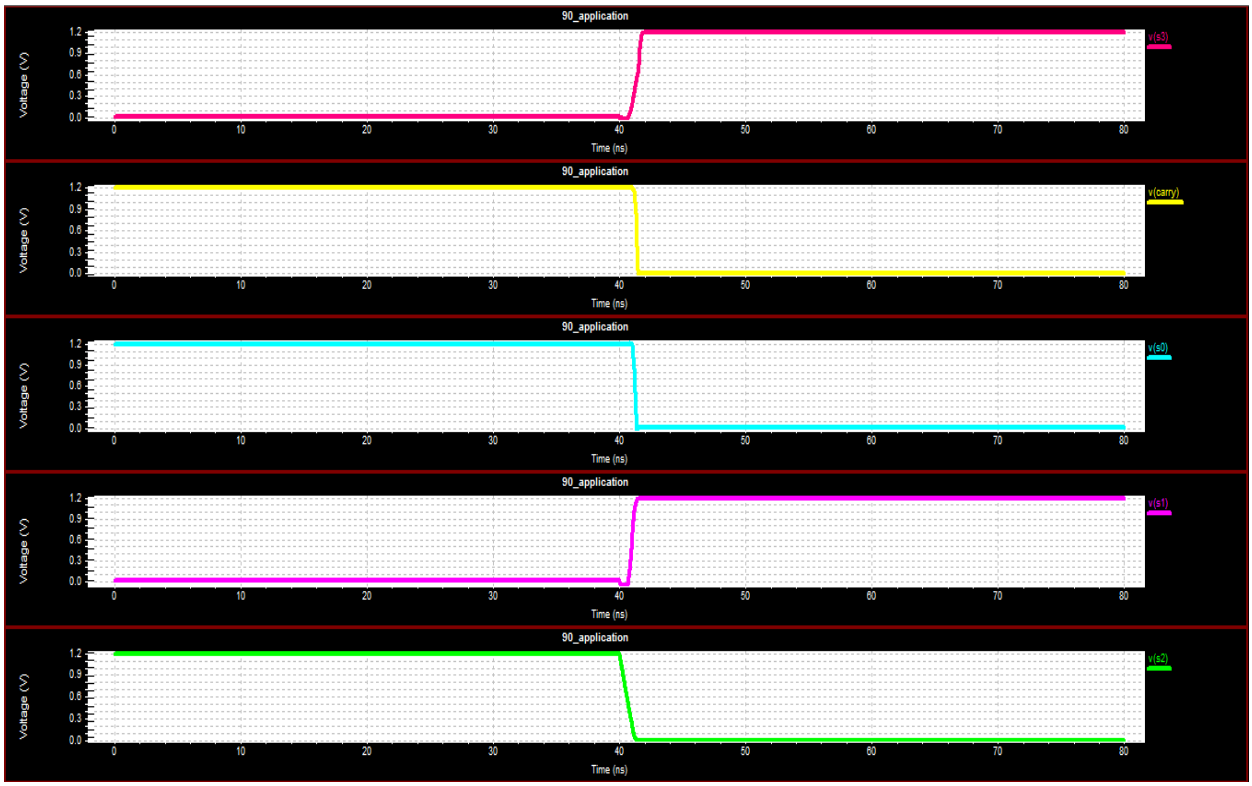

Fig.8: Waveform of proposed 4 bit Ripple Carry Adder at 90nm technology

Simulation results for the 4 bit Ripple Carry Adder is compared below.

Table 3 Results of Multiplier at various technologies

Parameters	**Multiplier Results**	
Technology	180nm	90nm
Supply Voltage	1.8 V	1.2 V
Power	3.431 uW	0.8095 uW
Delay	342.29 ps	691.71 ps
PDP	1.1745 fJ	0.559 fJ

V. CONCLUSION

The simulation was carried out using standard Tanner EDA tool with 180-nm and 90-nm technology and compared with other standard design approaches like CMOS, CPL, TFA, TGA, and other hybrid designs. The simulation results established that the proposed adder offered improved PDP compared with the earlier reports. The design simulation of 1 bit hybrid full adder is providing less delay while using less power. Further we have extended this adder to implement a 4 bit Ripple Carry Adder to utilize the above mentioned qualities of the adder.

VI. REFERENCES

[1]. C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in *Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst.*, vol. 13. Apr. 2007, pp. 1–4.

[2]. S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energyefficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[3]. N. H. E. Weste, D. Harris, and A. Banerjee, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed. Delhi, India: Pearson Education, 2006.

[4]. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Delhi, India: Pearson Education, 2003.

[5]. D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEE Proc.-Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.

[6]. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[7]. C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[8]. A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysisof low-power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[9]. M. L. Aranda, R. Báez, and O. G. Diaz, "Hybrid adders for high-speed arithmetic circuits: A comparison," in *Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE)*, Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.

[10]. C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in *Proc.IEEE Conf. Design Diagnostics Electron. Circuits Syst.*, vol. 13.Apr. 2007, pp. 1–4.

[11]. S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[12]. N. H. E. Weste, D. Harris, and A. Banerjee, *CMOS VLSI Design:A Circuits and Systems Perspective*, 3rd ed. Delhi, India: Pearson Education, 2006

[13]. J.-M. Wang, S.-C. Fang, and W.-S. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," *IEEE J. Solid-State Circuits*, vol. 29, no. 7, pp. 780–786, Jul. 1994.

[14]. P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," in *Proc. World Congr. Inf. Commun.Technol. (WICT)*, Dec. 2011, pp. 240–244.

[15]. M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design of new full adder cell using hybrid-CMOS logic style," in *Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2011, pp. 451–454.