Delay and power analysis of bundled SWCNT interconnects with variation in driver size

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***Abstract*—** In this paper, the propagation delay and power consumption for bundled SWCNT and Cu interconnects are analyzed by varying the driver size at 32nm and 22nm technology node. The variation in driver size approach is used to minimize the propagation delay and power consumption. An equivalent circuit model for bundled SWCNT interconnects is proposed to estimate the propagation delay and power consumption at global length of interconnects. A simple approximation of an *RLC* interconnect line for bundled SWCNT interconnect is obtained by using pi (π) model to achieve better accuracy for estimating propagation delay and power consumption. The propagation delay and power consumption for bundled SWCNT interconnects are analyzed, estimated and compared with Cu interconnects by running the SPICE simulations. SPICE simulation results demonstrate that the propagation delay ratio (T_{swcntb}/T_{Cu}) is lesser for smallest value of driver size and the ratio of average power consumption (P_{swcntb}/P_{Cu}) is lowest in between 800µm to 1000µm length of interconnect at both technology nodes.

Keywords*—Delay; Power Consumption; SWCNT Interconnect; π-Model; Driver.*

I. INTRODUCTION

The resistivity of copper is increasing rapidly due to the combined effect of enhanced electron-surface, grain boundary scattering, and the presence of highly resistive diffusion barrier layer in current deep-submicron technology node [1]. The steep rise in parasitic resistance of copper interconnects poses serious challenges for interconnect reliability and delay at the global level [2]. It has a significant impact on the performance and reliability of VLSI circuits and systems. In order to overcome these problems, researchers are forced to find an alternate material used for on-chip interconnects at global level. Recently, carbon nanotubes (CNTs) have been reported as a promising material for interconnects due to its long mean free path of about several micrometers, high current densities greater than 10^9 A/cm^2, and high thermal stability than copper [3]. These unique properties create a lot of interest among researchers to use the CNTs for future VLSI interconnects.

CNTs consist of the hexagonal graphene sheets rolled up of hollow cylinders. CNTs can be categorized into single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). Depending on the chirality, CNTs can be either metallic or semiconducting. The diameter of SWCNTs ranging from 1 to 5nm and length from 2 to 10nm, while the diameter of MWCNTs ranging from few to hundreds of nanometers and length of several microns. The SWCNTs consist of single shell, whereas MWCNTs consist of various concentric shells. CNTs are one-dimensional (1D) system of electrons that provide extraordinary electrical and thermal properties. Since the electrons can move in 1D and scattered only backward, therefore the scattering of nanotubes in the phase space is very limited [4]. The mean free path (mfp) of the metallic nanotubes is about of 10^3 to 10^4 nm at room temperature, whereas in three dimensional (3D) metallic copper wire, the electrons can be backward by a series of small angle scattering and the mfp is ranging of 40 nm [5-6]. Due to these extraordinary electrical, and thermal properties, CNT based interconnects play an important role to minimize the delay and improve the performance of circuits and systems in the modern era of nanoelectronics.

Kreupl *et al.* [3] demonstrated the possible implementations of CNTs in interconnect applications. In recent past, several researchers reported that an isolated SWCNT could not achieve better performance than copper interconnect due to of its higher resistance. Therefore, researchers have always focused on CNT bundles to improve the interconnect performance [3, 7]. Raychowdhury and Roy [8-9] presented a realistic *RLC* model for metallic SWCNTs and analyzed the impact of SWCNTs on the performance of ultra-scaled digital VLSI design. Based on the realistic *RLC* models, Naeemi, Sarvari, and Meindl [10-11] compared the performance of bundled SWCNT and copper interconnects for the first time. It is observed that the SWCNT bundles can have adequately large propagation speed and outperform than the copper in terms of resistance and delay. The authors also demonstrated that the performance enhancement increases as the length of interconnect increases or the feature size decreases. Later on, Srivastava and Banerjee [13] compared the performance of bundled SWCNT and copper interconnects by assuming large contact resistances. It is also observed that the SWCNTs can outperform copper in terms of resistance and can have adequately small kinetic inductance. It is also demonstrated that the performance of bundled SWCNT can outperform copper wire interconnects at global level. Later, based on physical models, Naeemi and Meindl [4] presented the distributed circuit models of SWCNTs and bundled SWCNTs that are valid for all voltages and currents. These models can be used for circuit simulations and compact modeling. Recently, Srivastava, Li, Kreupl and

Banerjee [12] reported a comprehensive and realistic evaluation of SWCNT bundle interconnects.

The variation in driver size is an important approach to minimize the propagation delay and power consumption. The propagation delay and power consumption for bundled SWCNT interconnects against conventional Cu interconnects are minimized at 32nm and 22nm technology nodes for various driver sizes. The parasitic components based on interconnect geometry and its equivalent circuit model of bundled SWCNT interconnect are described and discussed in Section II. The set up for simulation is presented in Section III. The propagation delay and power consumption for bundled SWCNT are analyzed and compared with traditional Cu interconnects by running the SPICE simulations in Section IV. Finally, conclusions are drawn in Section V.

II. EQUIVALENT CIRCUIT MODEL OF BUNDLED SWCNT INTERCONNECTS

The bundled SWCNT interconnect is assumed to be composed of hexagonally densely packed identical metallic SWCNTs. Each SWCNT is surrounded by six immediate neighbours and their centres uniformly separated by inter-CNT distance '*x*'. The schematic of bundled SWCNT, dense triangular packing of SWCNTs with Van der Waal gap '*δ*' are demonstrated in Fig. 1.(a) and (b).

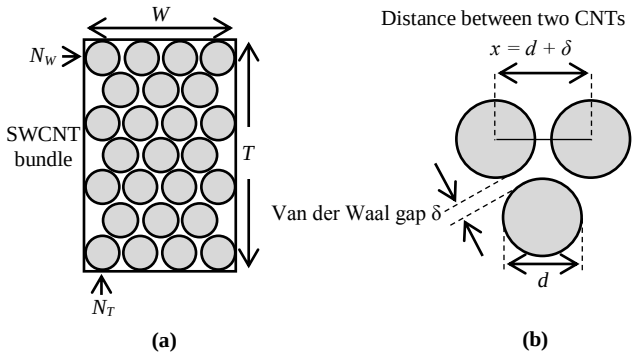

Fig. 1.(a) Schematic of bundled SWCNT interconnect [12]
(b) Dense triangular packing of SWCNTs with Van der Waal gap δ [12]

The geometrical structure of densely packed bundled SWCNT interconnect, and Cu interconnect are identical as illustrated in Fig. 1(c). In the geometrical structure, the distance between two CNTs, $x = d+\delta$, is considered, where d (=1 nm) is the diameter of SWCNT and δ (= 0.34 nm) is the Van der Waal gap between each CNT in the bundle. The two immediate adjacent wires (left and right) held at ground potential, parallel to SWCNT bundle are considered. The physical parameters such as wire width (W), spacing between adjacent CNTs (S), thickness of the bundle (T), and height from the ground plane to the SWCNT bundle (H), aspect ratio ($=T/W$), and dielectric constants are technology dependent. The spacing between the adjacent bundles is assumed to be equal to the bundle width and the thickness of the bundle is assumed to be equal to the height from the ground plane to the bundle. N_W and N_T are the number of SWCNTs along the width and thickness in the SWCNT bundle, respectively, as shown in Fig. 1(a).

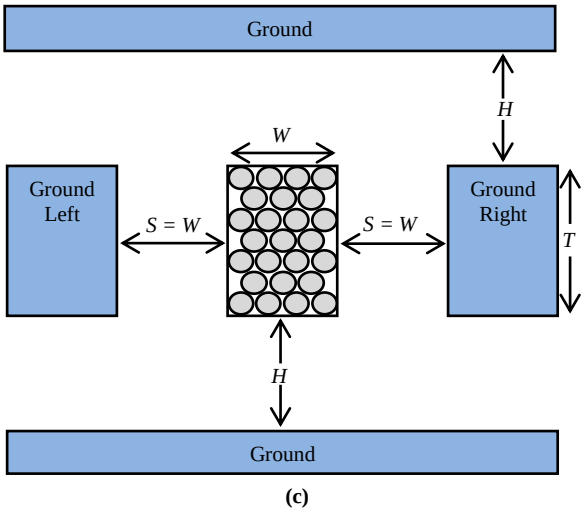

Fig. 1. (c) Equivalent geometrical structure of bundled SWCNT/Cu interconnect [12]

The total number (N_{CNT}) of SWCNTs in a bundle can be expressed as [13]:

$$N_{CNT} = N_W N_T - N_T/2, \quad for \ \ N_T \text{ is even} \quad (1)$$

$$N_{CNT} = N_W N_T - (N_T - 1)/2, \quad for \ \ N_T \text{ is odd} \quad (2)$$

where, $N_W = \text{int}\left[(W - d)/x\right]$; and

$$N_T = \text{int}\left[\frac{T - d}{(\sqrt{3}/2)x}\right] + 1$$

The equivalent circuit model of bundled SWCNT interconnect is employed for delay and power analysis as illustrated in Fig. 2 [12]. The modeling of bundled SWCNT interconnects and its parasitic resistance, inductance, and capacitance are explained below.

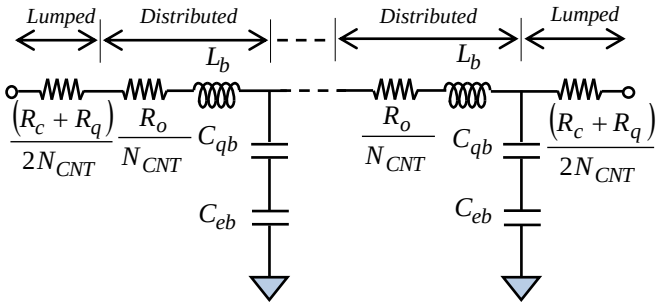

Fig. 2. Equivalent circuit model of bundled SWCNT interconnect for bundle length (l) greater than electron mean free path (λ) [12]

A. Resistance of Bundled SWCNT Interconnect

The resistance (R_b) of SWCNT bundle interconnects can be evaluated as [12]:

$$R_b = \frac{R_{CNT}}{N_{CNT}} \quad (3)$$

where R_{CNT} is the total resistance of an isolated SWCNT. It is the sum of three different types of resistances: (1) metal-nanotube contact resistant R_c; (2) fundamental quantum resistance R_q ($=h/4e^2$); and (3) ohmic resistance due to scattering (R_o) that occurs when the nanotube length (l) greater than the electron mfp (λ). The ohmic resistance is distributed resistance along SWCNT interconnect and represented in per unit length. The contact resistance is in series with the quantum resistance and equally divided between the two-end contacts considered as lumped resistance. The total resistance of isolated SWCNT can be expressed as [12]:

$$R_{CNT} = R_c + R_q \text{ for } l < \lambda \quad (4)$$

$$R_{CNT} = R_c + R_q + l.R_o \text{ for } l >> \lambda \quad (5)$$

For the perfect metal-nanotube contact, the resistance (R_c) is assumed to be very small and can be ignored for the delay and power analysis. The resistance of an isolated SWCNT is too high for implementing an interconnection [12]. Consequently, it is necessary to have a bundle of SWCNTs to lower the effective resistance and may work effectively as Nano scale VLSI interconnects.

B. Inductance of bundled SWCNT interconnect

The inductance (L_b) of bundled SWCNT interconnects of length l can be estimated as [12]:

$$L_b = \frac{L_{CNT}.l}{N_{CNT}} \quad (6)$$

where L_{CNT} is the per unit length ($p.u.l$) total inductance of an isolated SWCNT. It is the sum of $p.u.l$ kinetic inductance (L_k) and $p.u.l$ magnetic inductance (L_m) of an isolated SWCNT. The $p.u.l$ total inductance (L_{CNT}) of CNT is the sum of $p.u.l$ kinetic inductance (L_k) due to four non-interacting parallel conducting channels and $p.u.l$ magnetic inductance (L_m) of an isolated SWCNT, can be expressed as [12]:

$$L_{CNT} = L_k + L_m \quad (7)$$

$$L_k = \frac{1}{4}\left(\frac{h}{2e^2 V_F}\right) \quad (8)$$

$$L_m = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{H}{d}\right) \quad (9)$$

where h, e, and V_F are the plank's constant, electronic charge, and Fermi velocity, respectively. H, and d, are height from ground plane to the SWCNT bundle, and diameter of SWCNT, respectively.

C. Capacitance of Bundled SWCNT Interconnect

The capacitance (C_b) of bundled SWCNT interconnect of length l is the series combination of its quantum capacitance (C_{qb}) and electrostatic capacitance (C_{eb}). It can be expressed as [12-13]:

$$C_b = \frac{(C_{qb}.C_{eb})l}{(C_{qb} + C_{eb})} \quad (10)$$

Where C_{qb} and C_{eb} are $p.u.l$ quantum capacitance and $p.u.l$ electrostatic capacitance of bundled SWCNT interconnect, respectively. The $p.u.l$ quantum capacitance (C_{qb}) of SWCNT bundle is given by,

$$C_{qb} = C_q.N_{CNT} \quad (11)$$

where C_q is the total $p.u.l$ quantum capacitance due to of four parallel conducting channels of an isolated SWCNT and it can be expressed as,

$$C_q = 4C_{q-CNT} \quad (12)$$

where $C_{q\text{-}CNT}$ is the $p.u.l$ quantum capacitance of an individual isolated SWCNT and equal to $2e^2/hV_F$. Now, the $p.u.l$ electrostatic capacitance (C_{eb}) of SWCNT bundle can be expressed as [13]:

$$C_{eb} = 2.C_{en} + \frac{(N_W - 2)}{2}.C_{ef} + \frac{3.(N_T - 2)}{5}.C_{en} \quad (13)$$

where C_{en} and C_{ef} are the $p.u.l$ electrostatic capacitances calculated assuming the ground plane to be at a distance equal to separation S, and ($S+W$) from the 'near' adjacent and 'far' adjacent interconnect, respectively. These capacitances can be expressed as [13]:

$$C_{en} = \frac{2\pi\varepsilon}{\ln(S/d)} \quad (6) \quad (14)$$

$$C_{ef} = \frac{2\pi\varepsilon}{\ln\left[\frac{(S+W)}{d}\right]} \quad (15)$$

III. SIMULATION SET UP

The parasitic resistance, inductance, and capacitance for bundled SWCNT interconnect are calculated by using the geometrical parameters and (3) to (15). The geometrical parameters used in simulations are obtained from the ITRS, as summarized in Table I at 32nm and 22nm technology nodes. The copper interconnect is modeled of the same geometrical structure and same dimensions as of bundled SWCNT interconnect. The predictive technology model is used to estimate interconnect parasitic elements for copper interconnect at same technology nodes. A typical schematic of driver-SWCNT/Cu interconnect-load (DIL) set up is used for the delay and power analysis, as shown in Fig. 3. In this Fig. 3,

R_t and C_{out} are the equivalent output resistance and capacitance of the gate driver, respectively, and C_{load} is the input capacitance of the load gate. The size of the driver and the load is to be assumed 100 times more than the minimum size gate for the global interconnects. The input excitation is assumed to be a ramp signal of 1V with clock frequency of 5 MHz. SPICE simulations are also carried out for copper interconnects of the same technologies and clock frequency. The pi (π)-equivalent distributed *RLC* circuit model proposed by Kahng and Muddu [14-15] is used for distributed *RLC* network of bundled SWCNT and Cu interconnect as shown in Fig. 4. (a) and (b). A simple approximation of an *RLC* interconnect line is obtained by using π-model achieving better accuracy in estimating the propagation delay and average power consumption.

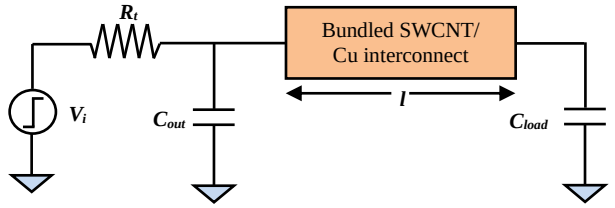

Fig. 3. Schematic of driver-bundled SWCNT/Cu Interconnect-load model [12]

Table I: Structural parameters for bundled SWCNT interconnects [17]

	Parameters	Values at 32nm node	Values at 22nm node
Global Interconnects	Width of SWCNT bundle (*W*)	48 nm	32 nm
	Spacing between adjacent SWCNT bundles (*S*)	48 nm	32 nm
	Thickness of SWCNT bundle (*T*)	144 nm	96 nm
	Height from the ground plane to the SWCNT bundle (*H*)	144 nm	96 nm
	Aspect ratio (*A/R*)	3	3
	Diameter of SWCNT (*d*)	1 nm	1 nm
Minimum size of the gate driver	R_t	13.85kΩ	16.67kΩ
	C_{out}	0.07 fF	0.049 fF
	C_{load}	0.25 fF	0.14 fF
Relative permittivity	ε_r	2.25	2.05

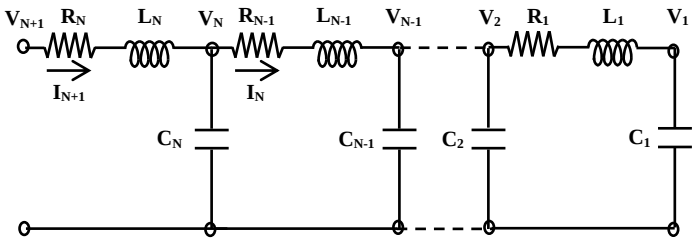

Fig. 4. (a) Distributed *RLC* interconnect line modeled from N-segment *RLC* Circuit [15]

The π-model becomes more accurate as the resistance, inductance, and capacitance of the distributed *RLC* line increases [16]. The propagation delay and average power consumption for bundled SWCNT interconnect is estimated by running the SPICE simulations and compared with the traditional copper interconnect.

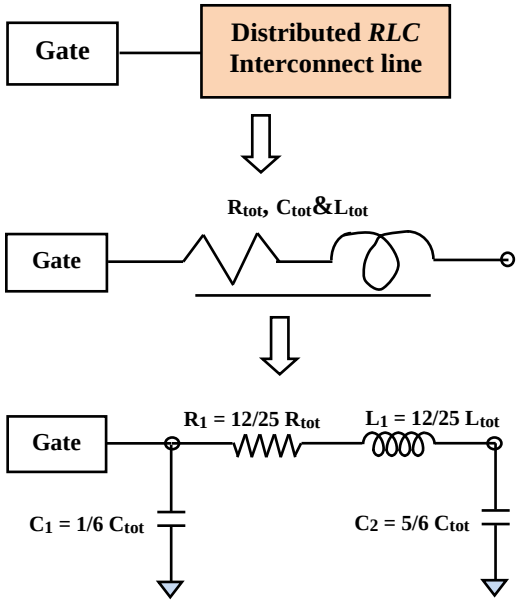

Fig. 4. (b) An open-ended *RLC* line to capture an *RLC* interconnect line, and the *RLC* π model [15]

IV. SPICE SIMULATION RESULTS

This section describes and analyzes the effect of driver size on propagation delay and power consumption for different lengths of bundled SWCNT interconnects at global level.

A. Delay Analysis

The 50 and 90 percent propagation delays for both bundled SWCNT and copper interconnect are obtained at 32nm and 22nm technology nodes by running the SPICE simulations. The length of interconnect is varied from 400μm to 1400μm which lies in global interconnect range. The delay ratio of bundled SWCNT to copper interconnects is evaluated and analyzed at both technology nodes for both cases. Figs. 5, and 6; and Figs. 7 and 8 demonstrated the delay ratio between the bundled SWCNT interconnects to the copper interconnects by varying the driver size at 32nm and 22nm technology node, respectively.

From Figs. 5, and 6; and Figs. 7, and 8, it is observed that both 50 percent, and 90 percent propagation delay ratio (T_{swcntb}/T_{Cu}), respectively, decreases with increase in length of interconnect for various driver sizes (variation in driver resistance and input capacitance of the load gate) at 32nm and 22nm technology nodes. Further, it is also observed that the propagation delay ratio increases with increase in driver size for both the cases at both technology nodes. Fig. 6 demonstrates the 90 percent propagation delay ratio which is less than the 50 percent delay ratio shown in Fig. 5, with respect to the variation of driver sizes at 32nm technology node. Moreover, it is observed that the 50 percent propagation

delay ratio shown in Fig. 7 is less than the 90 percent propagation delay ratio as in Fig. 8, at 22nm technology nodes. Due to the reduced feature size and scaled down of structural parameters of bundled SWCNT and copper interconnects, it is observed that the propagation delay ratio obtained at 22nm technology node is less than the propagation delay ratio at 32nm technology node for both cases. Therefore, the propagation delay ratio obtained at 22nm technology node is the better choice to minimize the delay for interconnects designers. Thus, it can be very well inferred that the bundled SWCNT interconnects would be more appropriate than copper to minimize the delay for global interconnects in near future.

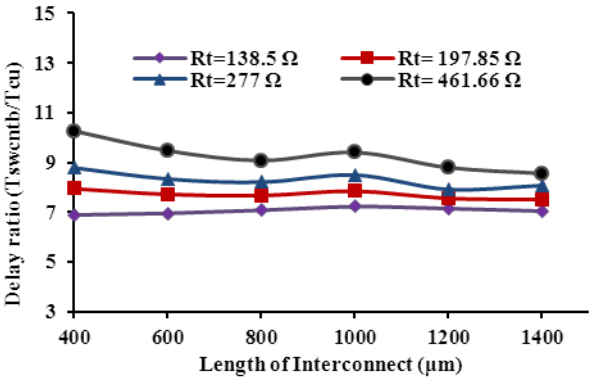

Fig. 5. Variation of 50 percent propagation delay ratio of bundled SWCNT to Cu, versus length of global interconnect with different driver sizes at 32nm technology node

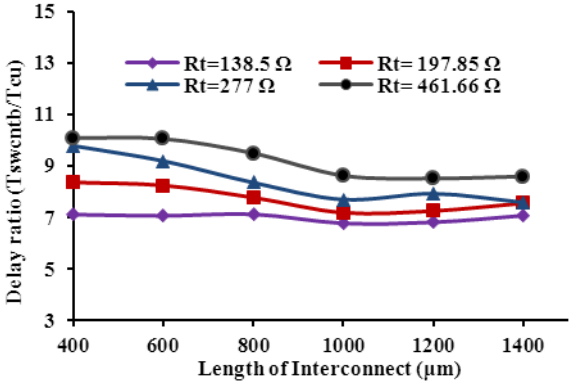

Fig. 6. Variation of 90 percent propagation delay ratio of bundled SWCNT to Cu, versus length of global interconnect with different driver sizes at 32nm technology node

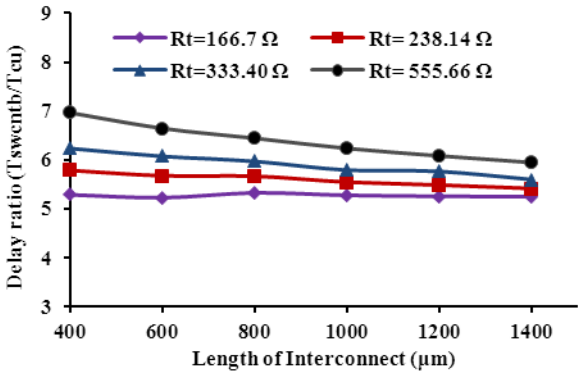

Fig. 7. Variation of 50 percent propagation delay ratio of bundled SWCNT to Cu, versus length of global interconnect with different driver sizes at 22nm technology node

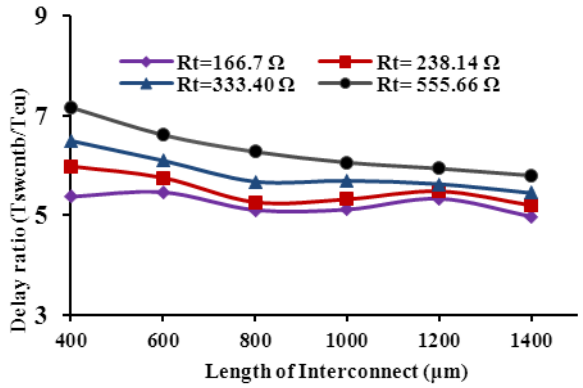

Fig. 8. Variation of 90 percent propagation delay ratio of bundled SWCNT to Cu, versus length of global interconnect with different driver sizes at 22nm technology node

B. Power Analysis

The average power consumption for both bundled SWCNT and copper wire interconnect is obtained by running the SPICE simulations at 32nm and 22nm technology nodes for the same global length of interconnect.

A ratio of bundled SWCNT and Cu interconnects; the average power consumption is evaluated and analyzed by varying the driver size at both technology nodes. This ratio of average power consumption is referred to as "relative average power consumption." From Figs. 9, and 10, it is observed that the ratio of the relative average power (P_{swcntb}/P_{Cu}) is decreasing with increase in length of interconnect, and varying the driver sizes for both technology nodes at global level. However, the ratio of relative power consumption is higher for minimum driver size and lesser for maximum driver size at both 32 and 22nm technology nodes. Thus the ratio of relative average power consumption is reducing with increasing the driver size.

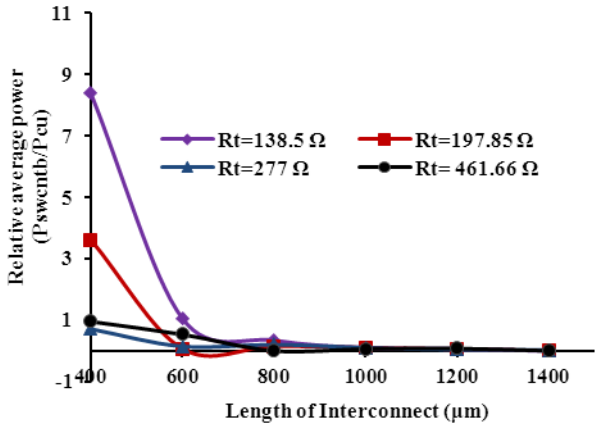

Fig. 9. Variation of relative average power consumption of bundled SWCNT to Cu versus length of global interconnects with different driver size at 32nm technology node

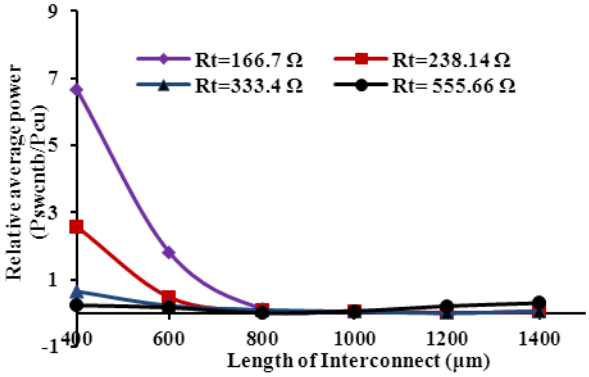

Fig. 10. Variation of relative average power consumption of bundled SWCNT to Cu versus length of global interconnects with different driver size at 22nm technology node.

V. CONCLUSION

This paper analyzed the effect of driver size on propagation delay and average power consumption for bundled SWCNT interconnects at 32nm and 22nm technology nodes. An equivalent circuit model of bundled SWCNT is chosen for the estimation and analysis of propagation delay and power consumption for global length of interconnects. The pi (π) equivalent distributed *RLC* circuit model is applied for bundled SWCNT and Cu interconnects to analyze the delay and power by varying the driver sizes. The delay ratio, and ratio of average power consumption of bundled SWCNT to Cu interconnects are obtained by running the SPICE simulations for various driver sizes at both technology nodes. It is observed that the propagation delay ratio is decreasing with increase in length of interconnect and it is minimum for smallest value of driver size for both technology nodes. Moreover, the propagation delay ratio obtained at 22nm technology node is less than the delay ratio at 32nm technology node for same length of interconnects. Furthermore, the ratio of average power consumption is decreasing with increase in length of interconnect and it is minimum between 800µm to 1000µm length of interconnect for higher value of driver size at both technology nodes. Therefore, it can be concluded that the propagation delay ratio is lesser for smallest value of driver size, and the ratio of average power consumption is lowest at 22nm technology node as compared with 32nm technology node.

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