Design of Architecture for H.264 Encoder Based Mosaicing System

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Abstract **-** A new architecture suitable for VLSI implementation has been developed for Mosaicing color pictures and effecting compression using H.264 Encoder. The architecture was coded in Verilog conforming to RTL coding guidelines. The proposed architecture is capable of processing high resolution color motion pictures of sizes of up to 1024 x 768 pixels in real time at 30 frames per second in 4:2:0 format. The compression effected is about 10 and the reconstructed picture quality is better than 32 dB.

Keywords **-** *Image/Video Mosaicing, Integer Transform, Quantization, CAVLC, Video Encoder*

I. INTRODUCTION

Image and Video Processing has been a very active field of research and development in the past years. Algorithms are essential for processes related to advanced technologies like digital television, internet streaming video and DVD video, where video compression has become an inevitable component of broadcast and entertainment media. In the last decade, many algorithms and architectures have been proposed and developed by a number of researchers for compression, image mosaicing etc. [1-7].

Currently, the video codec that achieves the highest data compression without sacrificing on the picture quality is the MPEG-4 Part 10 Advanced Video Coding, also known as the H.264 [8, 9]. This codec has many new features such as Intra-frame prediction, 4x4 Integer transform, quantization, context adaptive entropy coding, deblocking filter etc.

In an earlier work, one of the present authors has designed Integer Transform and Quantization Processor and their inverses (TQIQIT) and, Context Adaptive Variable Length Coder (CAVLC) suitable for FPGA realization of H.264 Video Encoder [5, 10]. These architectures have been used in the present work in order to realize Verilog implementation of an integrated image/video mosaicing system. The present work also uses the Design of Novel Algorithm and Architecture for Feature Based Corner Detection for Image Mosaicing, published earlier [7].

The rest of this paper is organized as follows. A new architecture for image/video mosaicing system based on H.264 video encoder is presented in Section 2. deals with the architecture of the proposed schemes for evaluating the transform and quantization suitable for high speed implementation on FPGA/ASIC. Results are presented in Section 3, followed by Conclusion.

II. PROPOSED ARCHITECTURE FOR VIDEO/IMAGE MOSAICING SYSTEM USING H.264 ENCODER

This section presents the overall building blocks of H.264 Encoder based Color Image/Video Mosaicing system. The basic architecture for Mosaicing and compressing of an image or a video sequence is shown in Figure 1. As shown therein, the Mosaicing System comprises a Mosaicing Processor, an RGB to YCbCr Color Format Converter and a H.264 Video Encoder to compress the mosaiced image or a video sequence. This architecture mosaics two still or video pictures that are fed pixel by pixel at the inputs of the mosaicing system. These inputs in RGB format are fed to the 3x3 pixels Sliding Window in a raster scan manner. The output pixel values from 3x3 Sliding Window are subsequently sent to 3x3 Convolution Modules for convolving the gradients of each pixel using pipelined architecture with FIFO module.

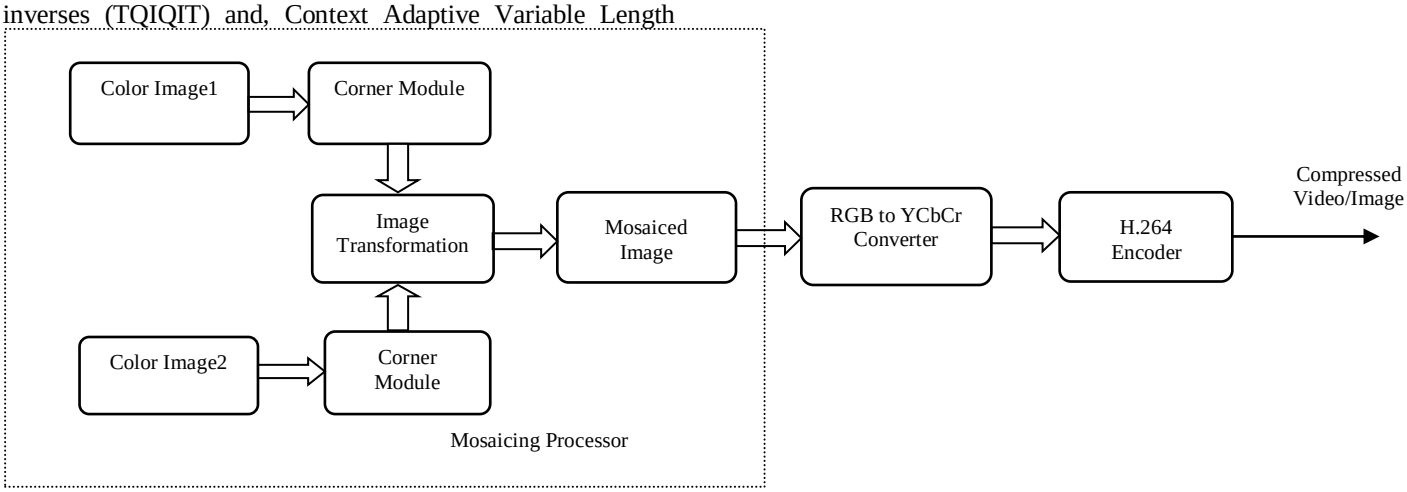

Fig.1: Basic Architecture of Image/Video Mosaicing System Using H.264 Encoder

The convolved derivatives are input to the next Mosaicing module in order to compute the corner values for each of the two pictures being mosaiced. The mosaiced picture output is in the RGB format. Since the H.264 encoder needs the data to be in the YCbCr format, an RGB to YCbCr Converter has also been designed in the present work. These individual processors are described at length in the following sub sections.

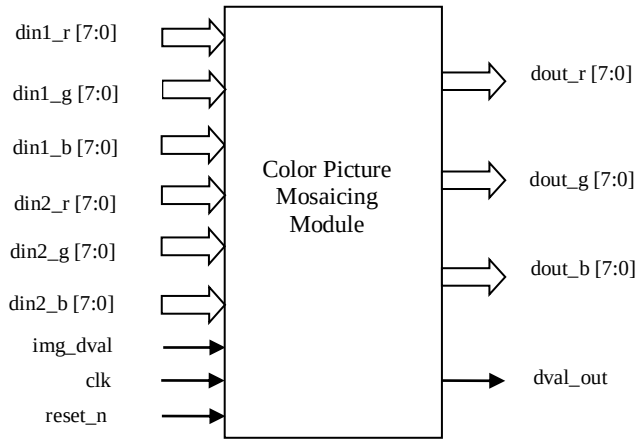

Fig.2: Architecture of Top Design Color Picture Mosaicing System

A. Architecture for Feature Based Image/Video Mosaicing System

This section presents the architecture of the feature based image mosaicing system presented in a previous paper by the present authors [7]. The architecture consists of several components such as Color and Gray Image modules, 3x3 Convolution modules, Corner modules, Image Transformation module and Image Blending module. The detailed algorithm and architecture for Sliding Window Based Image Mosaicing has been explained in the reference paper [7].

The architecture of the Top Design Color Pictur Mosaicing System is shown in Figure 2 and the signals used i this module are presented in Table 1. The architecture fc Sliding Window Based Corner Detection Processor uses number of pipelining stages and parallel processing in th design in order to increase the processing speed. Thi architecture mosaics two pictures which are fed pixel by pixel at input pins marked "din1" and "din2". The input pixels are valid at the positive edge of the "clk". The input pictures' data validity are indicated by asserting the "img_dval" signal. The color components from the two pictures being mosaiced are integrated and output as "dout_r", "dout_g" and "dout_b", each of 8 bits size. The mosaiced picture data ("dout_r", "dout_g", "dout_b") in RGB format is valid when "dval_out" signal is asserted.

Table 1 Signal Description for Color Picture Mosaicing System

Signals	Input/Output	Description
clk	Input	Clock Signal
reset_n	Input	Active low System reset
img_dval	Input	Input Data Valid Signal
din1_r [7:0]	Input	Picture 1 'R' color data
din1_g [7:0]	Input	Picture 1 'G' color data
din1_b [7:0]	Input	Picture 1 'B' color data
din2_r [7:0]	Input	Picture 2 'R' color data
din2_g [7:0]	Input	Picture 2'G' color data
din2_b [7:0]	Input	Picture 2 'B' color data
dout_r [7:0]	Output	'R' component of Mosaiced Picture
dout_g [7:0]	Output	'G' component of Mosaiced Picture
dout_b [7:0]	Output	'B' component of Mosaiced Picture
dval_out	Output	Output Data Valid Signal

B. RGB to YCbCr Format Converter

The image/video sequence from the Mosaicing Processor is input to the format converter, which converts the RGB format Red (R), Green (G) and Blue (B) components of a color Mosaic Picture to the standard 4:2:0 format luminance (Y) and chrominance (Cb, Cr) components.

In 4:2:0 format, each of the number of chrominance components are exactly half of the number of luminance components. The architecture for the format converter is shown in Figure 3. The mosaiced data "dout_r", "dout_g" and "dout_b" are input to the format converter when "dval_out" signal is asserted. The format converted outputs are available at Y, Cb and Cr and are valid if "dout_valid" signal is asserted.

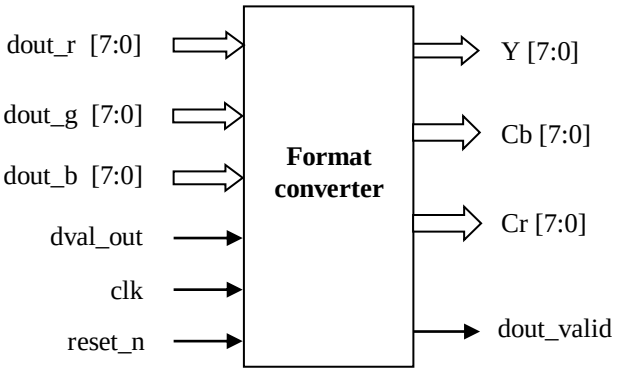

Fig.3: Architecture of Format Converter

C. Architecture of H.264 Video Encoder

The basic architecture of H.264 Advanced Video Encoder (AVC) is presented in Figure 4. As shown in the figure, it comprises an Intraprediction module, an integer transform and quantization (TQ) and their inverse (IQIT) modules and a Context Adaptive Variable Length Coder (CAVLC) [5, 10].

The Y, Cb, Cr components from the Format Converter module are input to the Intra-prediction module, transformed, quantized, inverse quantized and inverse transformed so as to get the reconstructed picture which is fed back to the Intra-prediction module. Horizontal mode of intraprediction has been

used in the Verilog realization [5]. The quantized coefficients are then input to the Context Adaptive Variable Length Coder (CAVLC) module [10], which generates variable length codes to get the required compressed bit stream.

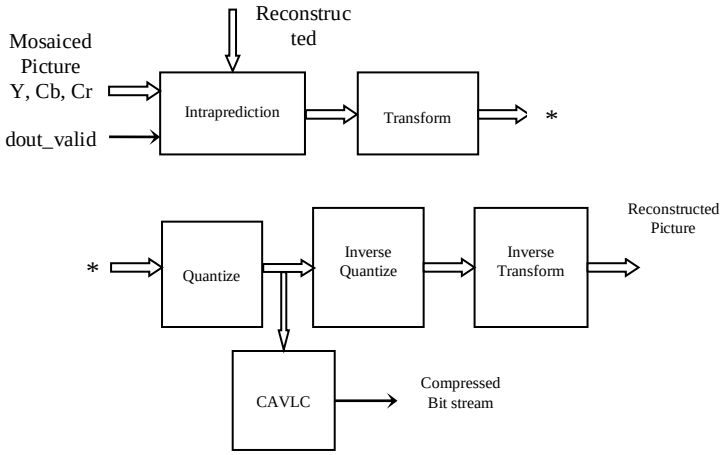

Fig.4: H.264 Advanced Video Encoder

III. SIMULATION AND PLACE & ROUTE RESULTS

The proposed H.264 Encoder based Mosaicing system, whose architecture was presented in the previous section, has been coded and tested in Matlab first in order to ensure the accurate functioning of the algorithm. Subsequently, the complete system has been coded in RTL compliant Verilog. The simulation of the proposed method has been done using ModelSim and synthesized using Xilinx ISE 13.2.

The Verilog design of feature based image mosaicing, whose architecture was presented in Ref. [7] was integrated with the RTL design of Intra Prediction, Integer Transformation, Quantization, Inverse Quantization, Inverse Transformation [5] and Context Adaptive Variable Length Coder [10] in order to design a Mosaicing system than can also bring about compression for effective serial transmission of high resolution motion pictures. The integrated design has been functionally verified using Modelsim. The H.264 encoder based mosaicing system was first implemented in Matlab in order to estimate the quality of the reconstructed image and the compression that can be achieved. In addition, Matlab output serves as a reference for verifying the Verilog output. The simulation results for a sample image Lena is presented in Fig. 5. The reconstructed image quality is better than 37 dB for a compression of about 9 and better than 32 dB for a compression of about 11 using 4:2:0 format. The designed architecture is capable of processing high resolution color motion pictures of sizes of up to 1024 x 768 pixels at 30 F/s in 4:2:0 format.

The Place & Route has been run using Xilinx ISE 13.2. The core parts of the Mosaicing system described in previous sections utilize more than 2.8 Million gates. The maximum frequency of operation is about 100 MHz.

a b c

Fig.5: Simulation Results of Color Mosaicing System Using H.264 Video Encoder
a Original Lena Image (512 x 256 pixels)
b Reconstructed Lena Image using Matlab, PSNR: 37.1 dB (Q step =8)
c Reconstructed Lena Image using Verilog, PSNR: 37.3 dB (Q step =8)
Compression effected: 9.3

IV. CONCLUSION

Using a H.264 Encoder, a new architecture suitable for VLSI implementation has been designed for compressing high resolution color image mosaics. The design is also capable of processing video sequences. The architecture comprises a sliding window based corner detection mosaicing module; an integer transformation and quantization and their inverse modules using horizontal mode of intra prediction and; a context adaptive variable length coder. These architectures were designed and coded in RTL compliant Verilog. The proposed architecture is capable of processing high resolution color pictures of sizes of up to 1024 x 768 pixels in real time in 4:2:0 format. The reconstructed picture quality is close to the original picture.

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