A Hybrid Low Noise Power Amplifier (LNPA) with Parallel Feedback for Fast Generation Technology

L.Amarender Reddy [1,] Dr.K.Manjunathachari [2]
[12]Department of Electronics and Communications Engineering
[1]Research Scholor, JJT University, Jhunjhunu, Rajasthan, India
[2]Gitam School of Technology, Gitam University, Patancheru, Hyderabad –Telangana, India

Abstract- A wideband noise-cancelling low-noise amplifier (LNA) without the use of inductors is designed for low-voltage and low-power applications. Low Noise amplifier have important feature like amplify the signal with rejection of noise. Low noise amplifier in modern communication used as filter with amplifier. In present days low noise amplifier the also reduces the reflection of signal exist by elements and connecting interface inside the amplifier. The aim of this paper is to propose a hybrid low noise power amplifier with CMOS architecture for the lower power consumption in memory devices, improving the speed for the fast generation. The proposed amplifier is integrated with 65nm CMOS technology to achieve high output power and high efficiency.

Keywords- 65nm CMOS Technology, Hybrid Low Noise Amplifier, Cross coupled inverter, LNA

I. INTRODUCTION

A low noise amplifier is the first block of receiver also it is key building block in analog circuit design. Now a day's CMOS become a very fast growing technology for a radio transreceiver implementation of various wireless communication system due to technology scaling. In RF front end is easy to integration with digital blocks by using CMOS whole system on single chip [1]. The challenge of building a single RF front-end capable of receiving and processing a multiplicity of bands (e.g., for a software-defined radio) has stimulated interest in broadband RFIC design. This has arisen in response to the potential complexity, cost and power consumption of portable wireless devices designed to incorporate new wireless standards and applications, while maintaining backward compatibility with existing standards and capabilities. Required for a multiband/multistandard RF front-end, UWB radio or perhaps both (e.g., a multiband/ multistandard receiver with UWB capability). Reducing the number of LNAs by reducing the number of RF receive paths could drastically reduce power consumption, chip size, and cost in a multiband/multistandard radio[2]. However, at present it is unclear how multiple antennas and preselect filter paths can best be multiplexed efficiently to a single LNA input.

Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology, which can get the similar low noise amplifier performance with very low power consumption. The fast-evolving scaled CMOS technologies demonstrate excellent performance including high frequency and low noise figure , providing a good margin for the design of high-performance LNAs with low cost [3]. However, traditional LNAs with on-chip inductors occupy a large area which counters the benefit brought by the scaled digital CMOS. Furthermore, although inductors resonant with parasitic capacitors lead to higher gain and better NF, the lack of accurate inductor modeling complicates the circuit design, resulting in possible trial-and-error tape-outs. Off-chip inductors have higher Q values than on-chip inductors. However, they increase the cost and reduce the yield. Thus, employing an inductorless LNA becomes an attractive choice for many low-cost applications[4].

Recently, RF-CMOS processes have become more and more popular for RFICs design because it is cost-effective and compatible with the silicon-based system on chip technology. In Ultra-Wideband receiver front end design, ultra wideband Low Noise Amplifier is a critical block that receives small signal from the whole UWB Band (3.0-10.6GHz) and amplifies it with a good signal-to-noise ratio. A Low Noise Amplifier should accommodate large signals without distortion, and frequently must also present specific impedance, such as 50Ω, to the input source. In additional, high and flat power gain, input and output impedance matching and good noise figure performances across the whole UWB band are required [5].

II. LITERATURE SURVEY

In [6], a concurrent dual-band low noise amplifier (0.35 mm CMOS) is presented. Here, series and parallel LC networks are utilized to achieve narrowband gain of 14 dB and 15.5 dB at 2.45 and 5.25 GHz respectively with just 10 mW power consumption. The NF for 2.45 GHz band is acceptable (2.3 dB) but is quite high for 5.25 GHz band (4.5 dB). One major drawback of this design is that its gain, NF and linearity cannot be further improved because the single input matching network cannot be optimized for both bands.

In [7], a 1.8/2.4 GHz dual-band concurrent LNA (0.18 mm CMOS) is presented. In this paper, a particle swarm based optimization technique (PSO) is employed for the selection and optimization of output matching network while switched capacitors are used for input matching. The simulation results show a good NF (≤2.4 dB), extremely low gain (≤9 dB) and 18 mW of power consumption.

In [8], a low voltage CMOS based 2.45/5.25 GHz LNA (0.18 mm SiGe BiCMOS) is presented. Dual band operation is possible by tuning two series LC loads each at the band of interest. This design provides two separate outputs for each desired band. However, it compromises Si area because of the use of the six inductors. A 2.4– 5.4 GHz LNA (0.13 mm CMOS), performs continuous frequency tuning by combination of switched inductors and varactors.

A Low Noise Amplifier with integrated notch filter is demonstrated by D. Bormann [9]. The authors used a coil less two - stages low noise amplifier with capacitive feedback with implementation of Q - enhanced notch filter. The circuit can be used in FDD system such as UMTS or WCDMA without additional off chip interstate filter. Since gain is not the main parameter for low noise amplifier, authors used shunt – shunt feedback which decreases the gain but increase the stability and linearity. In addition, the input impedance implemented feedback capacitor and load capacitance which turned the input impedance from the purely capacitive into less capacitive and more resistive impedance.

C. Lu, et al., [10] designed a 20 GHz low noise amplifier with notch filtering which filter the frequency band from 27.5 GHz to 31 GHz by using 0.25μm SiGe: CBiCMOS technology. Authors decided to implement the notch filter at different stages in order to have minor impact on the noise figure while gaining high rejection around 30 GHz. The authors use two-stage single ended filtering which consists of cascode stage. A design of UWB LNA based on simple resistive shunt feedback technique is presented by X. Guan (2011) [11]. The design is claimed to perform well over the entire UWB band which is from 3.1 - 10.6 GHz. The design of LNA consist of two stage where the first stage has two transistor connected in cascode with a resistive shunt feedback and contain loading element in formed by the resistor parallel with the inductor. The loading element is important because the input impedance also depends on it. Authors stated that the simplicity if the design make possible low power consumption, low noise figure, high linearity.

III. RESEARCH METHODOLOGY

A hybrid low noise power amplifier is proposed which consists of bidirectional amplifier with parallel feedback and complementary current-reuse circuit in order to reduce overall dc current consumption. The cross coupled inverter model is using here as low noise power amplifier.

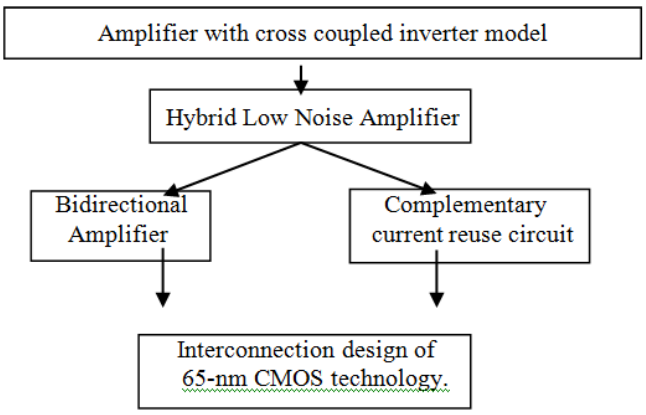

Fig.1: Proposed System Architecture

A. Cross coupled inverter model

Sense amplifier which detects the voltage difference on the bit lines is called voltage mode sense amplifier. There are some voltage mode sense amplifiers like single ended sense amplifiers, differential amplifiers and Cross coupled sense amplifiers.

Fig.2 shows the schematic of Cross-coupled voltage mode SA. M1 and M2 are the access transistors, whereas M3- M6 forms cross-coupled inverters. When SAEN is low, M1 and M2 are turned ON and voltage on BL and BLB will be transferred to SL and SLB respectively. Due to positive feedback, higher voltage level goes to VDD and other level goes towards zero.

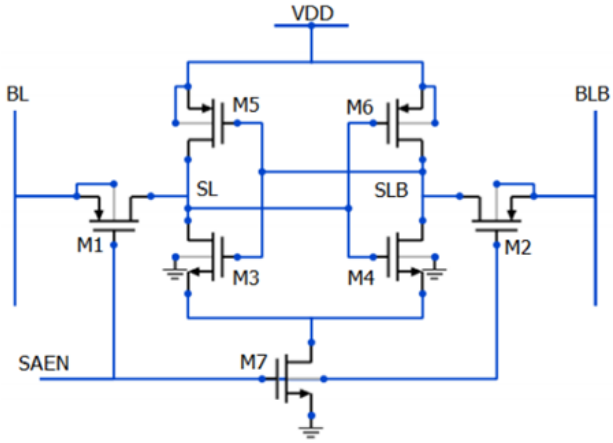

Fig.2: Cross Coupled inverter model

B. Hybrid Low Noise Amplifier

This amplifier reuses the drain current to bias two transistors and feeding of signal is from one stage to other stage of the resonance path. In the current reused differential pair the input voltage is coupled to the gate and source terminals of the transistors through the coupling capacitors.

Fig.3 explains that currents I_{D1} and I_{D2} can be reused as current I_D; there is just one current path between drain voltage V_{dd} and ground. In the experimental current-reuse LNA, the

amplifier topology has been transformed from a two-stage common source structure without changing the essential amplifier type, resulting in high gain without adding power consumption.

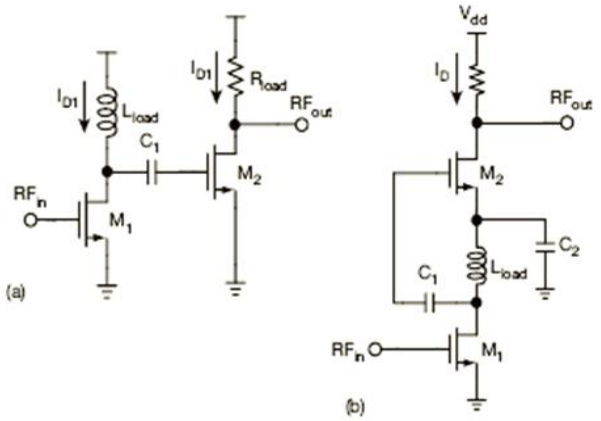

Fig.3: Bidirectional amplifier with current reuse circuit

C. Integration Process

The 65nm is starting to be considered as a new attractive solution in view of the development of high-density, high-performance, mixed-signal readout circuits. Total Power dissipated in a CMOS circuit is sum total of dynamic power, short circuit power and static or leakage power. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product. In the sections to follow we summarize the most widely used circuit techniques to reduce each of these components of power in a standard CMOS design.

S.No	Parameter	Value
1	VDD (V)	0.8-1.2 V
2	I_{OFF} N (N_a/µm)	5-100
3	I_{OFF} P (N_a/µm)	5-100
4	Gate dielectric	SiON
5	No of metal layers	8-10

Table 3.1: Key Features of 65 nm Technology

IV. PERFORMANCE ANALYSIS

A. Power Gain

In general gain is a ratio between the output signal and input signal. It shows how much the signal is amplified. LNA is required to achieve a high power gain in order to reduce the effect of noise introduced by the subsequent stages at the receiver front end. Value of the gain should be high. When relation between input-output is linear then it is called as linear gain. However all RF& IF circuits are inherently nonlinear.

B. Noise Figure (NF)

NF is a measure of degradation of the SNR, caused by components in the RF chain. Mathematically, NF is defined as the ratio of the input SNR to the output SNR of the system. NF may be defined for each block as well as the entire receiver [2]. Generally it is not possible to obtain minimum noise figure and maximum gain for an amplifier.

Parameters	Existing Design	Proposed Design
Technology used	130nm CMOS technology	65nm CMOS technology
Input voltage	Vin= 0.5V,	Vin=0.34V,
Output voltage	Vout=0.75V	Vout=0.43V
VDD Supply	2.5 Volt	0.8-1.2 Volt
Power	20.028dBm	20.09dBm
Efficiency	44.669%	81.90%

Table 4.1: Comparison of proposed work with existing design

V. CONCLUSION

The feasibility of a newly proposed hybrid low noise amplifier with cross coupled amplifier for improving noise performance, achieving good input matching and high power gain has been demonstrated in this paper. As 65 nm CMOS technology increases the switching speed of device which is mainly due to significantly reduced interconnection length therefore high output power with high efficiency is obtained using CMOS device for the power amplifier. As shown in the results this power amplifier dissipates low amount of power which is due to gate width is reduced and therefore is responsible for high efficiency. Efficiency can be increased or decreased depending on the power requirement.

VI. REFERENCES

[1]. A. A. Abidi, "RF CMOS comes of age," IEEE J. Solid – State Circuits, vol.39, pp. 549–561, April 2004

[2]. I.S.-C. Lu, N. Weste, S. Parameswaran, "A digital ultra-wideband multiband transceiver architecture with fast frequency hopping capabilities", in Proc. IEEE Conference on Ultra Wideband Systems and Technologies Conference, Piscataway, NJ, USA, 2003, pp. 448 – 452.

[3]. Y. Lu, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, Zh. Lu, "A novel CMOS low-noise amplifier design for 3.1- to 10.6-GHz ultra-wide-band wireless receivers", IEEE Trans. on Circuits and Systems—I:, vol.53, no.8, pp. 1683–1692, August 2006

[4]. Choong-Yul Cha and Sang-Gug Lee, "A 5.2-GHz LNA in 0.35um CMOS utilizing inter-stage series resonance and

optimizing the substrate resistance," IEEE Journal of Solid-State Circuits, Vol. 38, No. 4, pp. 669-672, April 2003.

[5]. J. Yavand Hasani, M. kamarei, and F Ndagijimana, "Analytic input matching for millimeter wave LNA in 90nm CMOS technology," IEICE Electronics Express, Vol. 4, No. 15, pp. 472-477, Aug. 2007.

[6]. H. Hashemi, A. Hajimiri, Concurrent dual-band CMOS low noise amplifiers and receiver architectures, IEEE Symposium on VLSI Circuits, Digest of Technical Papers, 2001, pp. 247–250.

[7]. K. Datta, R. Datta A. Dutta and T.K. Bhattacharyya,PSO-based output matching network for concurrent dual-band LNA, International Conference on Microwave and Millimeter Wave Technology (ICMMT), May 2010, pp. 1440– 1443.

[8]. S. Hyvonen, K. Bhatia, and E. Rosenbaum,An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply, IEEE Radio Frequency Integrated Circuits Symposium, Digest of Papers, 2005, pp. 43–46.

[9]. D. Bormann, T. D. Werth, C. Schmits, S. Heinen. 2009. A 1.3V, 65nm CMOS, Coilless Combined Feedback LNA with Integrated Single Coil Notch Filter. 2009 IEEE Radio Frequency Integrated Circuits Symposium.

[10]. C. Lu, M. Kammerer, R. Mahmoudi, P. G. M. Baltus. 2014. A 20GHz 1.9 dB NF LNA with Distributed Notch Filtering for VSAT Application. Microwave Symposium (IMS), 2014 IEEE MTT-S International. pp. 1-4.

[11]. X. Guan, C. Huynh, C. Nguyen. 2011. Design of a 0.18-μm CMOS Resistive Shunt Feedback Low- Noise Amplifier for 3.1 -10.6 GHz UWB Receivers. Infrared, Millimeter and Terahertz Waves (IRMMWTHz), 2011 36th International Conference. pp. 1-2.