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Research Article

Design of carry select adder using 8T-full adder and 4T-multiplexer

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Abstract

Design of carry select adder using 8T-full adders and 4T-multiplexers are proposed in the present work. These circuits are designed to have low power and reduced transistor size compared to regular circuits. Each one of the proposed designs has its advantages of area and power consumption. CSLA is the most suitable among conventional adder's structures because it performs fast addition operation at low cost. The proposed CSLA has reduced transistor count and has lesser power consumption as well as compared to regular CSLA and modified CSLA. The present was also study proposed the area and power utilization of modified circuits. Simulations are done in tanner tool 180 nm technology.

Keywords: CSLA; RCA; Full adder; Multiplexer; XOR gates; Low power.

Introduction

The primary aim of fastest growing technologies is to speed up the devices. But increasing the speed solely doesn't serve the purpose; the size of devices is also a matter of concern that is to be reduced to an optimum level for mobility issues. Another major problem is power; we cannot expend more and more power from a single device demonstrating mobility as the balance between the processor and power supply needs to be managed with utmost care [1, 2]. So, if we summarize the main problems that a design engineer faces from time to time are the management between: Delay, Area and Power Consumptions. The demand of Very Large-Scale Integration (VLSI) is booming. In any device capable of bringing about computation (simple and complex) Arithmetic Logic Unit (ALU) and Floating-Point Unit (FPU) happens to be the main brain. ALU is responsible for all the logical computations such as addition, subtraction, multiplication, division and logical operations.

Most of the fundamental adders are used for arithmetic operation with microprocessors, signal processing functions and different IC's, hence binary adders are the built-in blocks of VLSI circuits. Ripple carry adder (RCA) take a longer time to propagate the carry from first stage to the second stage and goes on [3]. So this adder will introduce the overall delay in the circuits. To avoid this error carry select adder came into the role and solves this delay problem up to some extent. Whereas, the carry look-ahead adder has fast speed but it consumes more area.

CSLA [4] clarifies the problems as generated by the RCA and Carry look ahead adder [5]. Then CSLA could be designed by using single RCA and add one circuit relative than using dual RCA [2]. Area and utilization of power requirements are depend on the modified adder structures have been determined. A Multiplexer based circuit prospective to reduce the area with fewer complexes [6]. This acts as the sum for each bit point in an adder which is propagated serially. Later the preceding bit point of sum and carry propagated to the next point. Initial idea of this study is to reduce the transistor counts and consuming the area and power utilization.

Proposed method

Full adder

Generally, full adders are designed by using XOR gates. The primary power utilization in full adder is XOR gates. So the power utilization for a full adder can be decreased by minimizing the power utilization of XOR gates. The proposed design has 3T XOR circuit [7, 8]. Fig. 1 and a modified full adder circuit [9] is obtained by two simultaneous 3T XOR gates shown in Fig. 2 are

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the essential blocks in designing RCA and CSLA.

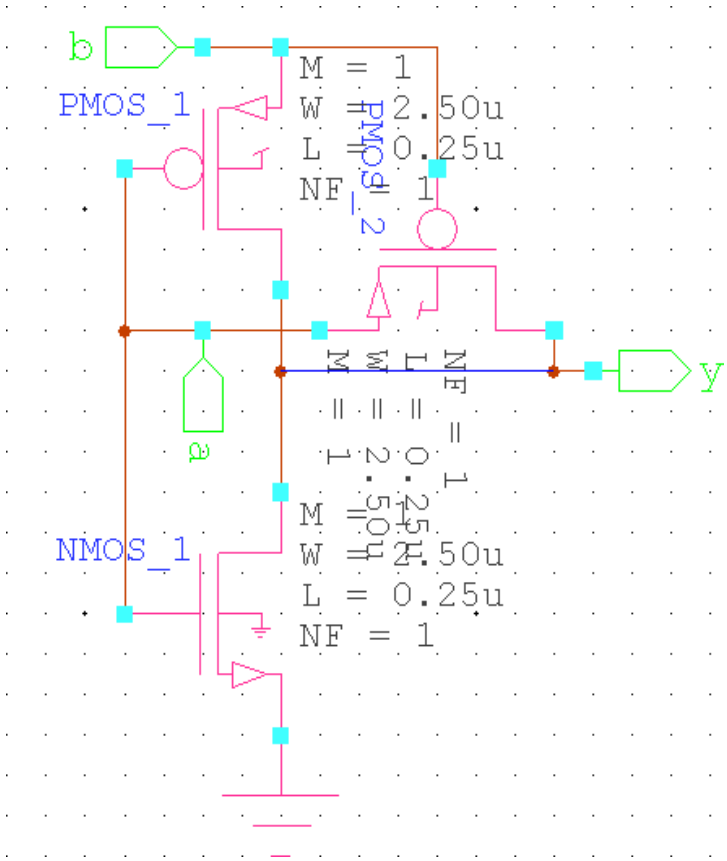

Fig. 1. Xor circuit

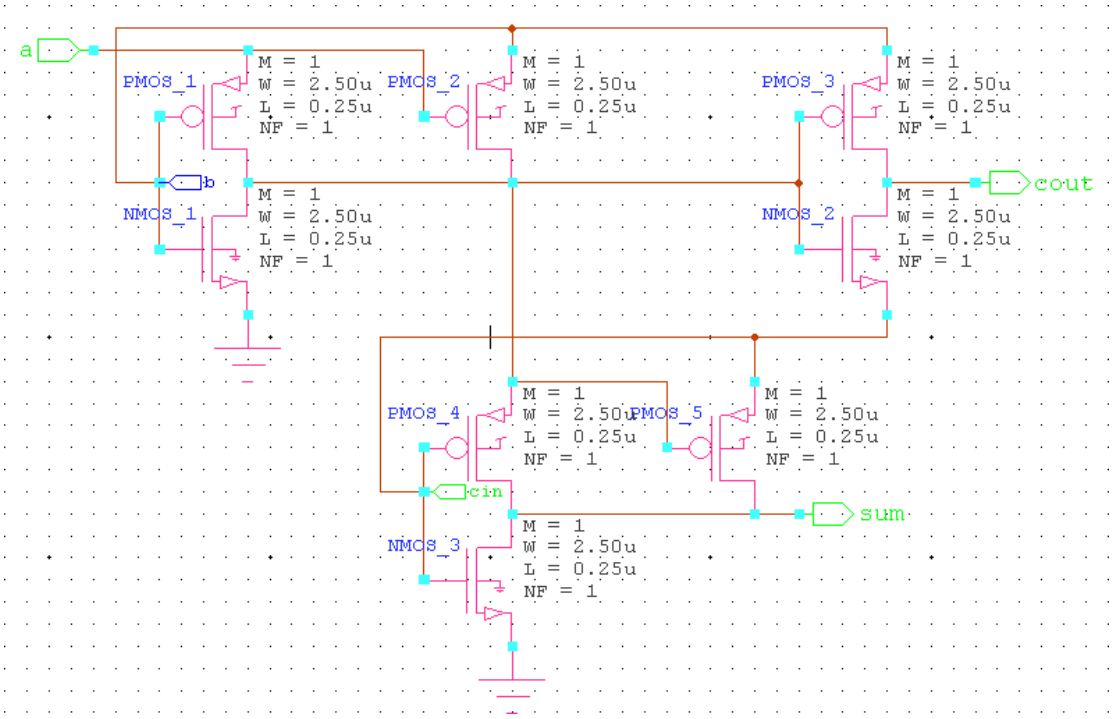

Fig. 2. Full Adder

Multiplexer

Generally, Multiplexers are used to transmit data by selectively to the receiver. By using the Complementary Pass Transistor logic gates Multiplexers (2x1)[6] size has been reduced to 4 transistor counts are compared to regular designs Fig. 3.

Carry select adder

From the Modified XOR, FA and RCA designs, a carry select adder circuit is designed. Fig. 4

shows the CSLA. Each full adder uses the modified XOR or simultaneous XOR circuits and a 2 to 1 multiplexer structure. This MUX uses complementary pass transistor logic gates and has four transistors. This MUX circuit does not have static and short circuit power consumption. The two n bit numbers are added by carry-select adder. A four bit of carry-select adder showed in Fig 4. Four full adders are composed of 2 four bit of ripple carry adder. One ripple-carry adder uses a carry-in value of 0 while the other uses a carry-in value of 1. Each ripple carry adder produce sum and carry-out values and the actual carry-in value is used to select between the outputs generated by each ripple-carry adder. This reduces the problem of carry propagation delay in the ripple-carry adder and is more efficient than ripple-carry adders at adding larger (higher bit-width) values of A and B.

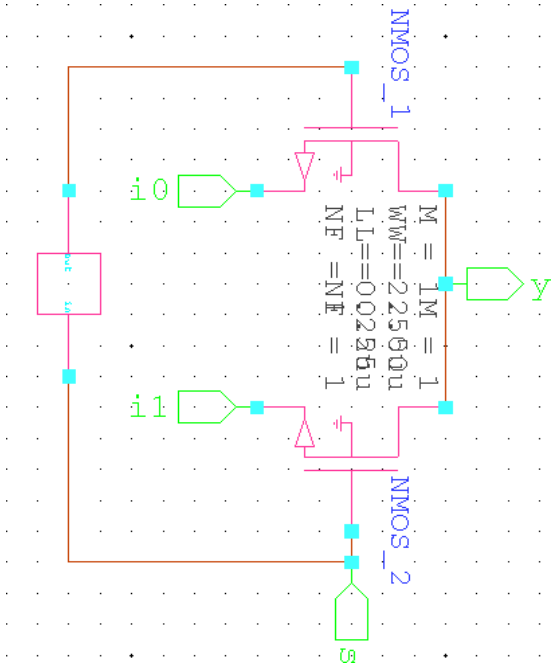

Fig. 3. Multiplexer

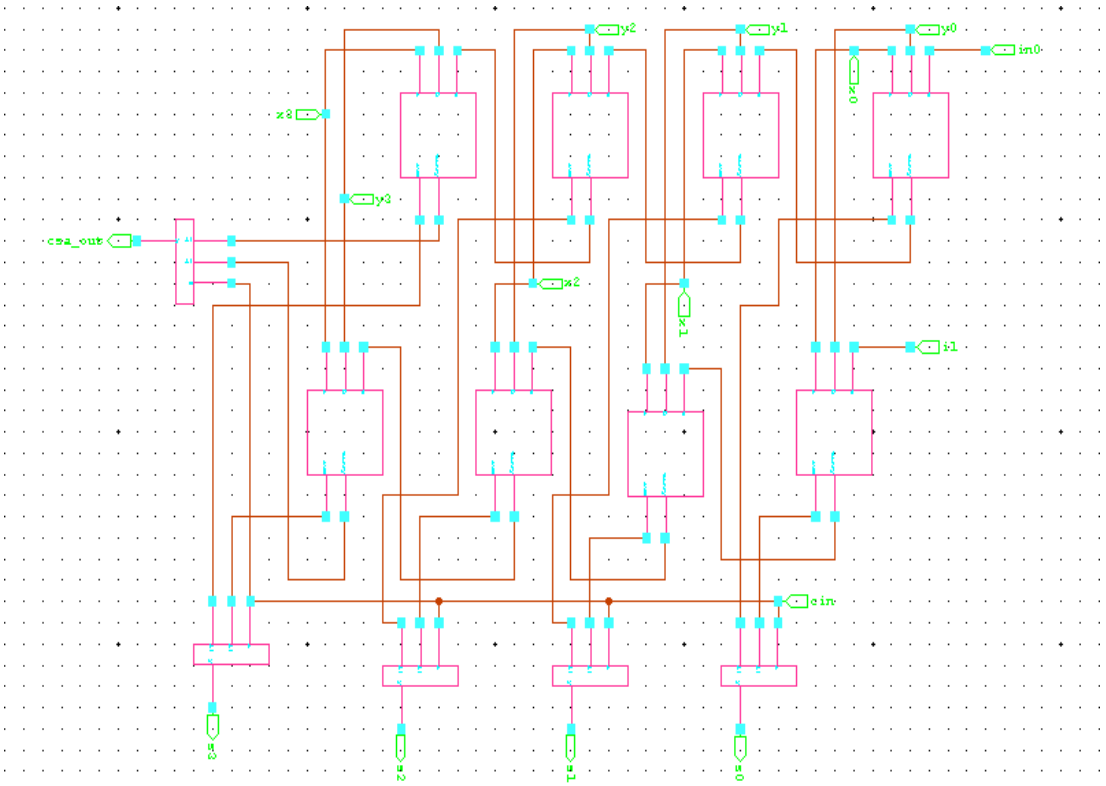

Fig. 4. Carry select adder

Result and discussion

All simulations are done in the Tanner tool in 180 nm technology. The power supply used for simulations is 5v. Fig. 5 shows the simulation waveform of CSA and table 1 shows the simulation results of the proposed CSA. Modified CSA has a minimum area and power utilization. The Modified CSA has 84 transistors compared to normal CSA has 314 transistors. So hence the area has been reduced and power utilization has been tested for 5v for all modified circuits and result in table 1. Further development in terms of design instead of using dual RCA in CSA using single row RCA and add one circuit and It would be interesting to test the design for the different n-bit CSA.

Table 1. Simulation results of Modified CSA circuit

Circuit	Area	Power (Ew)	Time Taken (S)
XOR	3	6.038	5.9
2-1 MUX	4	4.498	5.1
FA	8	4.504	6.2
RCA	32	2.303	5.9
CSA	84	2.328	6.2

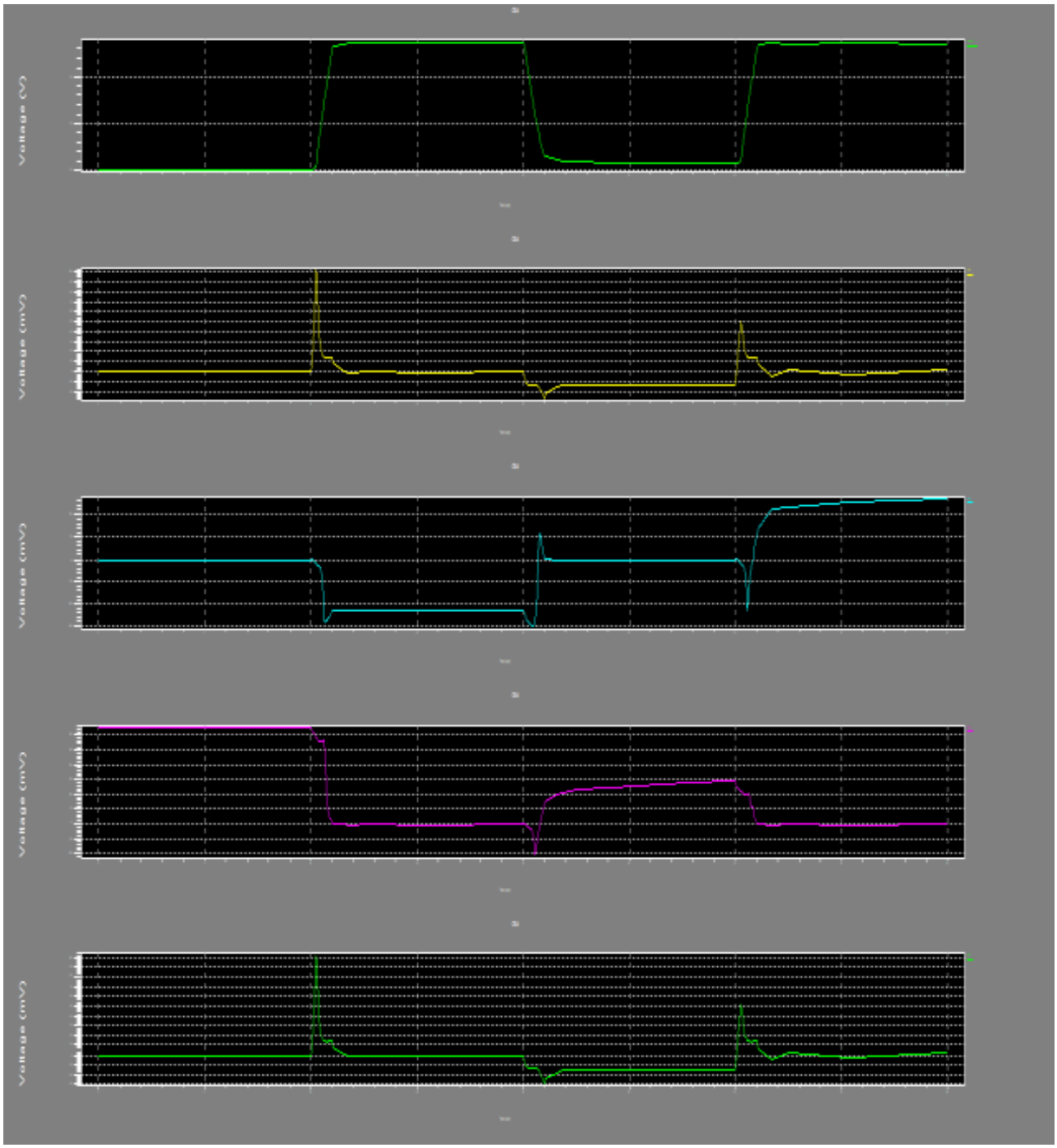

Fig.5. Simulation waveform

Conclusions

The modified CSA has high speed and less power consumption because of using modified XOR, full adder and CPL MUX circuits. The modified CSA has the good driving capability and less output capacitance. From simulation results, the modified full adders have low power utilization and reduced area compared to normal circuits. The modified CSA works reliably at VDD values 5v.

Conflict of interest

Authors declared no conflict of interests.

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