To Minimize the Total Harmonic Distortion of Cascaded Multilevel Inverter

Amrinder Singh, Prince Jindal
Department of Electrical Engineering, Bhai Gurdas Institute of Engineering and Technology Sangrur, India

***Abstract*—** For the various advantages of multilevel inverter (MLI) are used in the power system to control the voltage. The high quality of MLI waveforms allows, minimizing the total harmonic distortion (THD), less electromagnetic interference (EMI) and lower dv/dt ratio. In the present work different types of MLI are studied and various levels of cascaded multilevel inverter (CMLI) are design. The sinusoidal pulse width modulation (SPWM) technique is used. In the simulation work THD value of various CMLI is compared.

Keywords*—Cascaded multilevel inverter (CMLI), Total harmonic distortion (THD), Sinusoidal pulse width modulation (SPWM)*

I. INTRODUCTION

The use of multilevel inverter (MLI) having low total harmonic distortion (THD) have been widely accepted as next generation to reduce the harmonics. MLI can be used to provide the smooth output at critical points in the circuit. In the large network system there is used to maintain the supply voltage which must be free from the harmonics. This can be done by using the MLI. By using the MLI the harmonics are reduced without disturbing the average power. In recent years there has been a growing interest in MLI topologies since they can extend the application of power electronics systems to higher voltage and high power ratios. The technology of MLI is very attractive for medium to high voltage range (2-13kV) applications, which includes motor drive systems, power distribution, power quality and power conditioning applications. There are various types of MLI such as (i) diode clamped MLI (DCMLI) (ii) flying capacitor MLI (FCMLI) (iii) cascaded MLI (CMLI). Out of these MLIs CMLI is the best MLI, which has low THD, lower EMI and less dv/dt ratio. MLIs are based on the fact that sine wave can be approximated to step waveform. These steps being supplied from different dc sources connected in series. The level of the MLI can be calculated by using the formula m= 2s+1. Where 'm' is the level of the MLI and's' is the number of dc sources. As the level of the inverter increases, synthesized output waveform has more steps, producing very fine stair case waveform, approaching very closely to the desired sine waveform. The various types of pulse width modulation (PWM) techniques are (i) selective harmonic elimination

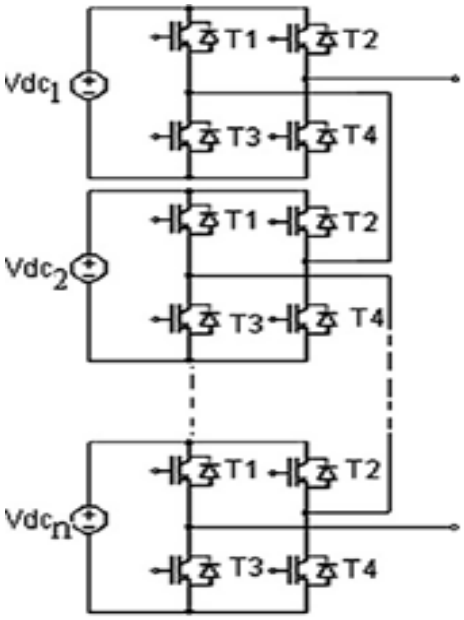

Fig. 1: Basic circuit diagram of MLI

PWM (SHEPWM) (ii) space vector PWM (SVPWM) (iii) sinusoidal PWM (PWM). Out of these modulation techniques SPWM is the best technique, in which sinusoidal wave form is compared with the triangular waveform. Fig 1 shows the basic circuit diagram of MLI.

II. MULTILEVEL INVERTERS

MLI are of three types as given below:

(1) Diode Clamped Multilevel Inverter

(2) Flying Capacitor Multilevel inverter

(3) Cascaded Multilevel Inverter

A. Diode Clamped Multilevel Inverter

A DMLI is shown in fig 2. The DC bus consists of four capacitors: C_1, C_2, C_3 and C_4. For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMLI output voltage synthesis is relatively straightforward [3][7][8][9]. An m-level DCMLI typically consists of (m-1) capacitors on the DC bus and

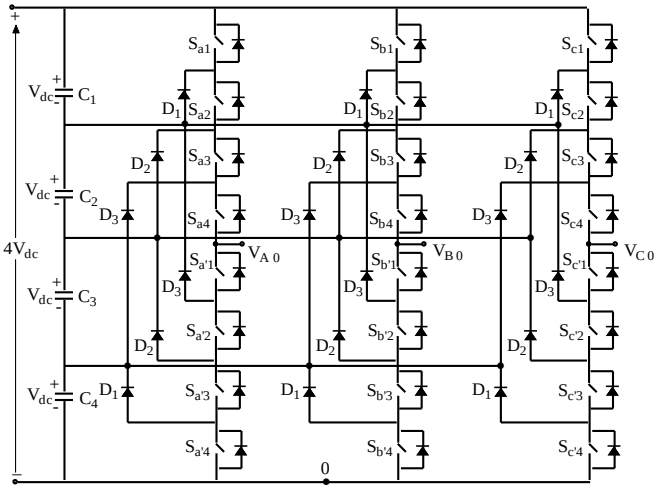

Fig. 2: Diode clamped MLI

produces (2m-1) levels of the phase and line voltages respectively. Each of the three phases of the inverter shares a common DC bus, which has been subdivided by four capacitors C_1, C_2, C_3 and C_4, voltage across each capacitor is V_{dc} and total DC link voltage is $4V_{dc}$ [5][9][12][14]. There are four complementary switch pairs in each phase, i.e., S_{a1}-$S_{a'1}$, S_{a2}-$S_{a'2}$, and S_{a4}-$S_{a'4}$.

B. Flying Capacitor Multilevel Inverter

The structure of this inverter is similar to that of the DCMLI except that instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the FCMLI is shown in fig 3. This topology has a ladder structure of DC side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage synthesis in a flying-capacitor inverter has more flexibility than a DCMLI [3][8][9][10][13]. Unlike the DCMLI, the FCMLI does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the FCMLI has phase redundancies, whereas the DCMLI has only line-to-line redundancies.

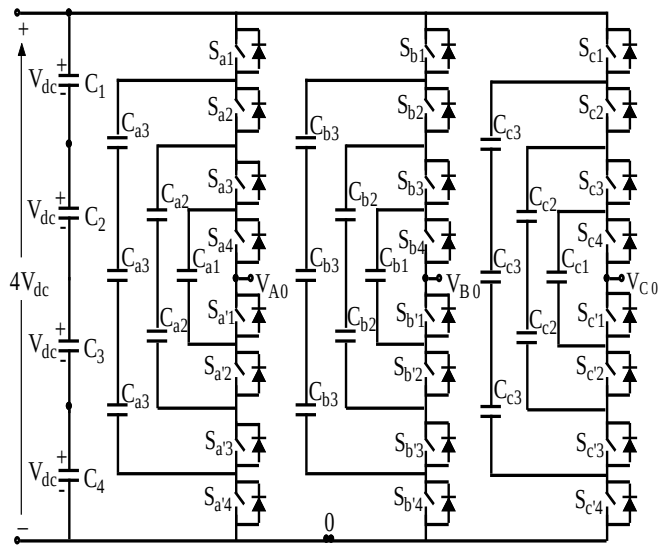

Fig. 3: Flying capacitor MLI

capacitors redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels. In addition to the (m-1) dc link capacitors, the m-level FCMLI will require (m-1) × (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches.

C. Cascaded Multilevel Inverter

Cascade multilevel inverter with separate dc sources is a relatively new inverter structure among the family of MLIs. A generalized structure of three-phase CMLI is shown in Fig. 4. It consists of series connected single-phase full-bridge or H-bridge inverter in each phase with separate DC source (V_{dc}) to each unit. Each inverter unit can generate three different voltage outputs, $+V_{dc}$, 0 and $-V_{dc}$ by connecting the DC source to the AC output by different combinations of the four switches, S_{a11}, S_{a12}, S_{a13} and S_{a14}. To obtain $+V_{dc}$, switches S_{a11} and S_{a14} are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_{a12} and S_{a13}. By turning on S_{a11} and S_{a12} or S_{a13} and S_{a14}, the output voltage obtained is 0. The number of output phase voltage levels (m) in a CMLI is defined by m = 2s+1, where s is the number of separate DC sources or H-bridges per phase [3][6][8][10][12][13]. The AC output of each H-bridge is connected in series and the resultant output voltage waveform thus obtained is shown in fig 5. The magnitude of the A.C. output phase voltage is given by $v_{a0} = v_{a1}+v_{a2}+v_{a3}$ [18], where v_{a1}, v_{a2} … v_{a3} are the magnitudes of output voltages of H_1, H_2, H_3 bridges respectively.

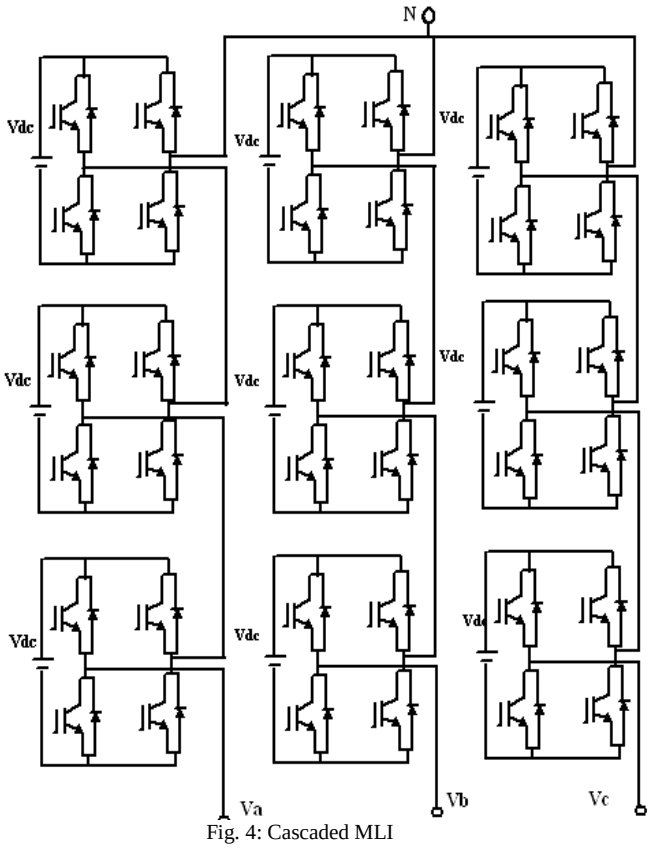

Fig. 4: Cascaded MLI

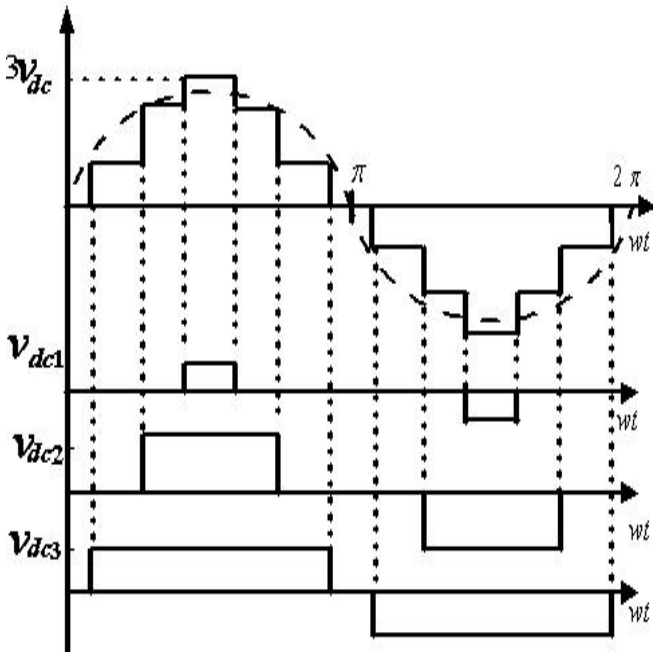

Fig. 5: Waveform of cascaded MLI

The difference between the three MLI is shown in the table 1.

Table 1: Difference between various types of MLI

TOPOLOGIES	DC MLI	FC MLI	CMLI
CLAMPING DIODE	(m-1) (m-2)	0	0
DC SIDE BUS CAPACITOR	m-1	m-1	(m-1)/2
BALANCING CAPACITOR	0	(m-1) (m-2) /2	0
FREE WHEELING DIODE	2 (m-1)	2 (m-1)	2 (m-1)
MAIN SWITCHES	2 (m-1)	2 (m-1)	2 (m-1)

III. PULSE WIDTH MODULATION

Pulse Width Modulation (PWM) is a technique where the duty ratio of a pulsating waveform is controlled by another input waveform. The intersections between the reference voltage waveform and the carrier waveform give the opening and closing times of the switches. The various modulation techniques are given below:

(1) Selective Harmonic Elimination PWM (SHE PWM)
(2) Space Vector PWM (SV PWM)
(3) Sinusoidal PWM (SPWM)

A. Selective Harmonic Elimination PWM

In this technique fundamental switching frequency is used to eliminate the particular defined number of harmonic orders [2][8]. This scheme is based on the fact that to eliminate the defined number of harmonic order the switching angles are defined and Fourier expansion of output waveform is obtained. To eliminate the defined number of harmonic order is given in the equation number (1).

$$v(wt) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi}\left(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)\right)\sin(n\omega t) \quad (1)$$

Where,
n= number of harmonic order
$\boldsymbol{\theta}$= switching angle

B. Space Vector PWM

This is the alternative popular control method for the MLI. This method uses the control variables directly. This technique use level shifted carrier forms than reference waveforms [8][11][14]. In SVM the maximum peak of output voltage waveform is 15% greater than triangular carrier based modulation techniques. But in the SVM the sector identification and look up table requirement for the switching interval for all the vector is very complex. As the level increases this problem increases to minimize this DSP and microprocessors are used, which makes this technique very bulky. For a three phase three level the space vector diagram consists of six sectors, which have $(m-1)^2$ vector combinations per sector and m^3 switching. In fig. 6, 27 different states have been located to find the required switching states.

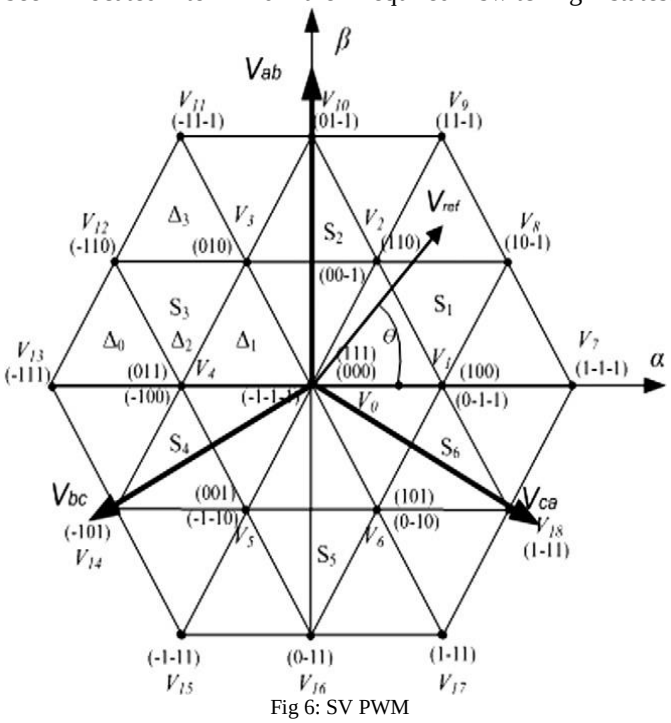

Fig 6: SV PWM

C. Sinusoidal PWM

This is the most widely technique used for the MLI. In this technique sinusoidal waveform is compared with the carrier

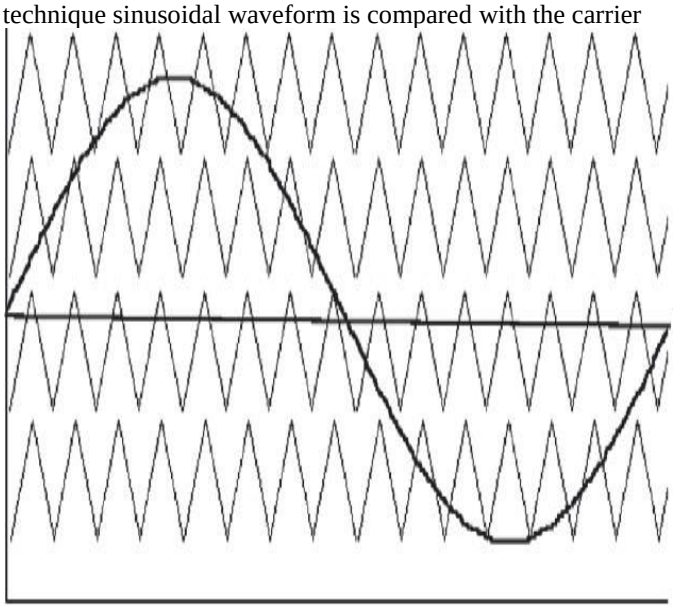

Fig. 7: SPWM

waveform, which generates the carrier signals for the switches. The main problem in this technique is that, power dissipation is very high. The SPWM technique produces a sinusoidal waveform by filtering an output pulse waveform with varying width. A high switching frequency leads to a better filtered sinusoidal output waveform. The desired output voltage is achieved by varying the frequency and amplitude of a reference or modulating voltage. The variations in the amplitude and frequency of the reference voltage change the pulse-width patterns of the output voltage but keep the sinusoidal modulation. A low-frequency sinusoidal modulating waveform is compared with a high-frequency triangular waveform, which is called the carrier waveform. The switching state is changed when the sine waveform intersects the triangular waveform [3][5][8][9][13]. In fig 7 the basic diagram of SPWM technique is given. The crossing positions determine the variable switching times between states. In three-phase SPWM, a triangular voltage waveform is compared with three sinusoidal control voltages (Va, Vb, and Vc), which are 120 degree out of phase with each other and the relative levels of the waveforms are used to control the switching of the devices in each phase leg of the inverter.

IV. CARRIER SIGNALS

For comparing the sinusoidal wave with the carrier waveform, there are various carrier signals are used. The various types of carrier signals are given below:

(1) Phase Dissipation
(2) Phase Opposition Dissipation
(3) Alternative Phase Dissipation
(4) Phase Shifted

A. Phase Dissipation

In this technique m-1 carrier waveforms are required. All the carrier waveforms are in phase as shown in fig 8. In this technique the significant harmonic energy is concentrated at f_c. But because of co phase component it does not appear in the line voltage [1][6][10][11].

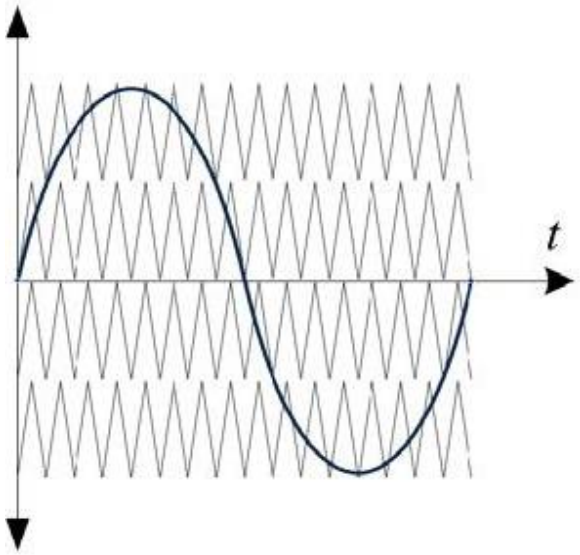

Fig 8: Phase dissipation

B. Phase Opposition Dissipation

In this technique all the carrier waveforms are in phase below and above the zero level. But there is 180 degrees phase shift between the waves below and above the zero level shown in fig 9. In this technique harmonics are located at f_c for phase and line voltage waveforms [4][6][10][11].

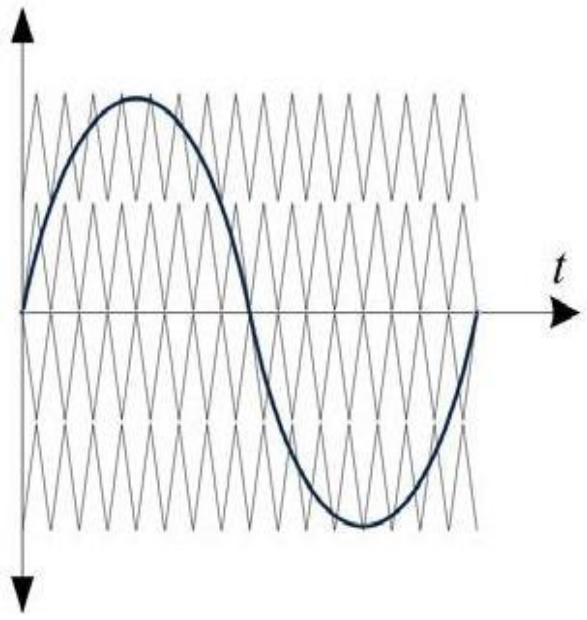

Fig 9: Phase opposition dissipation

C. Alternative Phase Opposition Dissipation

In this technique m-1 carrier waveforms are required similar to phase dissipation. The carrier waveforms are displaced from each other by 180 degrees alternatively shown in fig 10. In this technique no harmonics occurs at sideband around f_c [1][3][6][10].

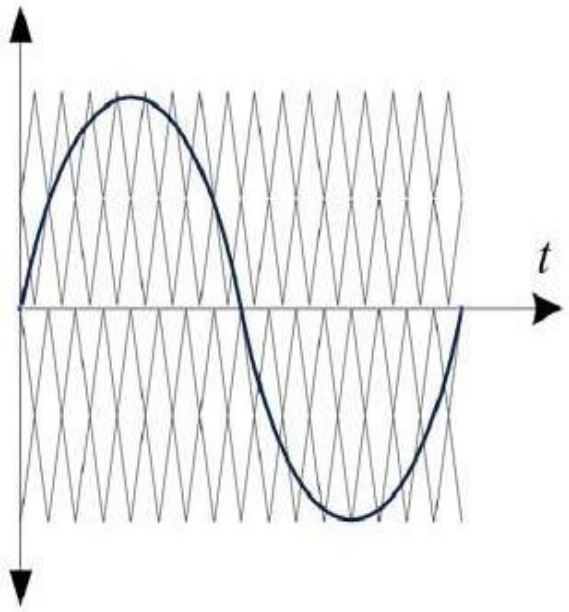

Fig 10: Alternative phase opposition dissipation

D. Phase Shifted

In this technique numbers of carriers are used, which are phase shifted accordingly shown in fig 11. The harmonics are produced at side bands $(m-1)\times f_c$. Higher the number of level more the wider gap between fundamental and significant harmonics [1][3][10][11].

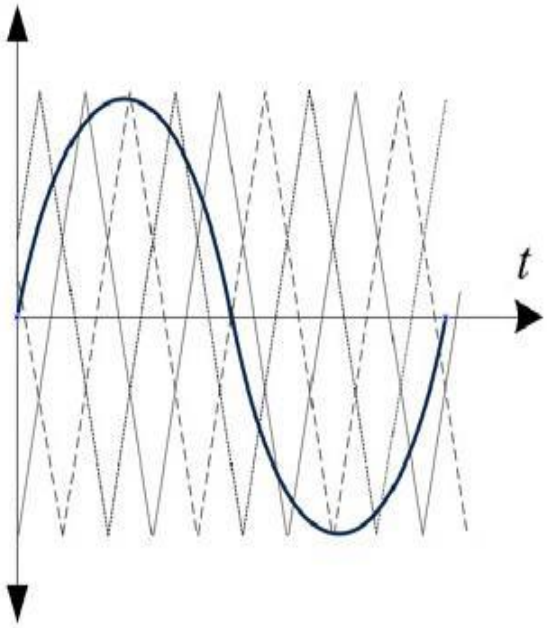

Fig. 11: Phase Shifted

V. SIMULATION RESULTS

In the table 2 THD level of various CMLI is given in table 2. From the simulation it is concluded that CMLI is the best then other MLIs and SPWM is the best among all. The THD value of two level inverter to eleven inverter is shown in fig. 12-18.

Table 2: THD value of various level of CMLI

CASCADE MULTILEVEL INVERTER	THD VALUE (%)
Two Level Half Bridge	77.78
Two Level Full Bridge	33.84
Three Level	21.60
Five Level	16.69
Seven Level	15.88
Nine Level	7.23
Eleven Level	4.54

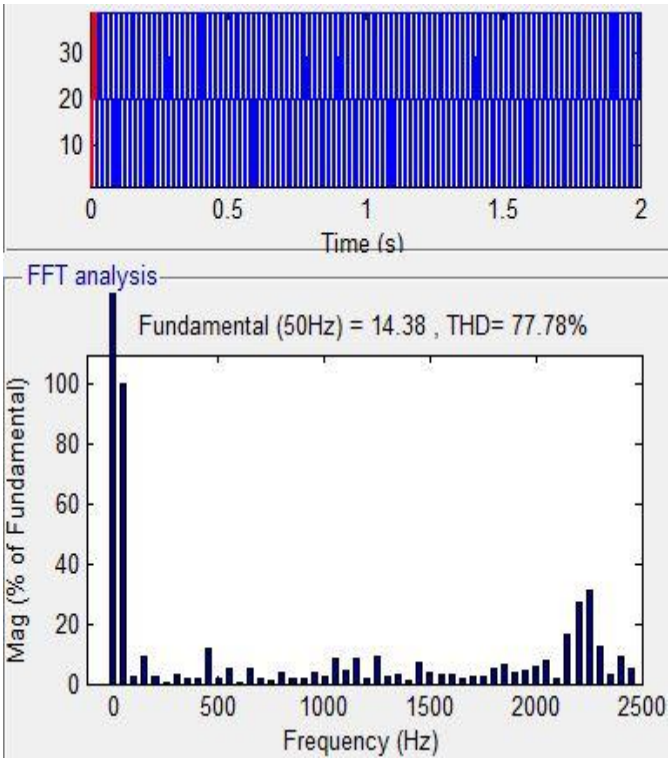

Fig. 12: Two Level Half Bridge Inverter

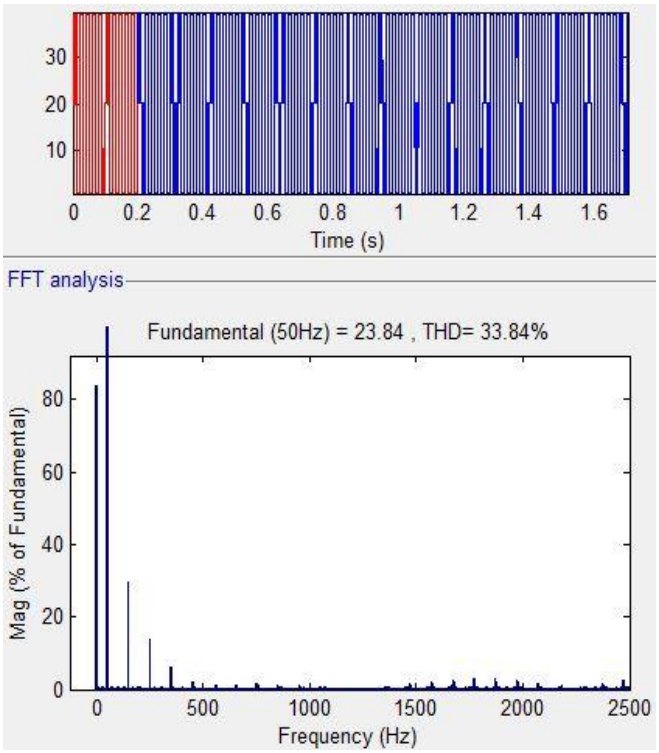

Fig. 13: Two Level Full Bridge Inverter

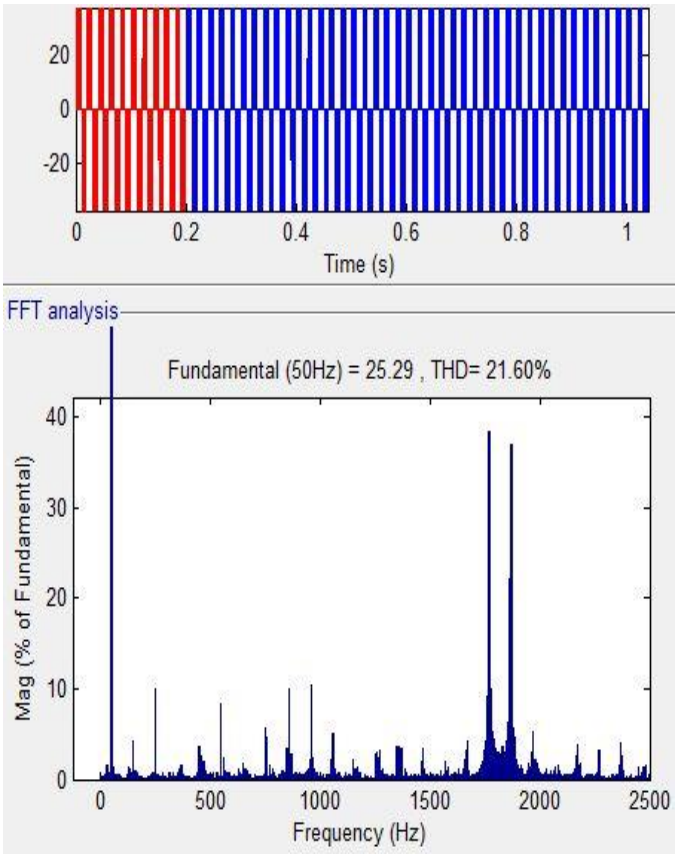

Fig. 14: Three level Inverter

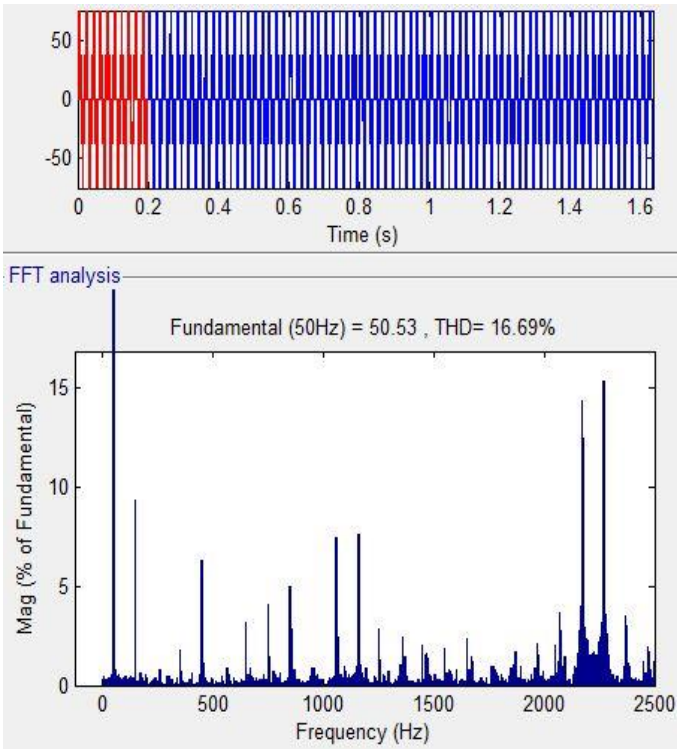

Fig. 15: Five Level Inverter

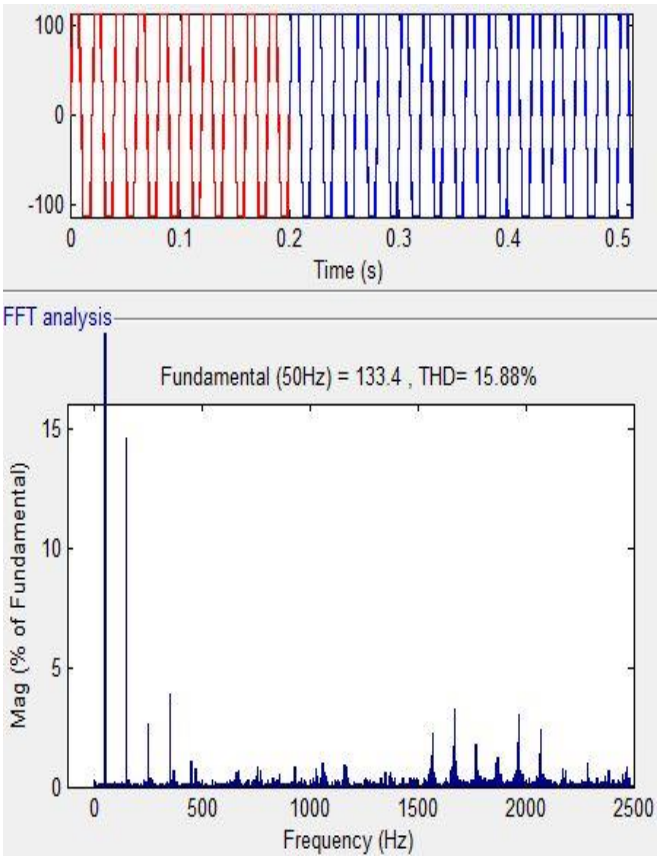

Fig. 16: Seven level Inverter

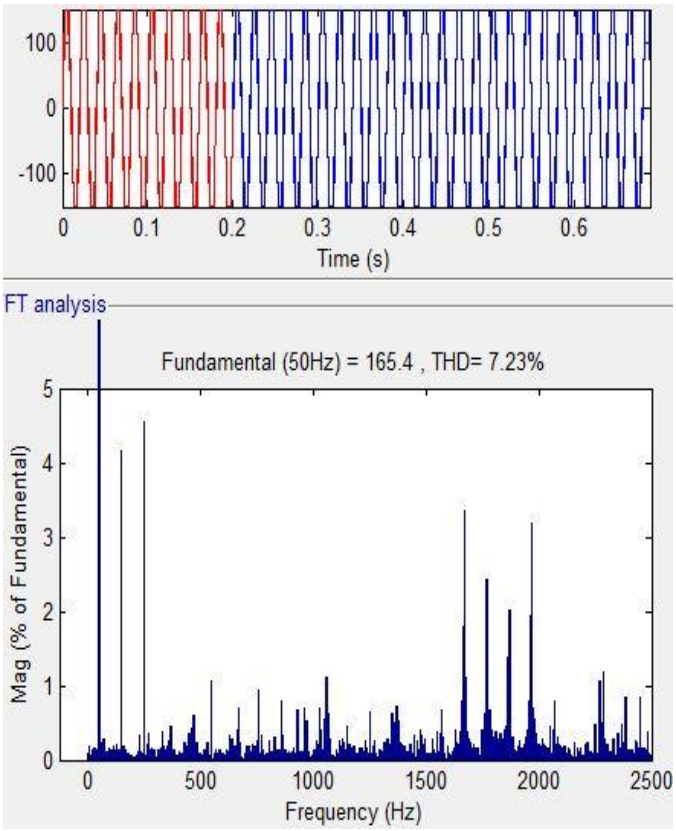

Fig. 17: Nine level Inverter

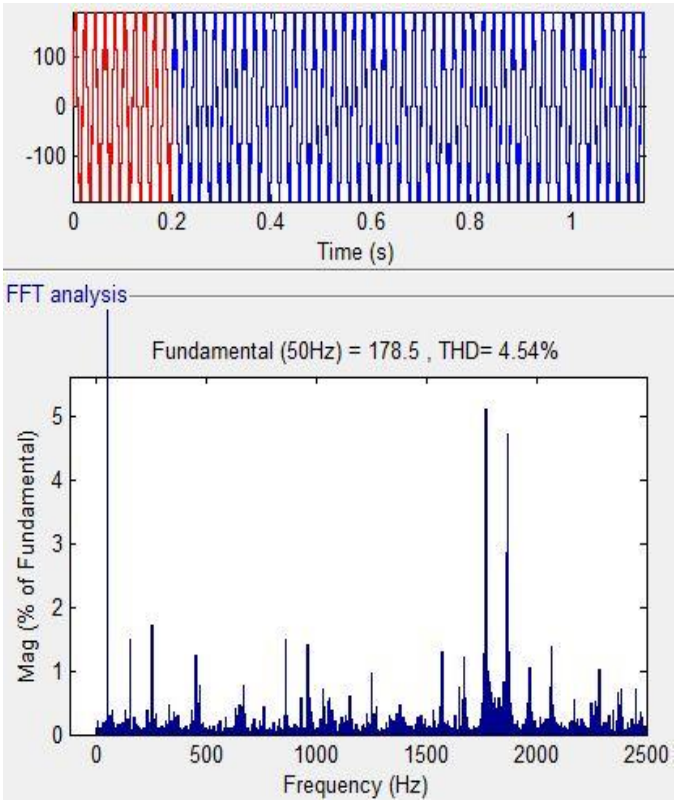

Fig. 18: Eleven level Inverter

VI. CONCLUSION

From the simulation work it is concluded that as the level of the inverter increases THD level increases, which must be less than 5% according to IEEE-519 and in the proposed work it reduced to 4.54 %. From the simulation it is also concluded that SPWM technique is better than other modulation techniques.

ACKNOWLEDGEMENT

The author would like to thank Bhai Gurdas Institute of Engineering and Technology (BGIET), Sangrur, India and faculty members of Electrical Engineering Department of BGIET Sangrur, India for providing such a good environment for the simulation work.

REFERENCES

[1] V Kumar Chinnaiyan, Dr. Jovitha Jeorme, J. Karpagam and Suresh "Control Techniques For Multilevel Voltage Sourse Inverter" IPEC, pp. 1023-1028, 2006.

[2] E.A. Mahrous, N.A. Rahim and W.P. Hew "Three-Phase Three-Level Voltage Source Inverter With Low Switching Frequency Based On The Two-Level Inverter Topology" IET Electr. Power Appl., pp. 637–64, 2007.

[3] Panagiotis Panagis, Fotis Stergiopoulos, Pantelis Marabeas and Stefanos Manias "Comparison Of State Of The Art Multilevel Inverters" IEEE, pp 4296-4301, 2008.

[4] Wenyi Zhang, Wensheng Chen "Research on Voltage-Source PWM Inverter Based on State Analysis Method" IEEE, pp. 2183-2187, 2009.

[5] Ilhami Colak Ersan Kabalci, Ramazan Bayindir "The Design And Analysis Of A 5-Level Cascaded Voltage Source Inverter With Low THD" IEEE, 575-580, 2009.

[6] P. Palanivel S.S. Dash "Analysis Of Thd And Output Voltage Performance For Cascaded Multilevel Inverter Using Carrier Pulse Width Modulation Techniques" IET Power Electronics, vol 4, pp. 951–958, 2010.

[7] A Ravi, P.S. Manoharan , J. Vijay Anand "Modeling And Simulation Of Three Phase Multilevel Inverter For Grid Connected Photovoltaic Systems" Solar Energy , vol 85, pp. 2811-2818, 2011.

[8] Ilhami Colak a, Ersan Kabalci b, Ramazan Bayindir a, "Review Of Multilevel Voltage Source Inverter Topologies And Control Schemes" Energy Conversion and Management, vol 52, pp. 1114–1128, 2010.

[9] Kapil Jain, Pradyumn Chaturvedi "Matlab -Based Simulation & Analysis Of Three Level Spwm Inverter" IJSCE, vol 2, pp. 56-59, 2012.

[10] T.Prathiba, P.Renuga "A Comparative Study Of Total Harmonic Distortion In Multilevel Inverter Topologies" JIEA,Vol. 2, pp. 26-36, 2012.

[11] Venkatachalam Kumar Chinnaiyan, Jovitha Jerome, J. Karpagam "An Experimental Investigation On A Multilevel Inverter For Solar Energy Applications" Electrical Power and Energy System, vol 47, pp. 157-167, 2011.

[12] Divya Subramanian, Rebiya Rasheed "Five Level Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique" IJEIT, Vol. 3, pp. 438-441, 2013.

[13] Abdelaziz Fri, Rachid El Bachtiri, Abdelaziz El Ghzizal "A Comparative Study Of Three Topologies Of Three-Phase (5l)

Inverter For A Pv System" Energy Procedia, Vol. 42, pp. 436 – 445, 2013.

[14] M. Valan Rajkumar , P.S. Manoharan , A Ravi "Simulation And An Experimental Investigation Of Svpwm Technique On A Multilevel Voltage Source Inverter For Photovoltaic Systems" Electrical Power and Energy System, vol 52, pp. 116-131, 2012.

Amrnder Singh, born in India, on 01 august 1989. He received his B.Tech in Electrical Engineering from SBSCET Ferozepur. He is pursuing M.Tech in Electrical Engineeing from BGIET Sangrur, India. His area of interest in power electronics.

Email: amrinderbittu@gmail.com

Prince Jindal, born in India, on 18 november 1985. He is working as a Assistant Professor in the Department of Electrical Engineering at BGIET Sangrur, India since last five years. He received his B.Tech in Electrical Engineering from SUSCET Tangori, India and M.Tech in Power System and Electric Derive from Thapar University Patiala, India. His area of interest in power electronics.

Email: thaprian.prince@gmail.com