A REVIEW ON LOW POWER DESIGN AND TESTING OF 6T SRAM CELL

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***Abstract*-** Power consumption is rapidly increasing for Static Random Access Memory, with increasing speed and area requirements, so lower power design techniques are required. Clock-gating methodologies have been used with commendable results in decreasing total power dissipation average. As we move into process technologies below the 100nm technology node, novel failure mechanisms are coming into picture for a CMOS circuit. In this paper, a low power design of SRAM using clock gating has been studied and the evolving failure mechanisms because of differences in threshold voltage of transistors in SRAM have been analyzed, which results from process variations. Optimizations in the March sequences have been studied to cater to these failure mechanisms. All this has been done involving a minimal overhead on test time.

Keywords — March test, clock gating, Dual port SRAM, Failure mechanisms

I. INTRODUCTION

The strong appealing that the rapidly emerging VLSI chips have for SRAMs, leads to both area and power constraints on these SRAMs to be used in the memory chips. Among the various designs that have been implemented for SRAMs, it has been found that the 6-T cell is most stable [16] among the 4-T, 7-T, 8-T, 9-T and 11-T cells [10]. Therefore, this paper uses 6-T cells. Various techniques exist for providing the area and power constraints that are being imposed on the SRAM chips [12]. To reduce the power dissipation, multiple methods can be implemented at different levels, like floor planning level [11], architectural level or using the power gating approach or self timed approach [11]. This paper particularly studies the clock gating approach, as clock signals lead to a 30%-70% of the total dynamic power dissipation. So, working on the clock to reduce the power consumption is deemed to be an optimum design. Furthermore there is a high need of fault free, self reliant SRAMs. Various sources of faults are emerging in SRAMs [8] with technology scaling. Various testing methodologies exist to ensure the same which include BIST [7] through March algorithms, transient current testing [2]. Here, different march algorithms are studied and the modified march algorithm have been studied to get a higher fault coverage and a reduced computation time [9], [13].

II. CLOCK GATING

The propagation of the clock signal in the logic gates and interconnections, constitutes a large part of the average dissipated power in a chip, on account of clock signal's high activity of switching. Clock gating ,one such method, to decrease clock induced power wastage [11]. Whenever, clock signal is not needed, it is deactivated, thereby reducing the unnecessary power dissipation in charging and discharging of the circuit. Clock-gating thus, provides savings in power by decreasing the switching activity on those circuit signals and avoiding unnecessary activity of those circuit modules which are of no consequence to the circuit [3], [18]. It is using ICG cells, Integrated Clock Gating. So it also saves die area occupied by the multiplexers by replacing them with ICG cells. The basic clock gating structure is shown in the Fig. 1. Since the clock gating structure is inside the clock tree, so it changes the clock tree structure. There are multiple ways to add clock gating logic to a design. Some of them are:

- By coding it as enable condition into the RTL (Register transfer level) code. The synthesis tools automatically add it as clock gating logic(fine grain clock gating).
- By making use of libraries, with Integrated Clock Gating, ICG cells for gating of the clock, of the particular sub-circuits. This has to be manually inserted into design file by the RTL.
- By automated tools for gating of clock, which insert an enable condition or add ICG cells in the Register Transfer level code or add ICG cells into the RTL.

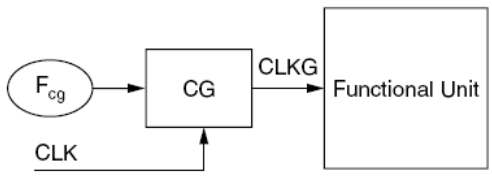

Fig 1: Clock gating

Before implementing clock gating in a VLSI circuit some important points are to be kept in mind:

i]The clock should only be turned on or off by the clock gating technique. It should not change the waveform of the clock in any form.

ii] The violations in clock gating, including both the setup time and hold may be corrected, similar to other violations in physical design, using multiple techniques like clock skewing/buffering.

iii] The phase of clock gating signal should be taken care of by the designer if the clock signal is being divided.

iv] Glitches in the gated clock should be taken care of.

Clock gating can be implemented via various techniques, depending on whether the design to be implemented is latch free, latch based, flip-flop based, or using the inbuilt option of clock gating present in the synthesis tools.

The latch-free design uses an AND or OR gate [1], but a shortcoming of this technique is that if in between a single clock period, the enable signal gets inactive, then the gated clock signal can terminate, as shown in the Fig. 2. This makes the design erroneous for use in flip flop based circuitry.

In the latch based design, edge sensitive latch is used in the design, so the enable signal is just considered when, around the edge of the clock pulse, thereby overcoming the problem in latch free design. The technique of flipflop based design is quite similar to that of the design based on latch with the exception that in place of latches D-flip-flops are used.

It is shown in the Fig. 3, the way the enabled design is gated to the clock transformation design.

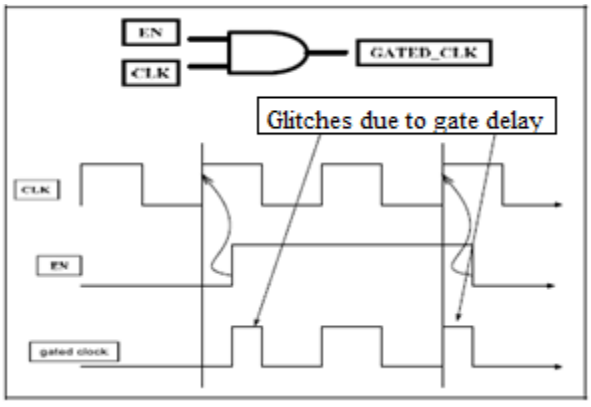

Fig 2: Clock gating-latch free

It's advantage over the design with gated clock is that it lead to an easier implementation of testability and a better control of the clock skew.

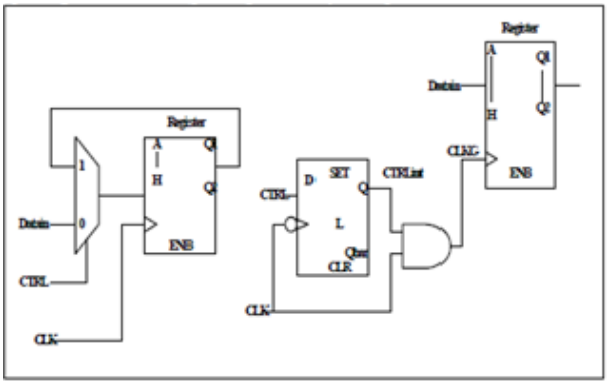

Fig 3: Clock gating- Flip flop based.

III. MECHANISMS OF FAILURE AND THEIR CORRESPONDING FAULT MODELS

In single port SRAMs, intra-die variations, leading to inter-variations in similar transistors' parameters (L or W or geometry and threshold voltage V_t) or undesired particles called spot defects(SD) cause memory failures [14], [15]. These variations appear as intrinsic fluctuations of threshold voltage due to the random dopant effect [13]. Here faults due to variations in V_t have been studied. Testing of dual port SRAM needs tests different from those of single port SRAM because dual port needs multiple and simultaneous accesses to sensitize the faults. A 6-T SRAM cell is specifically prone to process variations due to the constraint of area. This perhaps results in any of the following conditions.

1)Weak access transistors, AXL, AXR (Fig. 4), connecting the latch cell to the bit/bit' lines, or weak pull down transistors cause a decrease in discharging current in bit line, causing the Sense Amplifier(SA) to detect a lesser difference in the voltage between the bit lines. So, it leads to wrong evaluation by SA (Fig. 5).

2)The presence of access transistors that are stronger or pull-down transistors that are weaker NL, NR cause an increase in the voltage of the node storing "0" in SRAM cell, during read operations. Due to this, the contents of the cell can flip while the read operation is being performed. This is referred to as flipping read failure. But since the flip of voltage of internal node may occur in a later stage of read cycle, so it can happen that the flip does not cause a change in the bit line voltage differential due to which the logic after read is the correctly stored logic.

3) The presence of stronger pull-up transistors or weaker transistors in pull down section cause a drift in tripping point

of the coupled transistors, making up the SRAM cell . This drift is generally to a increased voltage, leading to an unsuccessful write in the cell, referred to as write failure.

4) In order to save leakage, the supply voltage is generally reduced, this can lead the cell to abandon its contents, even when the cell is not being approached. This is called hold failure [17]. It occurs due to high degree of mismatch between the cross coupled inverters, making up the SRAM cell.

5) Spot defects are generally encountered in dual port SRAM cells, causing unwanted connections or disconnections in memory [15]. They include opens, shorts as well as bridges, where open refers to an added resistance inside an already existing connection and a short refers to the creation of an unwanted resistive connecting path between a node and either the power supply for logic 1 or the power supply for logic 0. Bridge Short refers to the creation of an unwanted resistive connecting path between the two nodes.

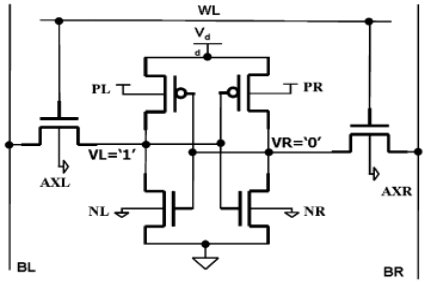

Fig. 4: The 6-T SRAM cell

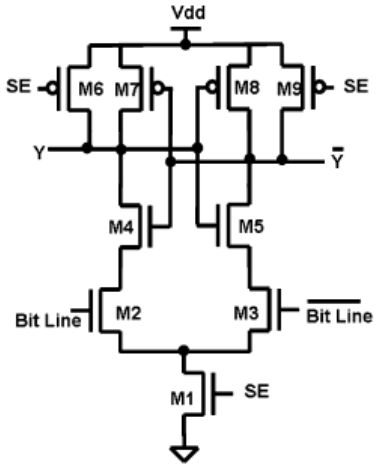

Fig. 5: The Sense amplifier

IV. MARCH ALGORITHM FOR TESTING OF SRAM

March algorithm is a widely used testing algorithm because of it's high fault coverage, but it has a very high computational time. A complete March test is given in the "{….}" and each March element is specified in "(…)". represents either an upward addressing order or a downward addressing order. The March Notation for both the single and dual port SRAMs has been given here.

A) *Functional Fault Models for Single Port SRAM*

The Functional Fault Models (FFMs)for single port SRAM include(1PF1s), that is faults involving single cells and (1PF2) that is faults involving 2 cells. In 1PF2, the 2 cells are the aggressor cell, ca, cell used for sensitization of v-cell's fault, c_v. In 1PF1the v cell itself is aggressor cell.

Fault primitive for IPF1 is given as <*S/F/R*>, whilst that for 1PF2 is given as <S_a; S_v /*F/R*>,

where S is the sensitizing operation in aggressor cell(S_a) or victim cell(S_v), F represents logic in the victim cell, R is the value of SRAM, once read sensitization function is done on the victim cell.

B) *Functional Fault Models For Dual Port SRAM*

Two port faults(2PFs) need two ports to be sensitized at the same time, so single port fault models are insufficient here [15]. The 2PF are classified into -2PF1s (faults in dual port comprising one cell) and 2PF2s (faults in dual port comprising 2 cells, aggressor and victim cell.

The 2PF1s are sensitized if the same victim cell is victimized by the two ports at the same time. The notation is given as: <S_1:S_2/F/R>; this is the representation of a two port fault making use of just the victim cell for both sensitization and detection. S_1:S_2 represent both the sensitization functions implemented simultaneously to victim cell through the two ports. v-cell's data is given by F. R is the logic read from the v-cell, when read is done on SRAM, as a result of the sensitizing operations. Similarly the 2PF2s are given by 3 types:

$2PF2_a$: It represents sensitization of the victim cell's fault through both operations applied at the same time on one aggressor cell. It is denoted by

$<S_a : S_a ; S_v /F/R>_{a,v}$

$2PF2_v$: It represents sensitization of victim cell's fault through both operations applied at the same time on victim cell itself. It is denoted by $<S_a ; S_v ; S_v /F/R>_{a,v}$

$2PF2a_v$: This represents sensitization of the victim cell's fault both operations applied at the same time on the v-cell and the other on the a-cell. It is denoted by $<; S_a ; S_v /F/R>_{a,v}$

The March algorithm consists of various march elements applied in different orders that detect a wide range of faults. Various modifications have been proposed to make the March test more

efficient in terms of the computation times and fault coverage [9]. In single port faults, for the conventional single cell fault models and the coupling fault models, the commonly used base sequence was, March C-[13]. However detection of deceptive read destructive faults, was not covered by March C-, but due to deviations in the threshold voltage of the various transistors, these frequently occur in memory. Another test sequence called, March SR had been formulated which covered the deceptive read destructive fault, but with time taken to test being 14N (where N is the total count of memory locations), and this is much more than that for March C- (which is 10 N). Furthermore, the typical sequence of March test does not take into account the hold failures. As in the standby mode, it is necessary to importantsupply voltage, in order to decrease the leakage power, as the technology scales, so it is getting necessary to test these faults. So, in another modification, two March sequences have been proposed which covers these fault models and have the least effect on the computation time. The proposed sequence has been called Extended March C-. This gives test time as 12N, thereby giving 15% better test time than that for March SR. It also gives a better fault coverage [13]. Similarly for the dual port SRAMs there is a need to optimize the March sequences with less computation time and high fault coverage. So, with every new modification, the efficiency of memory testing via March algorithms increases.

V. RELATED WORK

Author	Description	Technique used
Qikai Chen	This paper achieves a good fault coverage in memory circuits by using an evolved march test sequence with lesser computation time .	1)An optimized march algorithm to get higher fault coverage 2)Double sensing-at the hardware level, to reduce power loss
Said Hamdioui	This paper gives the need to propose a march test sequence, different from that of single port memories, for dual port memories	A novel march sequence: • 1PF1 • 1PF2 to test dual port memories
Anmol Gulati	Power dissipation in dual port SRAM has been decreased using clock gating.	Negative latch based clock gating
Navneet Kaur Saini	Analysis of the variations in operating conditions on the power dissipation of a 2 MB SRAM has been studied and techniques have been presented to reduce power dissipation under these variations.	Reduction in Power dissipation at: • Floor planning level • Architectural level • Transistor level

V. CONCLUSION

Clock gating is promising for power reduction in circuits promising high performance. This paper, presents the clock gating approach to save power. As the technology scales, memory systems are becoming more prone to functional failures because of process variations. So, the variations in the transistor V_t in an SRAM cell, lead to physical failures, the mechanisms for which have been discussed in this paper, along with their corresponding logical fault models as well. A study of the March test sequences to detect these rising failure mechanisms and the optimized March test sequences, to reduce the test time with better fault coverage has been done.

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