A Review of Various Low Power Compressor Adders for Multipliers

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Abstract- The compressor adders decrease the critical delay compared to conventional adders and can be used in multiplier architectures. A Multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, Digital Signal Processors (DSPs), Microprocessors etc. With the advent of new technology in the domain of VLSI, communication and signal processing, there is an ever going demand for the high speed processing and low area design. Hence the compressors can remarkably reduces power consumption. In this review article, various architectures and designs of arithmetic circuits are discussed.

Keywords- Compressors, Multiplier, .

I. INTRODUCTION

In recent years, the focus of VLSI design is mainly on high performance microprocessors. There is an increase in demand for high speed, small area, low power and low cost designs. It is due to rapid growth of portable battery operated devices such as personal computing devices, wireless communication systems (PDAs and mobile phones), medical applications and other portable devices. Advancement of computer system performance has flattened out as fabrication technology is reaching its physical limit. Therefore there is a need to review circuit designs in search of possible improvement in order to meet the demand of the future for faster computing. One potential area for improvement is in the multiplier unit design. Typically, compressors are used in high speed addition and multiplication unit design in microprocessor. Thus, a faster compressor unit would result in an improvement in the latter for future computer architecture systems design.

A compressor adder provides reduced delay over conventional adders using full adders and half adders. It is represented as N-r, where N represents the number of bits and r represents the total count of 1s present in N bits. It is termed as compressor so that it reduces the gate count and delay compared to other adder circuits. Studies are taken place to improve circuits of lower order compressors.

Multiplication can be considered as a complicated and time-consuming arithmetic operation. Nevertheless, it is the key operation in most of the signal processing algorithm. Generally, the process of multiplication can be split into three stages: generating partial product, reducing partial product, and computing final product . The partial product generation and final product computation concept is shown in Figure 1.

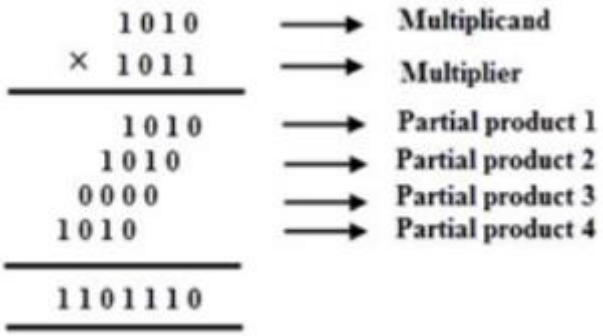

Fig.1: Partial Product Generation and Final Product Computation

This article discusses various designs of arithmetic circuits such as full adders, compressors which are all applicable to the field of low power architectural design.

II. LITERATURE SURVEY

Riya Garg et. al (2013) [1] presents 4-2 compressor using two different 8T full adder designs. The aim of this paper is to reduce the power consumption of 4-2 compressor without compromising the speed and performance. A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. The author first describes about the 4-2 compressors which consists of 5 inputs and 3 outputs. It is called compressors since it compress four partial products into two. In this paper 4-2 compressors using full adders which is made up of existing and proposed 3T XNOR gate is design and discussed. It is designed by compressing two 8T full adder architectures.

Basant kumar and sujit kumar patel (2013) [2] In this paper made an analysis on the logic operations involved in conventional CSLA and BEC-based CSLA to identify both the data dependency, redundant logic operations. They have eliminated all the redundant logic operations of conventional

CSLA.SQRT-CSLA on average for different Bit-width due to small carry output Delay.

Nirlakalla et al. (2011) [3] proposed a (7:3) compressor which consisted of 4 full adders. He proved that 16-T full adder showed lowest PDP and EDP at gate level proving that it is the most energy efficient if compared to the other 4 types of adders mentioned in his paper. However, The research done by Nirlakalla did not take into account the aspect of fan-in and area and these 2 aspects are vital since the fan-in of logic gates or area of compressors increase, the cost increases.

Sreehari Veeramachaneni et. al (2007) [4] presented novel architectures and designs of high speed, low power 3- 2, 4-2 and 5-2 compressors capable of operating at ultra-low voltages. The power consumption, delay and area of these new compressor architectures are compared with existing and recently proposed compressor architectures and are shown to perform better. The proposed architecture lays emphasis on the use of multiplexers in arithmetic circuits that result in high speed and efficient design. In the proposed architecture these outputs are efficiently utilized when compared to existing designs to improve the performance of compressors. In the proposed novel architectures of 3-2, 4-2 and 5-2 compressors, the author replaces some XOR blocks with MUX blocks. Since the availability of the select bits before the input bits arrive completes the switching activity of the transistors, the overall delay in the critical path is reduced while using MUX blocks. This paper concludes by analyzing the proposed architectures of 3-2, 4-2, 5-2 compressors with the conventional architectures.

III. PROPOSED 4-2 COMPRESSOR

In this section a new design of a 4-2 compressor with two 8T XOR-XNOR modules and four MUXs based on transmission gate logic is described. Fig. 2(a) and 2(b) shows the 8T XOR-XNOR module and Transmission Gate Mux respectively. A 4-2 compressor is a combinatory device which compresses four partial products into two partial products. The architecture of a 4-2 compressor is shown in Fig. 3(a). It accepts five inputs namely M1, M2, M3, M4 and Cin; and generates three outputs, viz. Sum, Carry and Cout.

The input Cin is the output coming from a compressor in preceding lower significant stage and the output Cout is the input to a compressor in the consecutive higher significant stage. M1, M2, M3, M4, Cin and Sum are weighted equally as i; and Carry is weighted one binary bit order higher i.e. i+1.

M1 + M2 + M3 + M4 + Cin = Sum + 2 * (Carry + Cout)

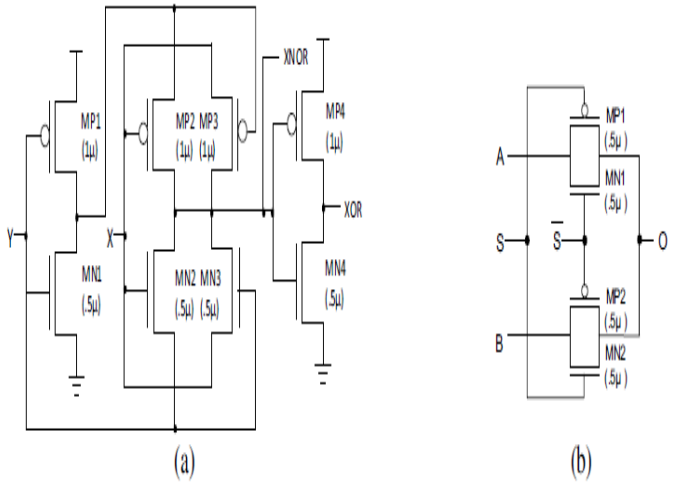

Fig.2: (a) 8T XOR-XNOR module (b) Transmission Gate Mux

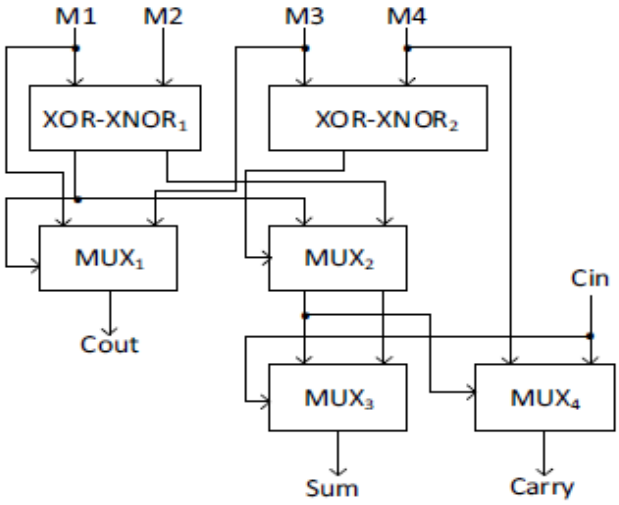

Fig.3: Architecture of Compressor Adder using XOR-XNOR module.

For the reduction of power consumption, the transistors of the inverter are appropriately sized and also the speed of the compressor is heightened by sizing the transistors of transmission gate logic style MUXs equally. The complete circuit diagram of the new proposed 4-2 compressor is shown in Fig. 4.

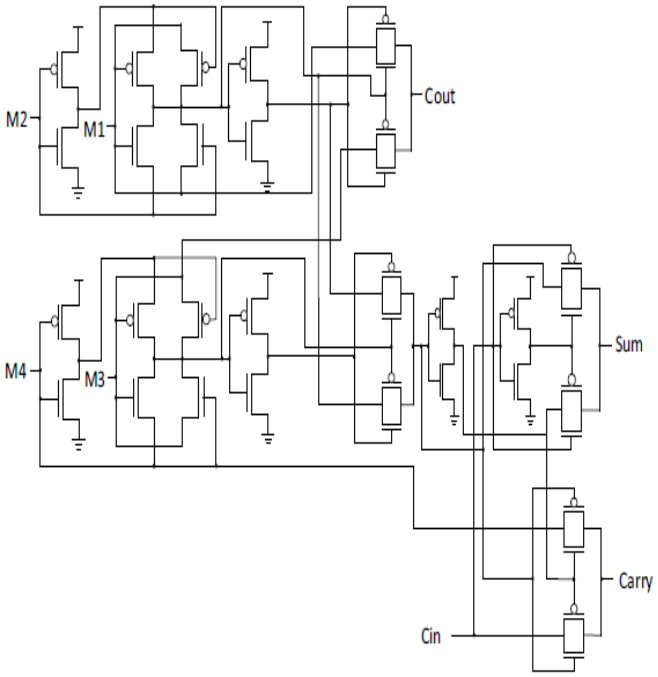

Fig.4: Circuit Diagram of 4-2 Compressor

IV. CONCLUSION

We have discussed various logical techniques of compressor adder and parameters like power delay and power delay product for its improved performance further work can be done on reducing power consumption and delay for high speed so it can be more efficient to work on various applications such as multiplier. As Multipliers are of great significance in today's Digital Signal processing applications like DFT, IDFT, FFT, IFFT, and ALU in Microprocessor.

V. REFERENCES

[1]. Riya Garg, Suman Nehra, B.P. Singh, "Low Power 4-2 Compressors for arithmetic Circuits", International Journal of Recent Technology and Engineering, Vol. 02, Issue No. 01, pp. 204-207, 2013.

[2]. Basant kumar and sujit kumar patel ," Area–delay-power efficient carry select adder ", *IEEE Transaction on circuits and systems II,2013.*

[3]. R. Nirlakalla, R. T. Subba, and T. Jayachandra-Prasad, "Performance evaluation of high speed compressors for high speed multipliers," Serbian Journal of Electrical Engineering, vol. 8, pp. 293-306, 2011.

[4]. Sreehari Veeramachaneni, Kirthi M Krishna, Lingamneni Avinash, Sreekanth Reddy Puppala, M.B. Srinivas, "Novel Architectures for HighSpeed and Low-Power 3-2, 4:2 and 5:2 Compressors", 20th International Conference on VLSI Design, pp: 324-329, 2007.

[5]. Wallace Tree Multiplier Designs: A Performance Comparison Review, Himanshu Bansal, K. G. Sharma, Tripti Sharma, Innovative Systems Design and Engineering ISSN 2222-1727 (Paper) ISSN 2222-2871 (Online) Vol.5, No.5, 2014.

[6]. R. Marimuthu, D. Bansal, S. Balamurugan, and P. Mallick, "DESIGN OF 8-4 AND 9-4 COMPRESSORS FORHIGH SPEED MULTIPLICATION," American Journal of Applied Sciences, vol. 10, p. 893, 2013.

[7]. D. Radhakrishnan and A. P. Preethy, "Low power CMOS pass logic 4-2 compressor for high-speed multiplication," Proceedings of the IEEE Midwest Symposium on Circuits and Systems, vol. 43, pp. 1296-1299, 2000.

[8]. J. R. choi, L. H. Jang, S. W. Jung and J. H. Choi, "Structured design of a 288-tap FIR filter by optimized partial product tree compression," Solid-State Circuits, IEEE Journal of 32.3, pp. 468-476, 1997.

[9]. J. Gu and C-H. Chang, "Ultra low voltage, low power 4-2 compressor for high speed multiplications," Proceedings of the International Symposium on Circuits and Systems (ISCAS), vol. 5, pp. V-321, 2003.

[10]. G. Goto, et al., "A 4.1-ns compact 54× 54-b multiplier utilizing sign-select Booth encoders," Solid-State Circuits, IEEE Journal of 32.11, pp. 1676-1682, 1997.

[11]. H. Kaul, et al., "A 320 mv 56 μw 411 gops/watt ultra-low voltage motion estimation accelerator in 65 nm cmos," Solid-State Circuits, IEEE Journal of 44.1, pp. 107-114, 2009.

[12]. S. R. Huddar, S. R. Rupanagudi, M. Kalpana and S. Mohan, "Novel high speed vedic mathematics multiplier using compressors," International Multi-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), pp. 465-469, 2013.