ANALYSIS OF CMOS AND MTCMOS CIRCUITS USING 250 NANO METER TECHNOLOGY

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Abstract— The low-power consumption with less delay time has become an important issue in the recent trends of VLSI. In these days, the low power systems with high speed are highly preferable everywhere. Designers need to understand how low-power techniques affect performance attributes, and have to choose a set of techniques that are consistent with these attributes .The main objective of this paper is to describe, how to achieve low power consumption with approximately same delay time in a single circuit. In this paper, we designed circuits with CMOS and MTCMOS techniques and verified its power consumption. The circuits designed using MTCMOS technique gives least power consumption as compared to CMOS.

All the pre-layout simulations have been performed at 250nm technology.

Keywords—*MTCMOS, sleep mode, leakage current, header switch, footer switch*

I. INTRODUCTION

In the earlier days VLSI designers mainly concentrated on area, performance, speed, cost and reliability. But this performance improvement has lead to the increase in power dissipation. Reducing this power dissipation and achieving low power consumption has become a challenging task to the current day designers as cooling technology and packing are very expensive and also now a days because of the battery life time, the electronic circuit designers are worried about decreasing the total power consumption to increase the battery life time [11], especially for portable embedded systems and decrease the battery's size which is reflected on the portability of the devices. Power is very much concerned due to the remarkable growth and success of fields like personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption .As the technology continue to scale down a significant portion of the total power consumption in high performance digital circuits is due to leakage current because of reduced threshold voltage [1]. MOSFETs are fabricated with high overall doping concentration, lowered source/drain junction depths, halo doping, high mobility channel materials, etc. Furthermore the reduction of the gate oxide thickness causes drastic increase in the gate tunneling leakage current due to carriers tunneling through the gate oxide, which is strong exponential function of the voltage magnitude across the gate oxide [2],[7] to minimize the leakage current. Here our main aim is to decrease the leakage current using MTCMOS technique.

II. CMOS

Complementary metal-oxide semiconductor is the most leading semiconductor technology used in the transistors that are manufactured into most of today's computer microchips. CMOS logic is well known for its extremely low static power dissipation and high noise immunity. CMOS is sometimes referred to as complementary-symmetry metal oxide semiconductor. Complementary-symmetry refers that a typical CMOS design style uses complementary and symmetrical pairs of p-type and n-type metal oxide field effect transistors for logic functions [8]. In CMOS technology, both kinds of transistors are used in a complementary way to form a current gate that forms an effective means of electrical control.

In this, all the PMOS devices will be together called as pull-up network and substrates are connected to the VDD, all the NMOS devices will be together called as pull-down network and its substrates are connected to the VSS. The output is taken at the centre as a function of inputs.

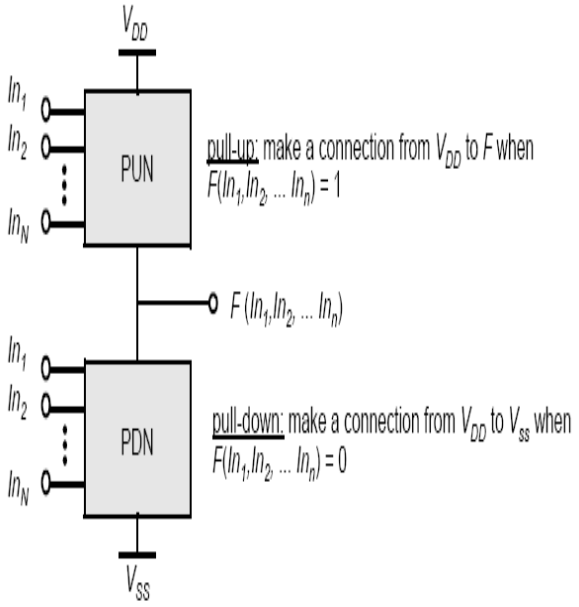

Figure 1 CMOS basic structure.

MTCMOS

Multi-threshold CMOS is a power reduction technique, widely used in today's industry to lower the gate leakage current. The multi threshold CMOS technology has two main parts. First, "Active" and "sleep" operational modes [13] are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip [9]. The low threshold voltage transistor is able to switch faster but has a high leakage current when turned off compared to the high threshold voltage transistor which is slower to switch but has a low leakage current when off. In this we use low threshold transistor for logic and to separate it from power /ground with high threshold transistors and also the circuit is operated at high performances because of low threshold voltage transistor.

When a logic circuit is active, the sleep signals are de-asserted which turn on high threshold voltage transistors and create virtual VDD and GND around the logic. In inactive mode the sleep signals are asserted which separate the logic from the power/ground, there by lowers the leakage current. The MTCMOS technique shows no impact over circuit parameters such as output impedance, gain, threshold voltage, fluctuations and frequency response [10].

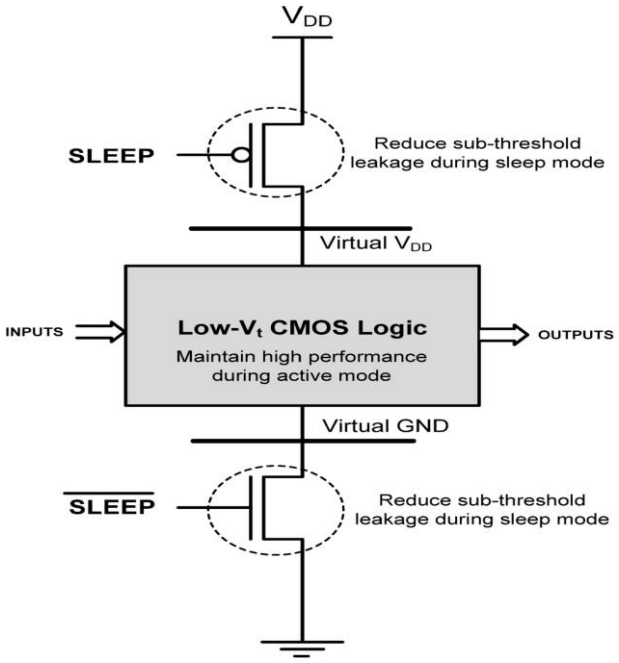

Figure 2 MTCMOS basic structure

III. POWER CONSUMPTION OF CMOS AND MTCMOS CIRCUITS

The Complementary-Metal Oxide Semiconductor technology is well-known for its low power consumption. CMOS gates in older technologies were very efficient. In newer technologies, it has been skyrocketed due to transistor scaling, chip transistor counts and clock frequencies.

The average power over the time interval is

$$Pavg=E/T=(1/T)\int 0T\ iDD(t)VDD\ dt$$

Where iDD(t) is supply current and VDD is the supply voltage.

MTCMOS is a power gating technique in which a power gating transistor will be placed between the logic transistors and either powered or grounded, thus creating a virtual supply and virtual ground, respectively. Power gating is a technique used to reduce power consumption by shutting off the current to blocks of the circuit that are not in use. Lowering the threshold voltage results in an exponential increase in sub- threshold current [6]. As the circuit spends more time in the ideal (stand-by) mode, so it is practical to reduce the leakage current to minimize the static power which represents the dominant part of the total power consumption. Multi-threshold CMOS

(MTCMOS) technology is one of the most effective techniques to reduce the leakage current during the standby mode by using a low threshold voltage transistor in the critical paths of the circuit to improve the performance while the high threshold voltage one is in uncritical paths and is used as an isolation switch between the virtual supply lines (VDD, GND) and the real one [14] . The high threshold voltage transistor is used for power consumption in the shortest path [3],[4]. Both active mode and sleep mode are associated for efficient power management.

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IV. IMPLEMENTATION OF 2-BIT SERIAL IN SERIAL OUT SHIFT REGISTER

A Shift Register is a sequential logic circuit that is used to store a sequence of data and this data is shifted by one clock pulse for every clock period at its output. They are a group of flip-flops that are connected in chain so that the output of one flip-flop will be given as the input to another flip-flop connected to it. All flip-flops are driven by a common clock and also they are set and reset simultaneously as shown in Figure 3. Here we are taking both input and output in a serial manner so we call it as serial in serial out (SISO) shift register. Taking d as the input, clock as the clock input, q1 as MSB and q0 as LSB we get the simulation results as shown in Figure 4.

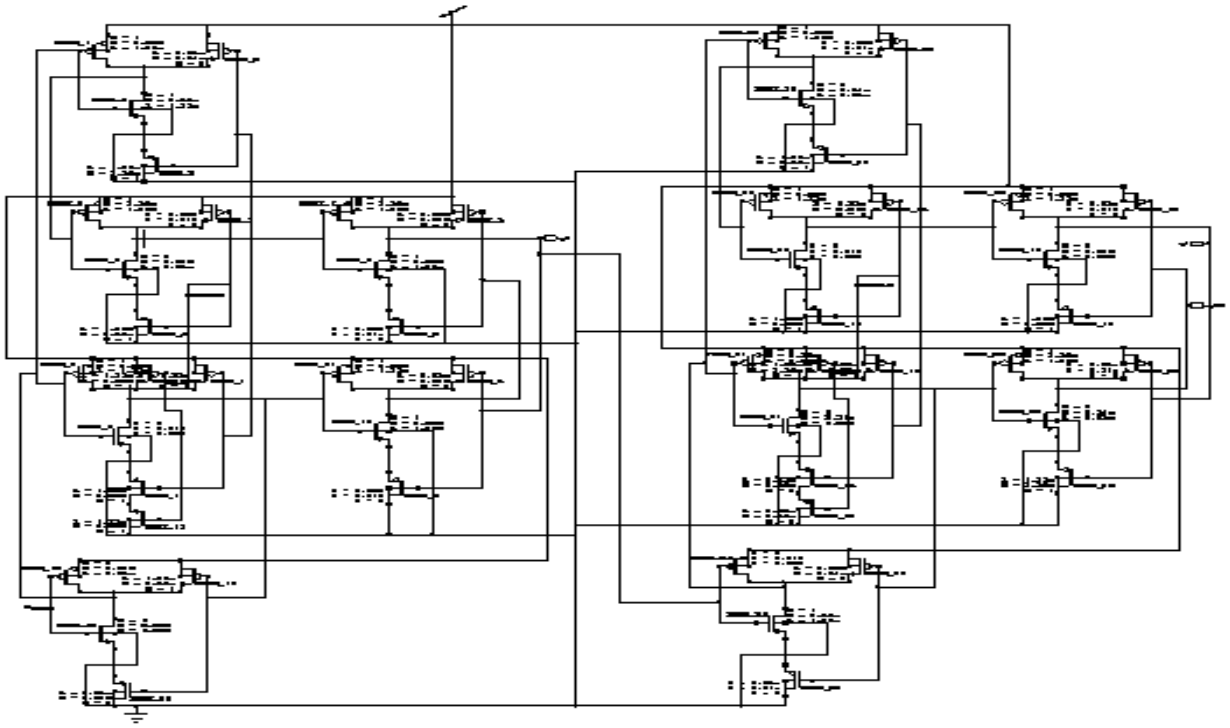

Figure 3 Schematic diagram of Conventional 2-Bit SISO Shift Register using CMOS

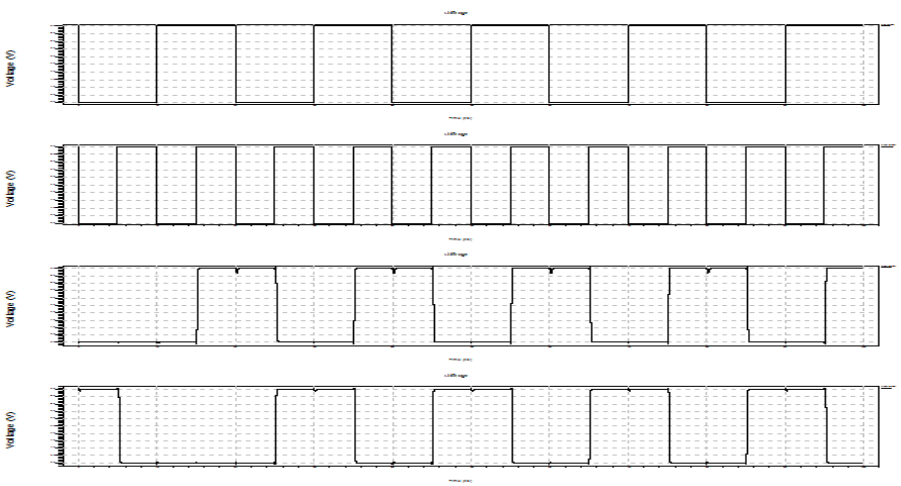

Figure 4 Output waveforms of conventional 2-Bit SISO Shift Register

V. PROPOSED 2-BIT SISO SHIFT REGISTER USING MTCMOS TECHNIQUE

To get the proposed design, we added a PMOS transistor that connects VDD and the circuit and forms a virtual power supply and a NMOS transistor that connects VSS and circuit and forms a virtual VSS. An inverter is designed; using it we give the sleep signal directly to PMOS and its inverted output to the NMOS. Proposed 2-bit SISO shift register is shown in Figure 5.

The sleep transistor is controlled by a sleep signal that can be used to switch on and off the device. The PMOS sleep transistor can be called as "header switch" as it connects VDD supply to the circuit and the NMOS sleep transistor can be called as "footer switch" as it connects VSS supply to the circuit.Taking d as the input, clk as the clock input, q1 as the MSB and q0 as the LSB, we got the results as shown in Figure 6 for 2-Bit SISO Shift Register using MTCMOS technique.

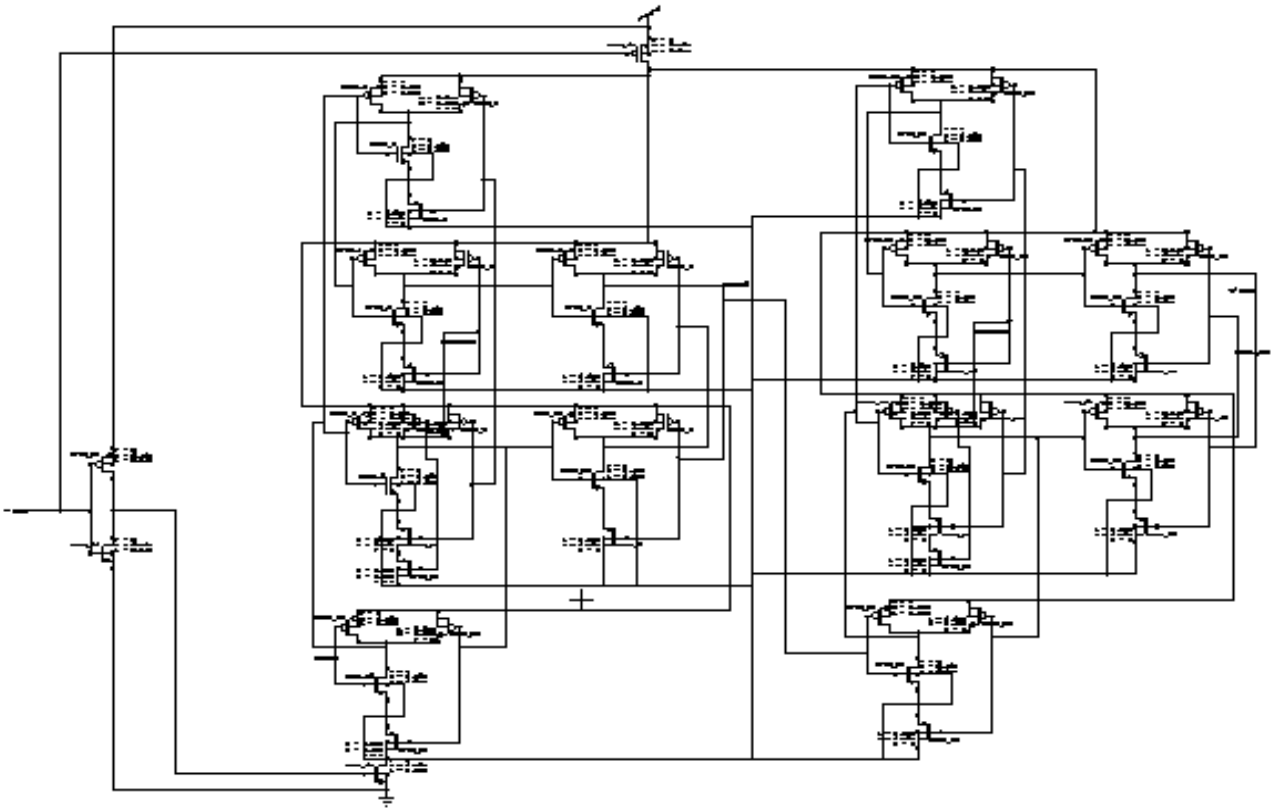

Figure 5 Schematic Diagram of Proposed 2-Bit SISO Shift Register using MTCMOS.

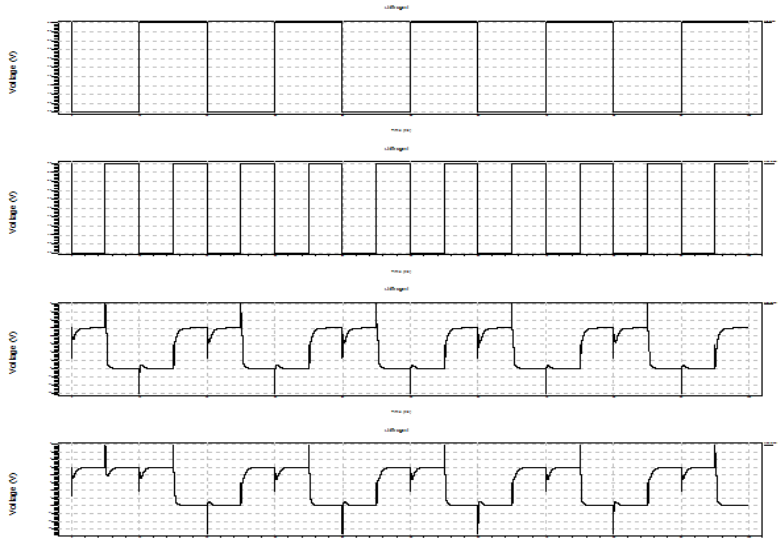

Figure 6 Output waveforms of proposed 2-Bit Shift Register

VI. IMPLEMENTATION OF 2-BIT BINARY INCREMENTER

The Binary Incrementer increases the value stored in the register by '1'. For this implementation it simply adds '1' to the existing value stored in the register. For this implementation we need 'n' half adders to add 'n' number of bits. The storage capacity of the register is to be incremented. Here in the below example we are using two half adder to get 2-bit incrementer. The carry of the first half adder is used as input for the second half adder.

The schematic diagram of Binary incremented is shown in Figure 7 and its out responses are shown in Figure 8

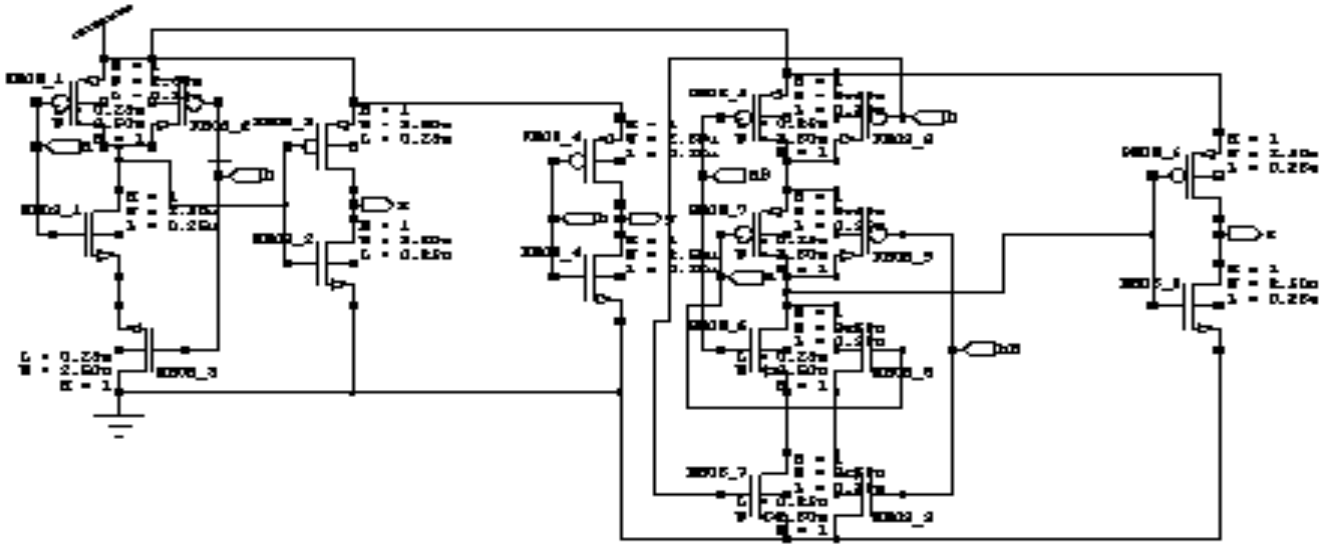

Figure 7 Schematic diagram of Conventional 2-bit binary incrementer using CMOS

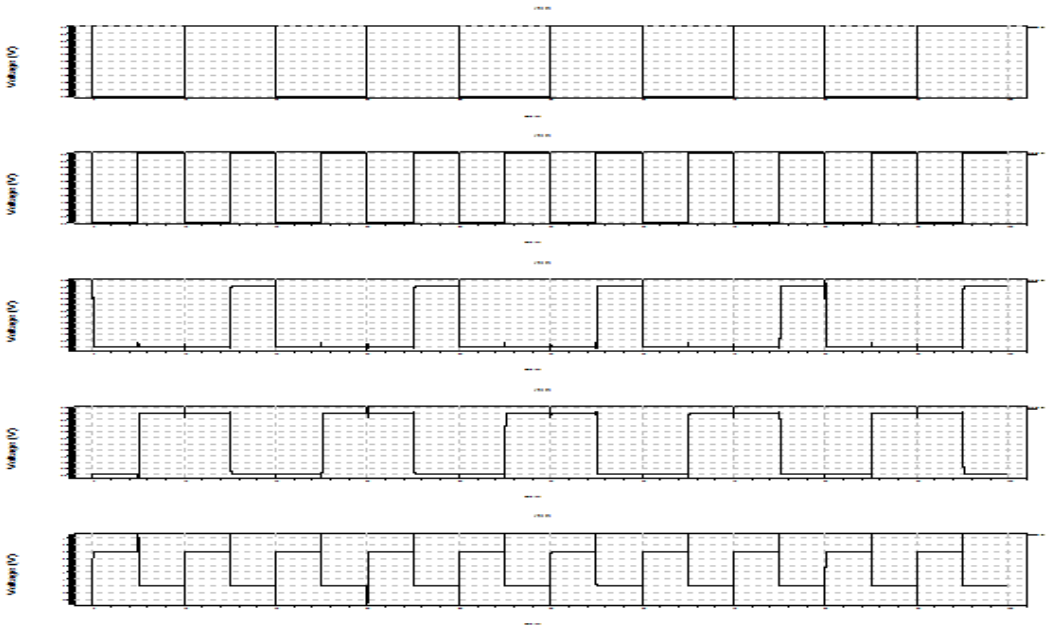

Figure 8 waveforms of conventional 2-bit binary incrementer using CMOS

Here we propose the 2 bit incremented using MTCMOS method. The schematic diagram is shown in Figure 9 and corresponding waveforms were shown in Figure 10

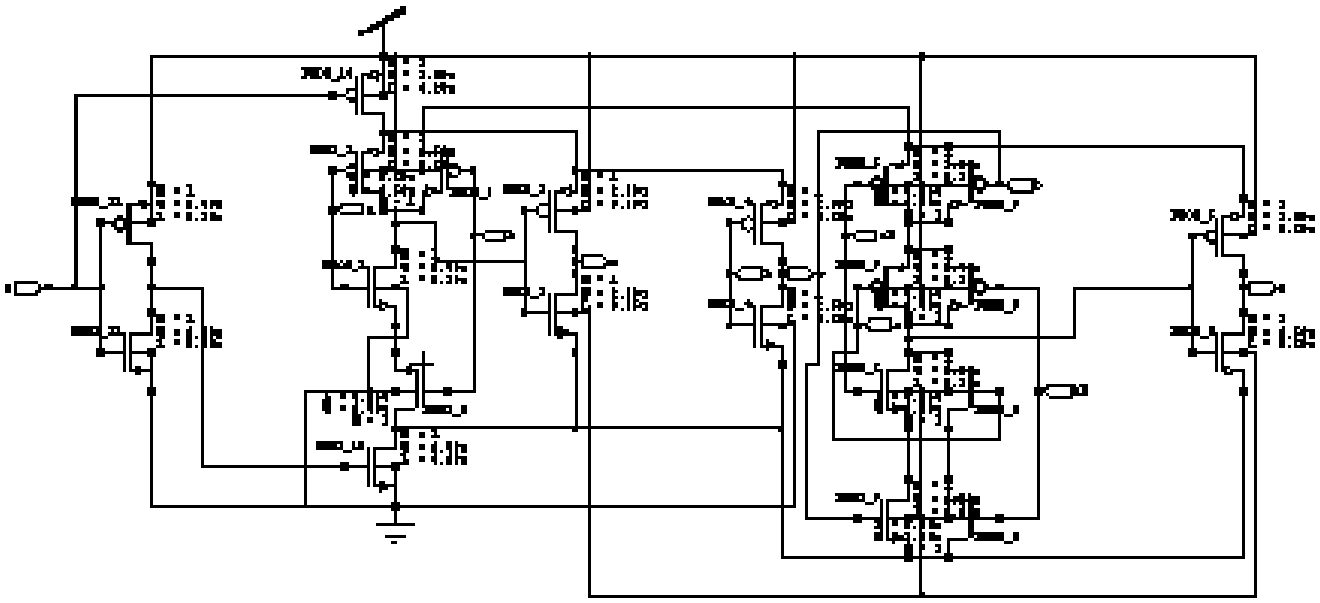

Figure 9 Schematic diagram of proposed 2-bit binary incrementer using MTCMOS

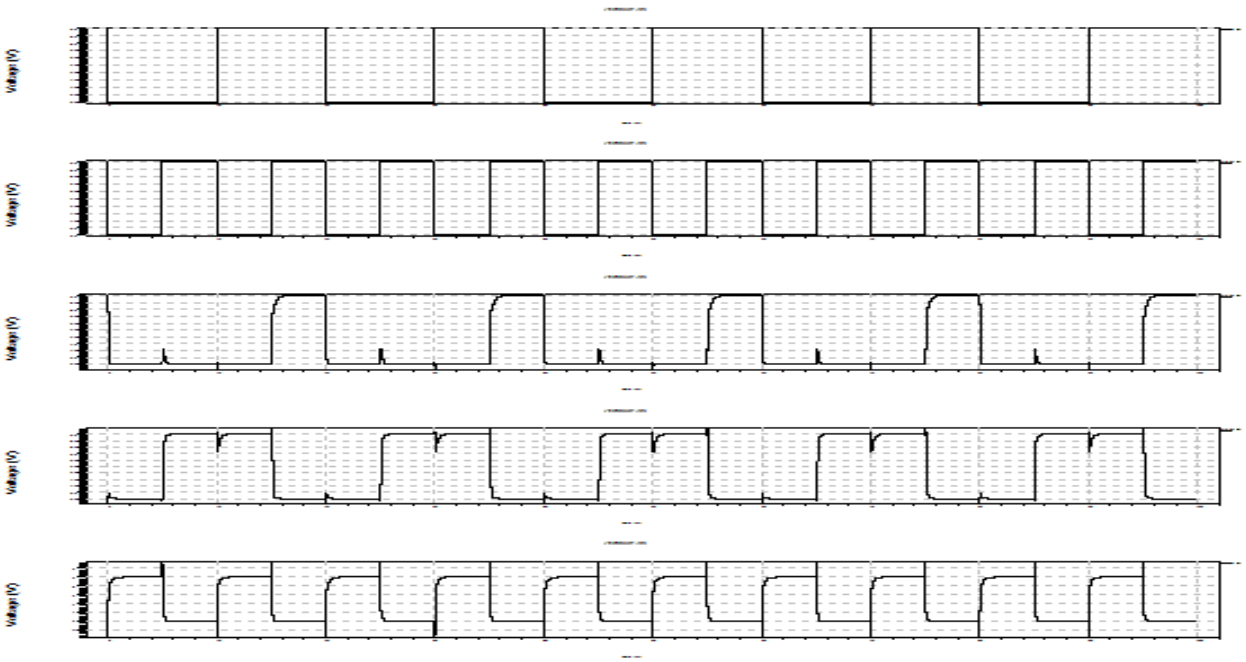

Figure 10 Output waveforms of proposed 2-bit binary incrementer

VII. RESULTS AND CONCLUSION

We have analyzed the power consumption of different logic circuits like different logic gates, adder, subtractor circuits as well as incrementer, D flip flpp and shift register. From the below Figure 11, it is clear that, MTCMOS design style will be consuming less power as compared to CMOS.

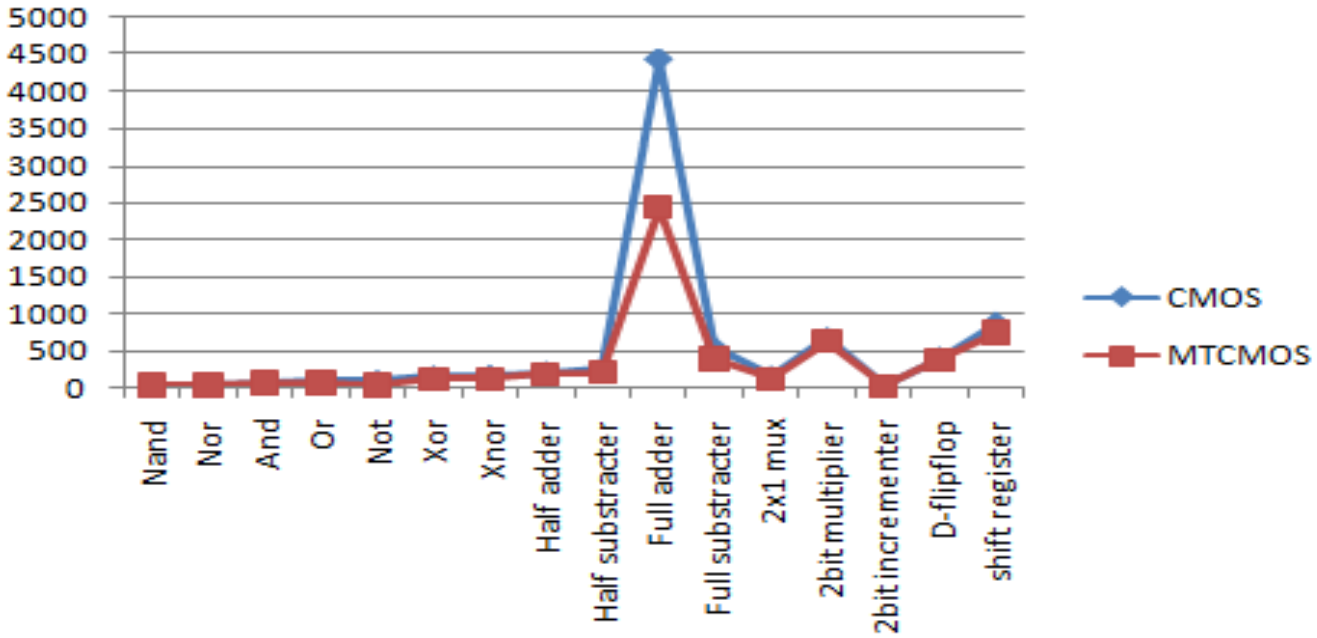

Figure 11 Difference in power consumption of various CMOS and MTCMOS Circuits

In this paper we concentrated on the leakage current analysis and it can be reduced using the MTCMOS technique. The proposed technique is associated with different threshold transistors to build the CMOS circuits. All the circuits are designed using 250nm technology and operated with supply voltage. In this the total average power is decreased because of it's reduction in leakage currents using MTCMOS. As this technique deals with leakage current, we should always take care of the temperature.

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