Comparative Study on Five and Nine Level MLI for Percentage THD Reduction

[1]Shraddha S. Lohakare, [2]Dr. Pravin M. Sonawane
School of Electrical Engineering
Sandip University, Nashik, Maharashtra

Abstract- *Renewable energy conversion systems has the main focus of many researches due to its promising potential of future electricity and advantages. Multilevel inverters(MLI) play a vital role in power conversion. The three different topologies, diode-clampedinverter, capacitor-clampedinverter and cascaded h-bridge multilevel inverter are widely used in these multilevel inverters. Among these, cascaded h-bridge multilevel inverter is more suitable for photovoltaic applications since each photo voltaicarray can act as separate DC source for each h-bridge module.This paper presents a comparison of 3-phase cascaded h-bridge 5-level and 9-level multilevel inverters for grid connected photovoltaic application using phase shifted pulse width modulation scheme.*

Multi-level inverters are basically used for high power applications as it helps in getting improved output waveform, nearly sinusoidal. As the levels obtained by multilevel inverters increased, harmonic content reduced but with this meritthere are certain problemsoffered by it. So to study this trade-offsthe theoretical study made in this paper considers comparison of grid connected 5-level and 9-level cascaded h-bridgemulti-levelinverters.

Keywords- Multi-level Inverter, H-Bridge Inverter,

INTRODUCTION

Multilevel inverters have more attention in the field of high voltage and medium power applications due to theiradvantages, such as low voltage stress on power semiconductor devices, low harmonic distortions, good electromagneticcompatibility, reduced switching losses and improved reliability on fault tolerance. Therefore, the multilevel inverters also have lower dv/dt ratio to prevent induction or discharge failures on the loads. Recently low voltage applications also hasbeen studied to apply the multilevel inverters for high efficiency such as in the uninterrupted power supply (UPS) andpower inverter for solar photovoltaic system (PV).

Recently, the multilevel converter is widely applied in the industries because the demand to operate switching, power converters in high power application has the development continuously. The ability of multilevel converters to operate at high voltages of the AC waveforms has low distortion, high quality and high efficiency. However, the multilevel converter technology has improved efficiency by employing various controls to achieve the high efficiency and maximize to save energy. In this paper, the topology presented nine-level diode-clamp inverter and principle are implemented to control the output waveform approaching to the sine-wave as close as possible. A nine-level PWM inverter to reduce the Total Harmonic Distortion (THD) of the inverter output voltages for three-phase induction motor drive are presented.

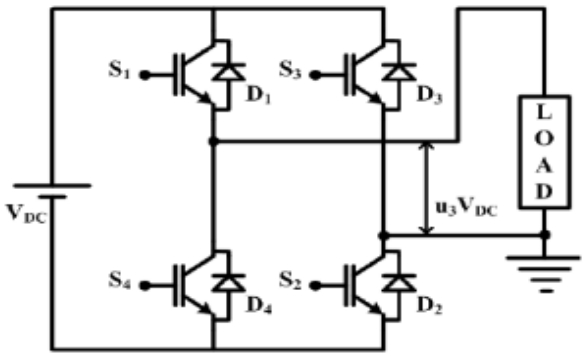

Fig-1-Single Branch of H Bridge Inverter

Inverters are needed to convert the direct current electricity produced into alternating current

electricity required for loads. Multilevel inverter promises a lot of advantages over conventional inverter especially for high power applications. Some of the advantages are that the output waveform were improved since multilevel inverter produced nearly sinusoidal output voltage waveforms, hence the total harmonic distortion is low, reduced switching losses and the filter needed to smooth the output voltage is small; hence, the system is compact, lighter and much cheaper.There are different types of multilevel circuits involved.

The first topology introduced was the series H-bridge design followed by the diode clamped converter, which utilized a bank of series capacitors. The H-Bridge inverter is as shown in the fig. 1.Here the switches s1 and s2 are used to get positive voltage and switches s3 and s4 are used to get negative voltage.By using this single h-bridge we get only three levels (0,+V,-V) of voltage. To get more levels we should connect these h-bridge inverters in series.

The flying capacitor design in which the capacitors were floating rather than series-connected is also used by many configuration designers. Another important multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire DC voltage, but share the load current uniformly.

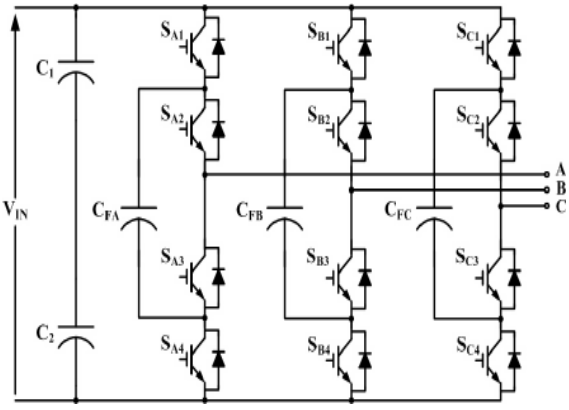

Fig 2- Flying Capacitor Inverter

The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

DESIGN OF THREE PHASE FIVE-LEVEL INVERTER

As we already discussed to get more than three levels of voltage we should connect h-bridge inverters in series as shown in the figure above. The main advantages of the cascaded h-bridge multilevel inverters are its ability to offer improved regulation of the dc bus voltage and its structure, which is modular to simplify control as well as maintenance.

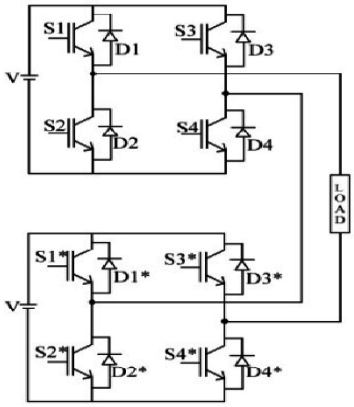

Fig 3- Cascaded Multilevel Inverter

From the figure, one can observe that for three-phase inverter three sets of five level inverters are used.

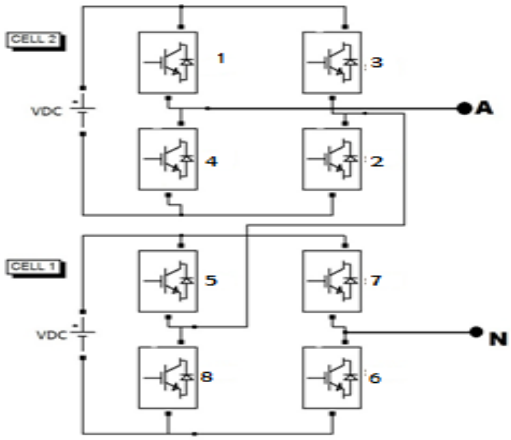

Fig 4- Five-Level Cascaded H-Bridge Inverter per phase

The cascades single phase H-Bridge multilevel inverter uses different single phase h-bridge ones, each with an independent dc voltage source. The different legs of a cascaded h-bridge multilevel inverter can have different levels of voltage that are switched by the individual single phase h-bridge inverters, where three levels of voltage can be obtained. The ac outputs of the single phase h-bridge inverters in each leg are connected in series such that the synthesized voltage waveform is the sum of the h-bridge inverters outputs.

Table 1 shows the switching sequence of five level inverter, where E = VDC. Same switching sequence is applicable for all phases with 120 degree phase shift.

V	1	2	3	4	5	6	7	8
2E	1	1	0	0	0	0	0	0
E	1	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0
-E	0	0	1	1	0	0	0	0
-2E	0	0	1	1	0	0	1	1

DESIGN OF THREE PHASE NINE-LEVEL INVERTER

These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The main disadvantage of the conventional n Level cascaded H-bridgeis that when the voltage level increases, the number of semiconductor switches increases and also the source required increases. There arefew topology where the number of switches are less than the expected number of switches required and also the number of sources.

MODULATION TECHNIQUES

Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have controlled output voltage. There is variety of modulation techniques available. Basically the control technique can be classified as the pulse width modulation which is considered as the most efficient method. The main advantage of PWM is that power loss in the switching devices is very low.When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero.

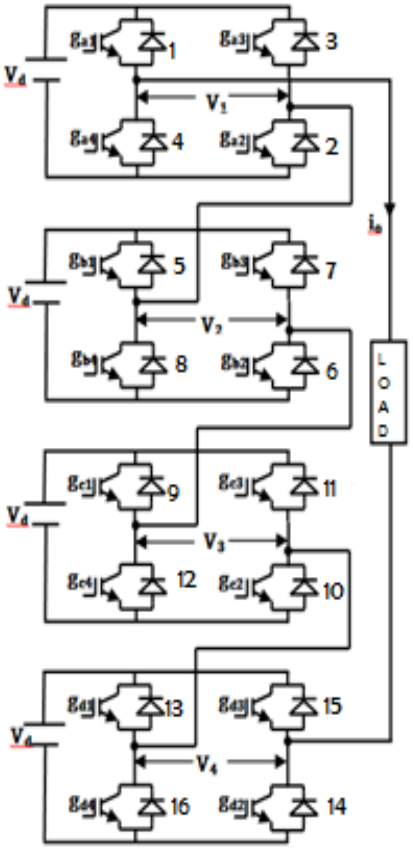

Fig 5- Nine-Level Cascaded H-Bridge Inverter per phase

In this inverter, the sinusoidal pulse width modulation is going to use. In the Sinusoidal pulse width modulation scheme, as the switch is turned on and off several times during each half-cycle, the width of the pulses is varied to change the output voltage. Lower orderharmonics can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle. Higher order harmonics may increase, but these are of concern because they can be eliminated

easily by filters. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter. The modulation index, M of the proposed multilevel inverter is defined by,

$$M = ½ (V_{ref} / V_{cr})$$

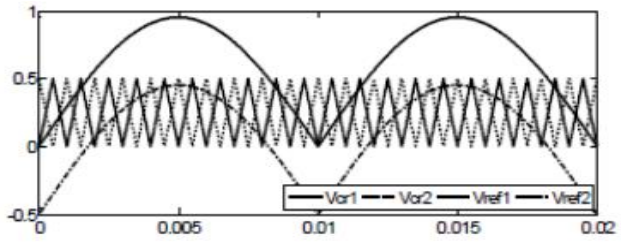

Fig 6- Multicarrier Phase shifted PWM

When the voltage reference is between 0<Vref≤½, Vref1 is compared with the triangular carrier and alternately switches S1 and S3 while maintaining S5 in the ON state to produce either ½Vdc or 0. Whereas, when the reference is between ½<Vref≤1, Vref2 is used and alternately switches S1 and S2 while maintaining S5 in the ON state to produce either ½Vdc or Vdc. As for the reference between –½<Vref≤0, Vref1 is used for comparison which alternately switches S1 and S2 while maintaining S4 in the ON state to produce either –½vdc or 0. For a voltage reference between –1<Vref≤–½, Vref2 is compared with the carrier to produce either –½Vdc or –Vdc alternately switches S1 and S3, maintaining S4 in the ON state. It is noted that two switches, S4 and S5, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency. This allows the dc voltage to be switched at a low frequency so as to reduce the switching losses.

DISCUSSION ON INVERTER OUTPUT

As shown in Figure 2, if Two H-Bridges are cascaded then 5 level output is obtained. Though practically type of switches used do make difference in output but in simulations no major difference is observed.In this 5 level design, MOSFET switch is used. Figure below shows 5 level output voltage where V_{dc} is 20V for each bridge, thus DC voltage is equal for both bridges. MOSFETs are switched at approximately 10^0 and 56^0 to obtain V_{dc} and $2V_{dc}$ as the output, accordingly rest of switching takes place.

As per figure 5, design of 9-Level multilevel inverter is shown. Switches are switched at approximately 7.5^0, 19.1^0, 33.5^0 and 51.6^0 to obtain 0, V_{dc}, $2V_{dc}$ and $3V_{dc}$ and accordingly rest of switching takes place.

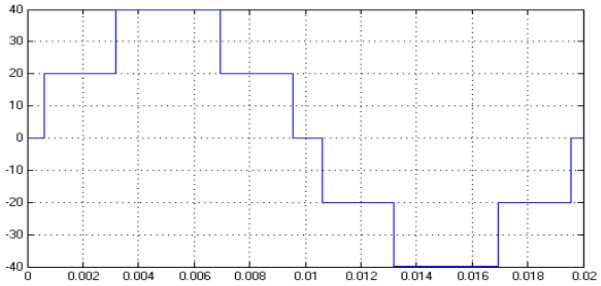

Fig 7- Voltage output profile of 5 level inverter

Fig. 9 shows 9 level output voltage where output levelsare obtained by addition or subtraction of applied DC voltage i.e. 10V and 30V. Thus output can be optimized with different switching angles and accordingly THD will change.

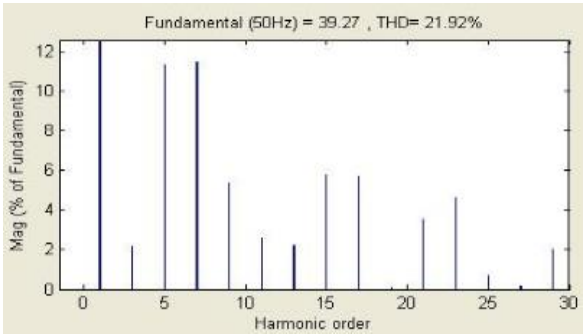

Fig 8- THD profile of 5 Level Inverter

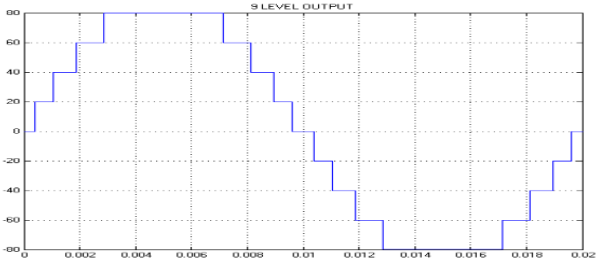

Fig 9– Output of 9 Level Multilevel inverter

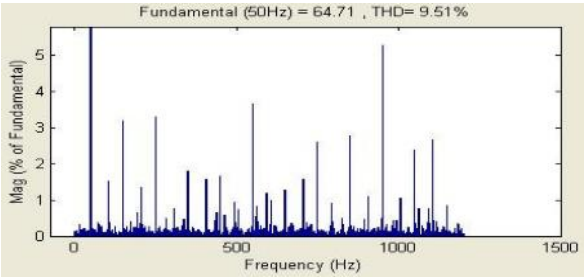

Fig 10- THD profile of 9 Level Inverter

CONCLUSION

Doing an absolute comparison of 5-level and 9-level output, it is seen that the 9 level inverter is better as it gives low THD with the same number or reduced number of switches.

References

[1] Nurul AisyahYusof, Norazliani Md Sapari, Hazlie Mokhlis Jeyraj Selvaraj, "A Comparative Study of 5-level and 7-level Multilevel Inverter Connected to the Grid", IEEE International Conference on Power and Energy, 2-5 December 2012

[2] Mr. V. Praveen, Mr. A. V. Suresh, "Analysis of Seven and Nine Levels Multilevel Inverters for Energy Saving in Induction Motor Drive for VTL Application", Intl. Journal of Electrical and Electronics Research, Vol. 2, Issue 4, pp-65-73, October – December, 2014

[3] Z. Pan, F.Z. Peng, K. Corzine,V.R. Stefannovic, J.M. Leuthen,and S. Gataric, "Voltage balancing control of diode clamped multilevel rectifier/inverter systems", IEEE Trans. Ind. Appl., vol. 41, no. 6, pp. 1698–1706, Nov./Dec. 2005.

[4] S. Ali Khajehoddin, AlirezaBakhshai, and Praveen K. Jain, "A Simple Voltage Balancing Scheme for m-Level Diode-Clamped Multilevel Converters Based on a Generalized Current Flow Model," IEEE trans. power electron, vol. 23, no. 5, September 2008.

[5] Rodriguez, J.-S. Lai, and F. ZhengPeng, "Multilevel inverters: A survey of topologies, controls, applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 655–667, Feb. 2012.

[7] Datar Singh Nathawat, Vishnu Goyal, "A Symmetric 9 - Level Multilevel Inverter with Minimum Number of Device,Intl. Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol-6 Issue-1, June 2016

[8] S.J. Park, F.S. Kang, M.H. Lee, C.U. Kim, "A New Single-Phase Five-Level PWM Inverter Employing a Deadbeat Control Scheme", IEEE Transactions on Power electronic, Vol. 18, No. 3, May 2003, pp. 831-843.

[9] K. Panda, Y. Suresh, "Research on Cascade Multilevel Inverter with Single DC Source by using Three-phase Transformers", Electrical Power and Energy System, Vol 40, March 2012, pp. 9-20.