Optimized CMOS Semi Custom Design of SRAM Cell

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Abstract— In this paper SRAM cell has been designed on 90nm technology. The two designs for SRAM cell have been proposed namely fully automatic and semi custom. In fully automatic design is proposed where inbuilt active devices are used along with auto routing and placement. In semi custom design inbuilt active device are used along with optimized manual routing and placement. In fully automatic approach proposed schematic is design with DSCH and it equivalent layout is created using Micro-wind. In case of semi custom design, optimized layout is created with Micro-wind. It can be observed from simulated results that area is improved by 74% and power has been observed as 27% in case of semi custom design as compared to fully automatic.

Keywords- *SRAM cell, SRAM chips, Low Power, Power dissipation, Leakage Currents, Very Large Scale Integration (VLSI)*

I. INTRODUCTION

SRAM (Static random access memory) is a static memory used for the storing the data in cache memory of various electronic systems such as CPU. Static RAMs are used for processors due to their huge storage volume. Low power on-chip memories is nowadays an uprising research topic as they state for nearly 50% of the overall CPU power dissipation, even for extremely power-efficient designs. The static power dissipation is becoming fractions of the total power and is calculated for future increase because as leakage current increases exponentially [1]. Leakage power dissipation is to control the overall power consumption. Due to sub-threshold leakage power, there is an increase in the leakage power. Some techniques are used to reduce the leakage power such as stack, sleep approach, sleepy keeper, leakage feedback techniques and which reduces leakage current. Each VLSI techniques are used for the reduction of power [1]. Recent and important trend for operating memory is applying lower supply voltage, by increasing the power in memory design [2]. The major problem while dealing with SRAM is their leakage power and leakage current which needs to be minimize, while retaining their data from standby mode for a particular period of time [3]. In this paper, we are analyzing the area and power consumption by automatic design and semi customized design of SRAM cell, designed by using micro-wind and DSCH.

II. SRAM

Static Random Access Memory (SRAM) is the most important memory technologies. They are found universally with microcontrollers and microprocessors on the same die. Device scaling is used in SRAM design. Low power SRAM design is difficult as it takes a large part of total power and area for high performance processors. The technique of CMOS technology has important impacts on SRAM cell .It consists of 2 PMOS and 2 NMOS pull up and pull down transistors respectively in form of two cross coupled inverters and to access SRAM cell in reading and writing operation, 2 NMOS transistors are to be used. For transmitting data in reading and writing operation, both the bit lines (BL and BL_b) will be used. BL and BLB has supply of data signal and its inverse. VR and VL will be used as storing points as high and low [1]. SRAM consists of many designs like 6TSRAM cell, 7TSRAM cell, 8TSRAM cell, 9T SRAM cell but out of all, 6TSRAM cell is used widely as it stores 1-bit of data [2]. We can design 6T SRAM cell by inverters working in 180nm, 120 nm, 90 nm, 70 nm, 50 nm, 45 nm. Here, we are working on 90nm technology. We can design 6T SRAM cell by using inverters also. Following is the basic diagram of 6T SRAM cell using inverter (Figure 1) and the inverter will be formed by using PMOS and NMOS (Figure 2).

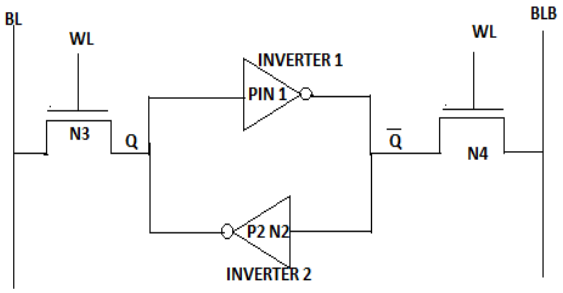

Figure 1.6T SRAM cell

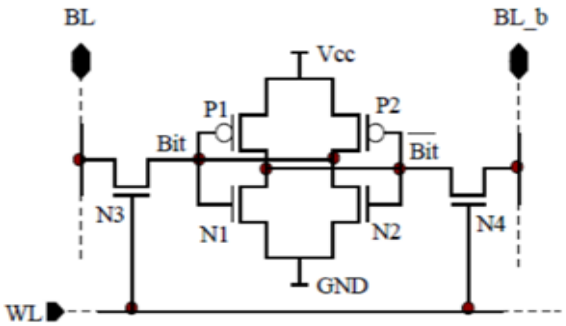

Figure 2.SRAM cell [1]

III. SCHEMATIC DESIGN

DSCH is a schematic editor and simulator used for designing of the logic circuits. It is user friendly as we could easily detect the faults in circuit designing. So first, we have to design SRAM cell in DSCH software .After making the layout of sram cell, we will make a verilog file which will compile in micro-wind. The execution of verilog file of sram cell will make a VLSI layout (stick diagram) in micro-wind. Following are the diagrams of particular steps. Now, the first simulation will be done by inverters and then by using NMOS and PMOS.

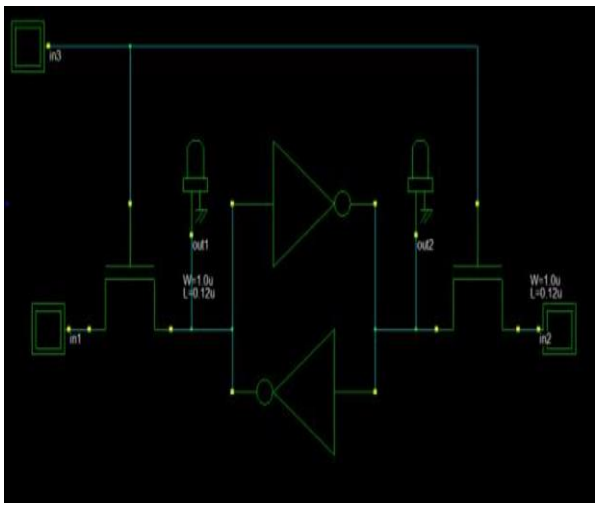

Figure 3.Gate level 6T SRAM cell Design

Now, we will perform the same design by using NMOS and PMOS. We will design that schematic layout in DSCH.

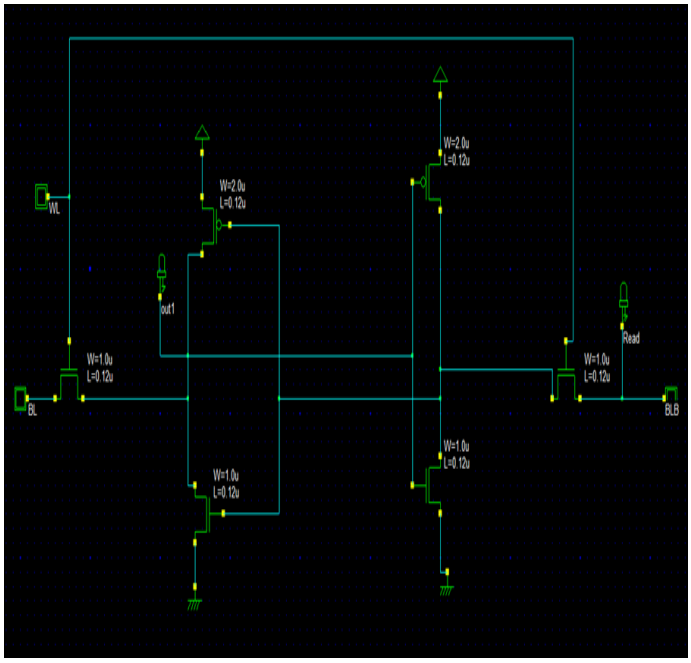

Figure 4.Transistor level 6T SRAM cell Design

Verilog is the only design unit and is useful for writing generic verilog code in different file .Now, we will compile the design by using verilog file and will open it in micro-wind for execution of the design.

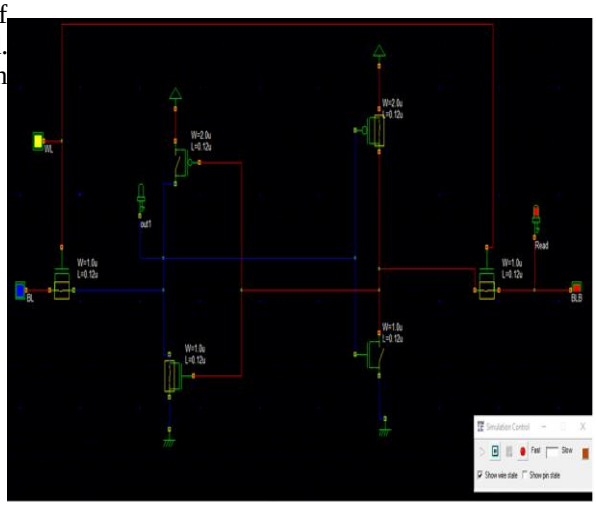

Figure 5. Simulation of the design

We will get a layout of 6T SRAM cell automatically.

Now, micro-wind will compile the verilog file of design. The Verilog file will be open in micro-wind to check the stick diagram of 6T sram cell.

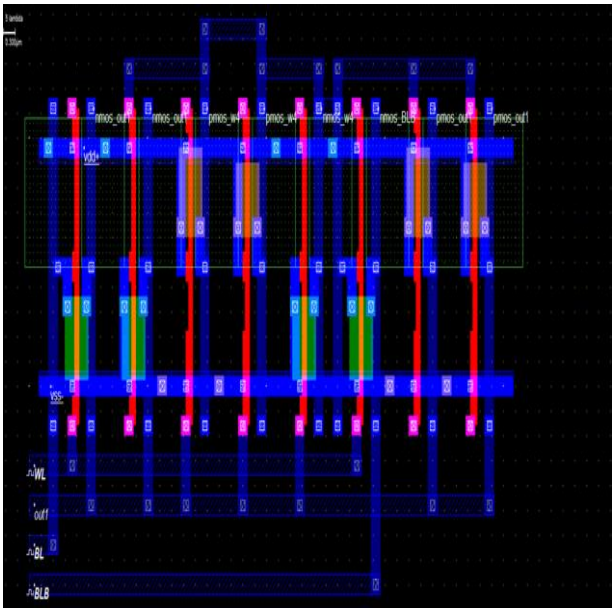

Figure 6.Micro-wind layout

The output so formed by simulating the layout of 6T SRAM cell is as follows. The output graph is between voltage and time. It shows the output between BL and PMOS out1. It

implies that when BL is high, BLB and WL is low , the output so obtained will be low only .

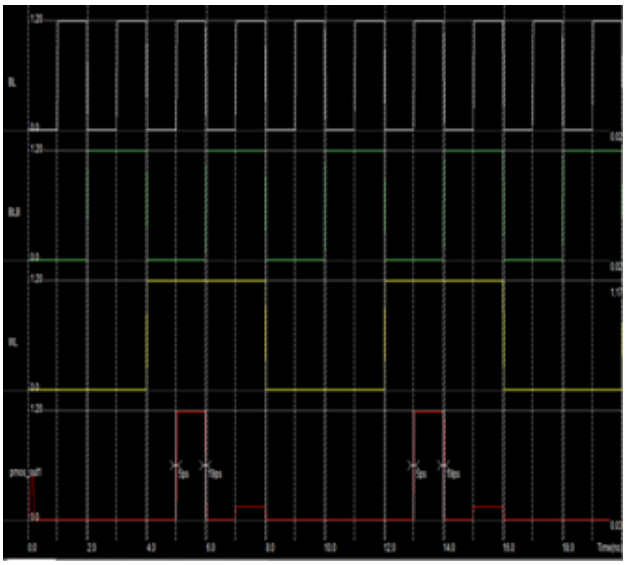

Figure 7.Output of the layout

This output graph shows how BLB, BL and WL changes with the input power given to the design. The output power is 0.129mW, with the time scale of 20ns . Display includes delay and bus value both.

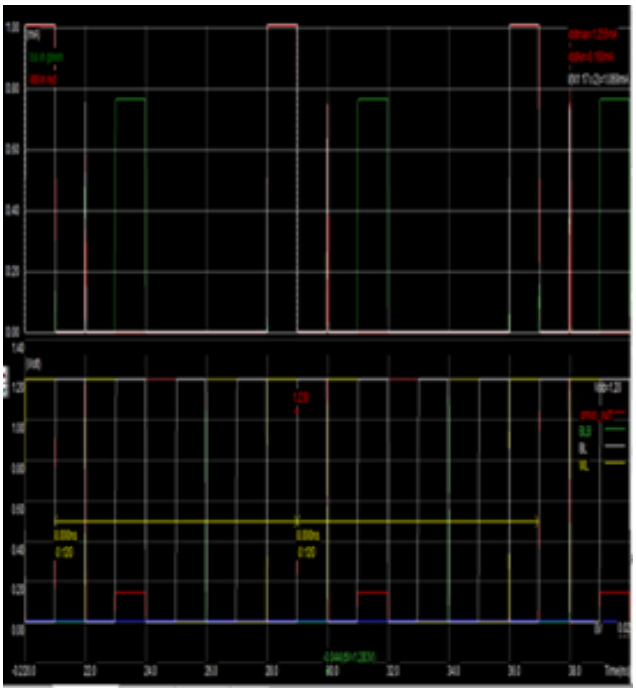

Figure 8.Simulation of layout

The output will include the total number of PMOS, NMOS, electrical nodes and area of the automatic generated layout.

The total surface covered by auto generated design is 87.7μm^2 .Total number of NMOS is 2 and PMOS is 4. Next, we will consider all the other parameter that include per element length , width for example the length of metal 1,metal 2, polysilicon, etc. Now, the supply voltage, temperature, I/O supply and the simulation length of the design are as follow. In auto generated design, we have fix I/O supply as 2.50V , temperature is 27°. In simulation on layout , redraw each 2 steps and add noise on input, the value of RMS is 0.10 V.

IV. SEMI CUSTOMIZED DESIGN

In semi customized design, we select the components by using drag and drop method to make the layout of 6T sram cell. Each layer/metal /component has its own thickness and follow λ rules. We use directly NMOS and PMOS from toolbar and form 6T SRAM cell by using polysilicon , metal , contacts. Following diagram shows the output so formed by semi customized design. After making the layout of the design we will run the design and after simulation we will get the following results . The ouput so formed will be between q and qbar. It is clear from the graph that when q has output high ,q bar is low . This shows that our design output is correct. Here, the output obtain at time scale of 5 ns. Here , the semi custom design is basically formed when it takes direct PMOS and NMOS from the library for the simulation , no need to make or design PMOS or NMOS by taking different layers, and then that circuit will be known as fully customized design. Following is the semi customized layout of 6T SRAM cell . It shows different layers , and how the PMOS and NMOS is attached to form the layout .

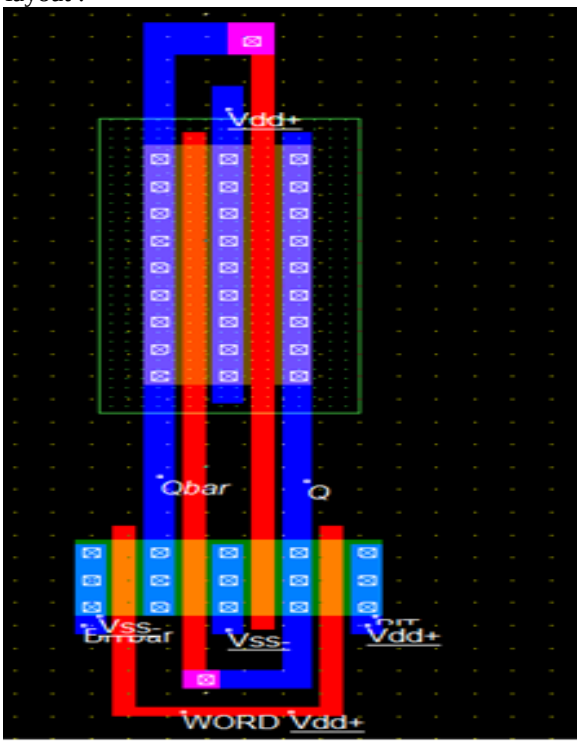

Figure 9.Semi design Layout of 6T SRAM cell

Now the results of semi customized design of 6T sram cell. In terms of area and power consumption are as follow.

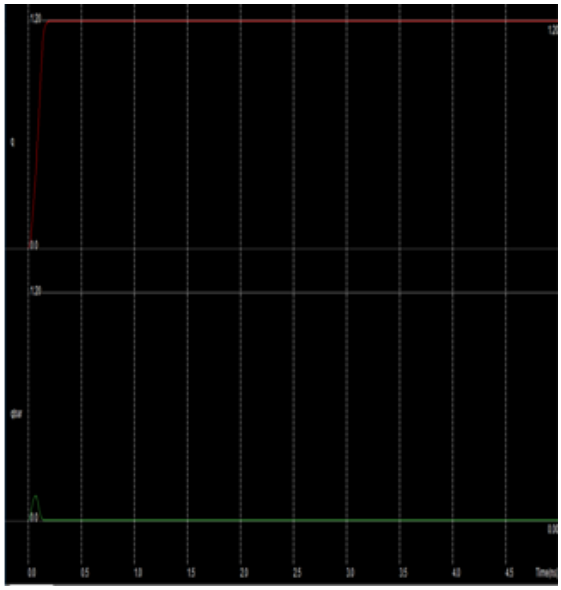

Figure 10.Voltage v/s Time output

Here, we can see that the area consumption is less than auto developed design. The total surface area so covered is 22µm^2. Now the power consumption . The total power consumed to obtain semi customized design of 6T SRAM cell is 3.590mw. So we can conclude that the power we obtain is much higher that we obtained from automatic generated layout. Following is the output of supply voltage , temperature , I/O supply , etc.

V. RESULTS

Finally the comparison between semi and auto customized design of 1-bit 6T sram cell by using DSCH and micro-wind is as follows.

Parameters	**Auto customized**	**Semi customized**
Width	12.6µm	2.4µm
Height	7.0µm	9.2µm
Surface	87.7µm^2	22 µm^2
Supply	1.20V	1.20V
I/O supply	2.50V	2.50V
Temperature	27°c	27°c
Simulation length	20ns	5ns
Power	0.129mW	3.590 mw

VI. CONCLUSION

Finally, after the simulation of both semi and auto customized design of 6T SRAM cell , we conclude that thought the area of semi customized is less than auto developed , whereas the power consumption of semi design increased . The total area will be reduced by 74% of semi custom with respect to fully customized design and the power will be increased by 27%.

VII. FUTURE WORK

Future research work could be done to reduce the power consumption. It could be achieved by using metal instead of polysilicon for connection the gates .By this, the power will also get reduce, and we are already getting the area. So the upcoming research will include both the reduction of area and power by using automatic and semi customized design of 6T SRAM cell.

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