Implementation of 64 Bit KoggeStone Carry Select Adder with BEC for Efficient Area

B.Tapasvi[1], K.Bala Sinduri[2], I.Chaitanya Varma[3], N .Udaya Kumar[4]
[1]*M.Tech Student, Department of ECE, SRKR Engineering College, Bhimavaram, India*
[2]*Assistant Professor, Department of ECE, SRKR Engineering College, Bhimavaram, India*
[3]*B.Tech Student, Department of ECE, SRKR Engineering College, Bhimavaram, India*
[4]*Professor, Department of ECE, SRKR Engineering College, Bhimavaram, India*

***Abstract*—** Carry Select Adder (CSLA) is one of the faster adder used in many data-processing processors to perform fast arithmetic functions. The speed of operation of such an adder is limited by carry propagation from input to output. This paper discusses about the implementation of linear Carry Select Adder with Kogge Stone Adder. The Kogge Stone parallel approach will give option to generate fast carry for intermediate stages. From the structure of linear CSLA it is clear that there is scope for reducing the area in CSLA by using Binary to Excess 1 converter. 64 bit linear CSLA architecture with Kogge stone is implemented which reduces area with slight increase in delay when compared with Regular Linear 64 bit CSLA architecture. Simulation and Synthesis are carried on Modelsim 6.3 and Xilinx ISE 12.2.

Keywords*—Kogge Stone Adder (KSA), Binary to excess-1 Converter (BEC),Carry Select Adder(CSLA).Ripple Carry Adder (RCA),Regular Carry Select Adder(RCSLA).*

I. INTRODUCTION

Binary addition is the most fundamental arithmetic operation. It has been ranked the most extensively used operation among a set of real-time digital signal processing benchmarks from application-specific DSP processors to general-purpose processors. In particular, carry-propagation adder (CPA) is frequently part of the critical delay path limiting the overall system performance due to the inevitable carry propagation chain. The speed of addition is limited by the time required to propagate a carry through the adder. The CSLA is used in many computational systems to moderate the problem of carry propagation delay which compromises between RCA and CSLA. The CSLA requires dual RCAs in which RCA with "cin=1" replaced by BEC improves area. The CSLA using variable block sizing, the delay can be further reduced. To increase the speed of CSLA, parallel prefix adder is used instead of RCA. The kogge-stone adder has low critical path and maximum fan-out. The high speed regular and modified CSLA is designed using kogge-stone adder by replacing RCA with "cin=0".

The details of ripple carry adder, multiplexer, binary to excess -1 converter and carry select adder discussed in Section II, the complete functioning of Kogge-Stone Adder is discussed in section III, The implementation of High Speed Proposed CSLA architectures in Uniform and Variable block size is described in section IV and V. The performance and simulation results are presented and discussed in section VI.

The CSLA is used in many computational systems design to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. It uses independent ripple carry adders (for Cin=0 and Cin=1) to generate the resultant sum. However, the Regular CSLA (RCSLA) is not area and speed efficient because it uses multiple pairs of Kogge Stone Adders (KSA) to generate partial sum and carry by considering carry input. The final sum and carry are selected by the multiplexers (mux). Due to the use of two independent KSA the area will increase which leads an increase in delay. To overcome the above problem, the basic idea of the proposed work is to use n-bit binary to excess-1 code converters (BEC) to improve the speed of addition [1]. This logic can be replaced in KSA for "Cin=1" to further improves the speed and thus reduces the delay. Using Binary to Excess-1 Converter (BEC) instead of KSA in the RCSLA will achieve lower area, delay which speeds up the addition operation of Modified CSLA (MCSLA). The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure because the number of gates used will be decreased.

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area**.** Parallel prefix adders can also be used to reduce the delay. Several examples of such adders have been published and there are many efficient implementations. Kogge and Stone scheme limit the lateral logical fan-out at each node to unity, but at the cost of a dramatic increase in the number of lateral wire at each level.

II. BINARY TO EXCESS-1 CONVERTER

The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation. This logic is replaced in KSA with "Cin=1". This logic can be implemented for different bits which are used in the modified design. The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA)

structure. As stated above the main idea of this work is to use BEC instead of the KSA with "Cin=1" in order to reduce the area and increase the speed of operation in the regular CSLA to obtain modified CSLA. To replace the n-bit KSA, an (n+1) bit BEC logic is required. The structure of a 5-bit BEC is shown in Fig.I and the function table of 5-bit BEC is shown in Table.I.

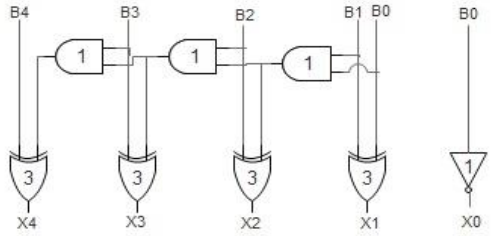

Fig.I. BEC to Excess 1 Converter for 5-bit.

Table.I: Function Table of the 5 bit BEC.

B[4:0]	X[4:0]
00000	00001
00001	00010
00010	00010
|	|
|	|
|	|
11111	00000

The Boolean expressions for the 5-bit BEC logic are expressed below.

X0 = not B0 (1)
X1 = B0 xorB1 (2)
X2 = B2 xor (B0 and B1) (3)
X3 = B3 xor (B0 and B1and B2) (4)
X4 = B4 xor (B0 andB1 and B2 and B3) (5)

The delay and area evaluation of the basic gates used in the Kogge Stone Carry Select Adder [2] are shown in the Table II. The delay and area calculations are done as follows, for example take multiplexer which has one not gate, one or gate and two and gates. All these three gates have one unit of delay and one unit of area each. So the multiplexer has three units of delay and four units of area as shown in Table.II. The basic structure of multiplexer is shown in Fig.II. Similarly area and delay of remaining gates are also calculated which are listed in Table II.

Table.II: Delay and Area Evaluation of KSCSLA

Design	Delay	Area
AND	1	1
XOR	3	5
2:1 MUX	3	4
Half adder	3	6
Full Adder	6	13

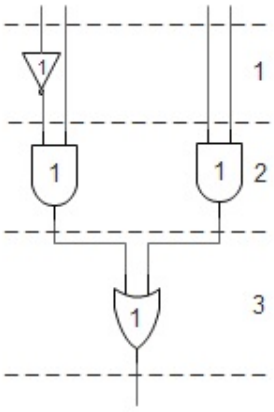

Fig.II: Delay and Area Evolution of MUX.

III. KOGGE STONE ADDER

The Kogge-Stone Adder is one of the fastest parallel prefix adder obtained from Carry Look Ahead (CLA) structure with focus on design time and is the common choice for high performance adders in industry. The parallel-prefix adder becomes more favorable in terms of speed due to the O(log2n) delay through the carry path compared to O(n) for the RCA. The arrangement of the prefix network specifies the type of the Parallel Prefix Adder. This comes at the cost of long wires that must be routed between stages. The tree also contains more PG cells; while this may not impact the area if the adder layout is on a regular grid, it will increase power consumption. Despite these cost, KSA is generally used for wide adders because it shows the lowest delay among other structures.

The complete functioning of KSA [3] can be easily comprehended by analyzing it in terms of three distinct stages:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

The carry equations of KS adder are shown below. The carry propagation delay of the adder is proportional to $\log_2(n)$ and the number of logic elements used is proportional to $n\log_2(n)$, where n is the number of bits used in addition. It is clear that for KS adder, area utilization is very large, even though it reduces the delay by a large amount.

$$g_0 = a_0 b_0 \quad (6)$$
$$p_0 = a_0 \; xor \; b_0 \quad (7)$$
$$c_1 = g_0 + p_0 c_{in} \quad (8)$$
$$c_2 = (g_1 + p_1 g_0) + p_1 p_0 c_{in} \quad (9)$$
$$c_3 = (g_2 + p_2 g_0) + p_2 p_1 c_1 \quad (10)$$
$$c_4 = (g_3 + p_3 g_2) + p_3 p_2 (g_1 + p_1 g_0) + p_3 p_2 p_1 p_0 c_{in} \quad (11)$$

IV. LINEAR CSA WITH KOGGE STONE

The structure of 64 bit Linear Kogge Stone Carry Select Adder is shown in Fig.III. It has eight groups of same size KSA. Each group consists of two identical 4 bit Kogge stone adders and one 10:5 multiplexer except first group which has single 4bit KSA only. In which we have given Cin=0 to one 4bit KSA and Cin=1 to another 4bit KSA. Depending upon the previous carry the selection of either

one of the 4bit KSA output is fed to the 10:5 multiplexer along with carry.

Methodology for delay and area evaluations are same for Kogge Stone Linear Carry Select Adder with Cin=0 and Cin=1. Depending upon the selection input i.e carry from previous group, final sum and carry differ in delays whereas Area evaluation for each group except group1 remains same.

Delay and area evaluation of each group [4]are represented in numerals within brackets specify the delay values. Steps involved during evaluation process are as fallows.

1) Group 1 has one set of Kogge Stone Adder. Based on the considerations of delay values shown in Table.III, the arrival time of selection input C4 (time = 8) of 10:5 mux is earlier than S3 (time = 9) and later than S4(time = 10).

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the KSA's. Thus, the delay of group3 to group8 are determined.

The sub groups involves in the single group of Linear 64-bit KSA are drawn below as Fig.III(a),Fig.III(b), Fig.III(c), Fig.III(d) respectively.

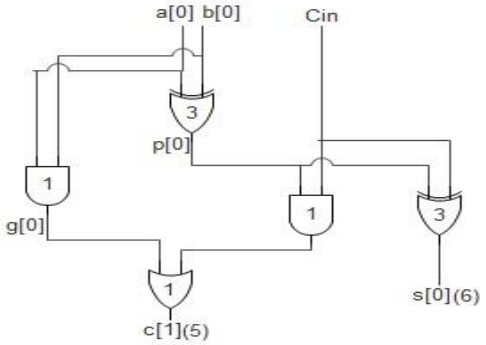

Fig.III (a).

The diagram shown in Fig.III(a). gives the s(0) and c(1) which has delays 6 and 5 respectively. For generating s(0) it requires two ex-or gates,2 and gates and 1 or gate. For generating c(1) it requires 1 ex-or gate, 2 and gates, one or gate. Thus area count for s(0) is 13 units and area account for c(1) is 8 units.

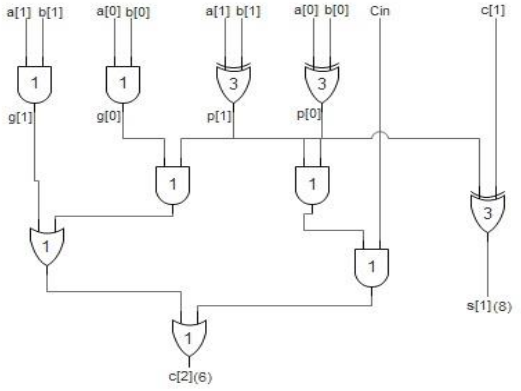

Fig.III (b).

The diagram shown in Fig.III(b). gives the s(1) and c(2) which has delays 8 and 6 respectively. For generating s(1) it requires two ex-or gates,2 and gates and 1 or gate. For generating c(2) it requires 1 ex-or gate, 2 and gates, one or gate. Thus area count for s(0) is 18 units and area account for c(1) is 17 units.

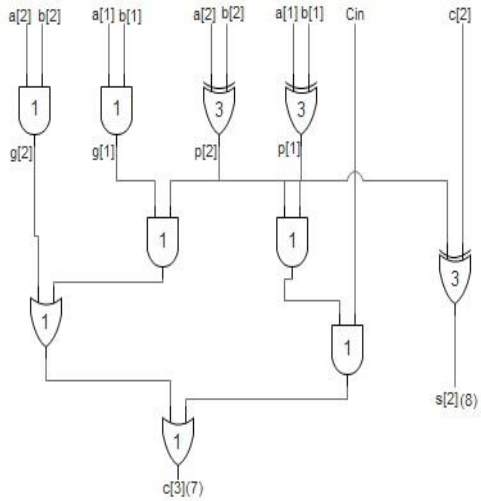

Fig.III(c).

The diagram shown in Fig.III(c). gives the s(2) and c(3) which has delays 8 and 6 respectively. For generating s(2) it requires two ex-or gates,2 and gates and 1 or gate. For generating c(2) it requires 1 ex-or gate, 2 and gates, one or gate. Thus area count for s(0) is 18 units and area account for c(1) is 17 units.

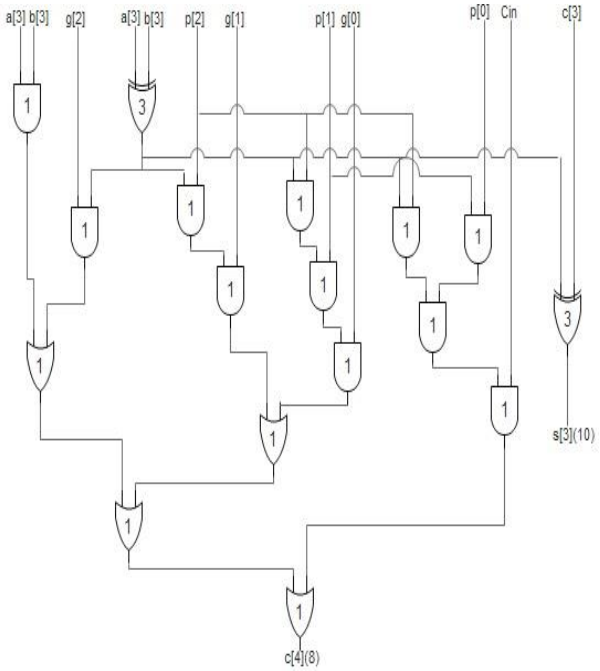

Fig.III(d).

The diagram shown in Fig.III(d). gives the s(3) and c(4) which has delays 10 and 8 respectively. For generating s(3) it requires 4 ex-or gates,7 and gates and 4 or gate. For generating c(4) it requires 4 ex-or gate, 14 and gates, 4 or gate. Thus area count for s(3) is 35 units and area account for c(4) is 38 units.

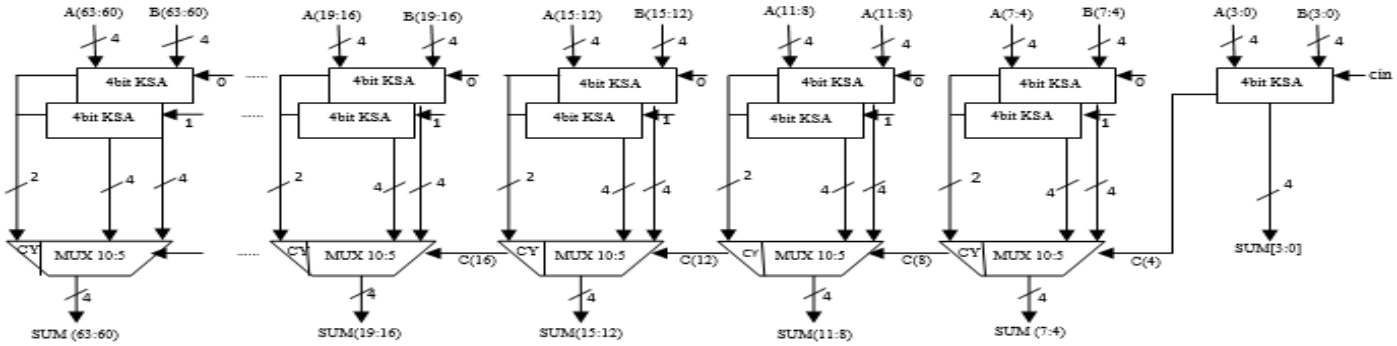

Fig.III: Linear 64-bit Kogge Stone Adder

The delay and area count of Linear Kogge Stone adder groups are shown in Table.III. Area count from group 2 is identical till group 8 which is 147 units, for group 1 it is 74 units.

Table.III: Delay and Area count of linear KSA Groups

Groups	Area	Delay
Group 1	74	10
Group 2	147	13
Group 3	147	14
Group 4	147	17
Group 5	147	20
Group 6	147	23
Group 7	147	26
Group 8	147	29
Group 9	147	32
Group 10	147	35
Group 11	147	38
Group 12	147	41
Group 13	147	44
Group 14	147	47
Group 15	147	50
Group 16	147	53

V. MODIFIED CSA WITH KOGGE STONE

The structure of 64 bit ModifiedKogge Stone Carry Select Adder is shown in Fig.IV. In this instead of KSA, BEC is used for Cin=1 to optimize the area and power. Thus the name Modified Kogge Stone Carry Select Adder. It has eight groups of same size KSA. Each group consists of one 4 bit Kogge stone adders, one 5 bit BEC(Binary to Excess-1 Converter) and one 10:5 multiplexer except first group which has single 4bit KSA only. In which we have given Cin=0 to 4bit KSA and Cin=1 to 5 bit BEC. Depending upon the previous carry the selection of either of the 4bit KSA output or 5 bit BEC output is fed to the 10:5multiplexer along with carry.

Methodology for delay and area calculations are evaluated for Kogge Stone Linear Carry Select Adder with Cin=0 and BEC with Cin=1[5]. Depending upon the selection input i.e, carry from previous group, final sum and carry differ in delays whereas area evaluation for each group except group 1 remains same.

Delay and area evaluation of each group shown in figures in which numerals within brackets specify the delay values. Steps involved during evaluation process are as fallows.

1) Group 1 has one set of Kogge Stone Adder. Based on the considerations of delay values shown in Table.IV, the arrival time of selection input C4(time = 8) of 10:5 mux is earlier than S3(time = 9) and later than S4(time = 10).

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the KSA's. Thus, the delay of group3 to group8 are determined.

Table IV: Delay and Area count of modified linear KSA Groups

Groups	Area	Delay
Group 1	74	10
Group 2	97	16
Group 3	97	19
Group 4	97	22
Group 5	97	25
Group 6	97	28
Group 7	97	31
Group 8	97	34
Group 9	97	37
Group 10	97	40
Group 11	97	43
Group 12	97	46
Group 13	97	49
Group 14	97	52
Group 15	97	55
Group 16	97	58

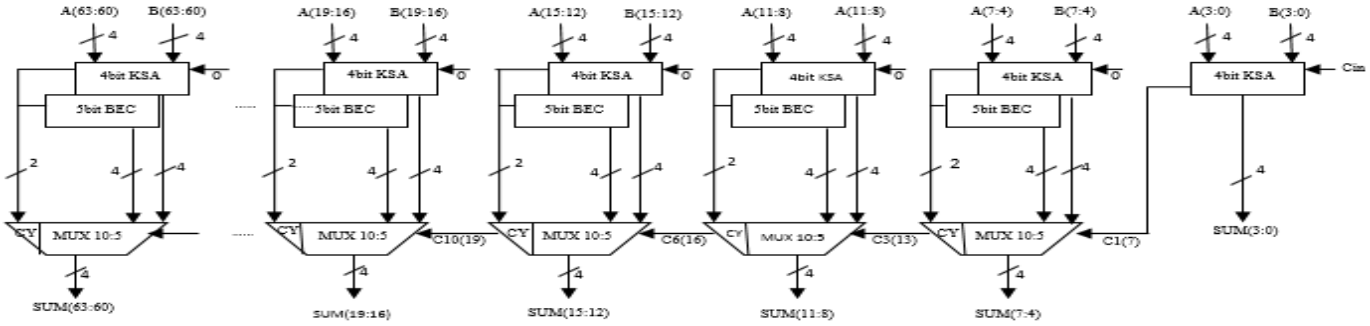

Fig IV: Modified Kogge stone adder using BEC

For group2

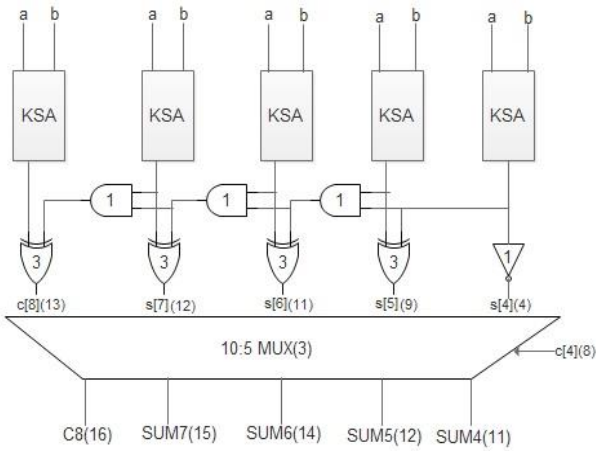

Fig.IV(e).

The BEC structure for group 2 is shown in Fig.IV(e). In group 2 the sum bits from 4 to 7 i.e, s(4) to s(7) are determined with carry c(8). The delay for carry bit c(8) is 16 units and for sum final delay in this group is 15 units.

For group 3

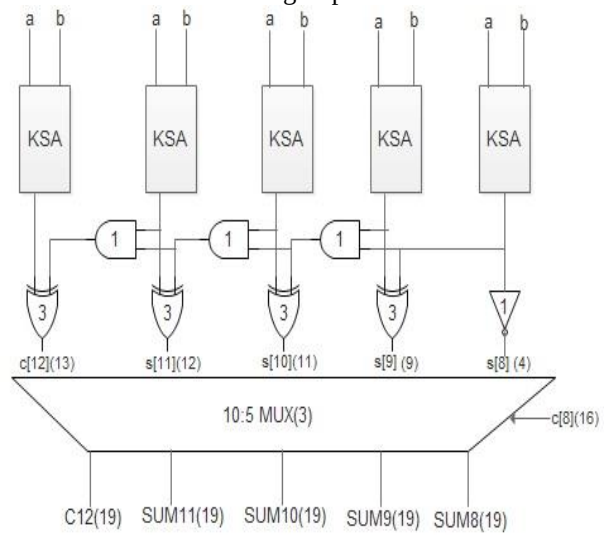

Fig.IV(f).

The BEC structure for group 3 is shown in Fig.IV(f). In group 3 the sum bits from 8 to 11 i.e, s(8) to s(11) are determined with carry c(12). The delay for carry bit c(12) is 19 units and for sum final delay in this group is 19 units.

For group 4

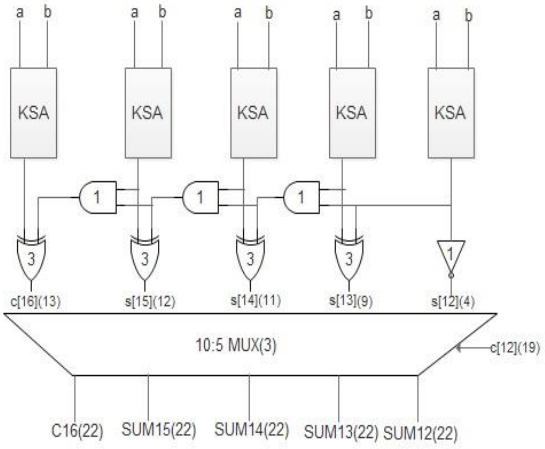

Fig.IV(g).

The BEC structures for different groups in Modified Kogge Stone Adder using BEC are shown in Fig.IV(e) ,FigIV(f), FigIV(g), FigIV(h), FigIV(i), FigIV(j), FigIV(k).

The BEC structure for group 4 is shown in Fig.IV(g). In group 4 the sum bits from 12 to 15 i.e, s(12) to s(15) determined with carry c(16). The delay for carry bit c(16) is 22 units and for sum final delay in this group is 22 units.

For group 5

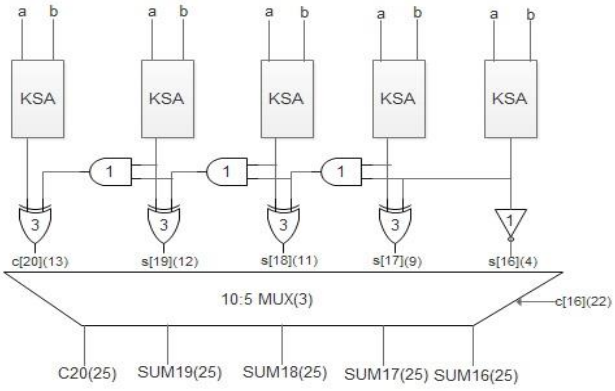

Fig.IV(h).

The BEC structure for group 5 is shown in Fig.IV(h). In group 4 the sum bits from 16 to 19 i.e, s(16) to s(19)

determined with carry c(20). The delay for carry bit c(20) is 25 units and for sum final delay in this group is 25 units.

For group 6

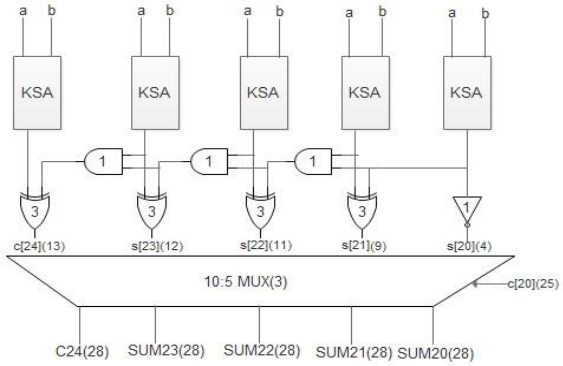

Fig.IV(i)

The BEC structure for group 6 is shown in Fig.IV(i). In group 6 the sum bits from 20 to 23 i.e, s(20) to s(23) determined with carry c(24). The delay for carry bit c(24) is 28 units and for sum final delay in this group is 28 units.

For group 7

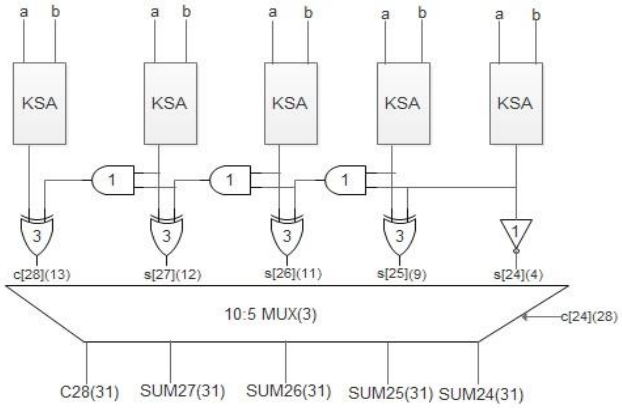

Fig.IV(j).

The BEC structure for group 7 is shown in Fig.IV(j). In group 7 the sum bits from 24 to 27 i.e, s(24) to s(27) determined with carry c(28). The delay for carry bit c(28) is 31 units and for sum final delay in this group is 31 units.

For group 8

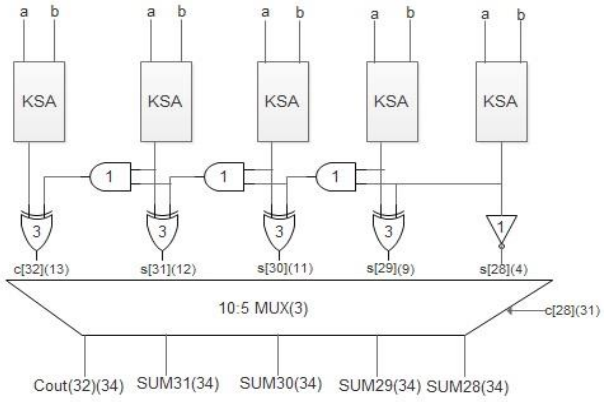

Fig.IV(k).

The BEC structure for group 8 is shown in Fig.IV(k). In group 8 the sum bits from 28 to 31 i.e, s(28) to s(31)determined with carry Cout. The delay for carry bit Cout is 34 units and for sum final delay in this group is 34 units.

VI. RESULTS

The simulated results for both Linear Kogge Stone adder and Modified Kogge Stone adder [6]using Binary to Excess-1 converter are shown in Fig.V. and Fig.VI. respectively.

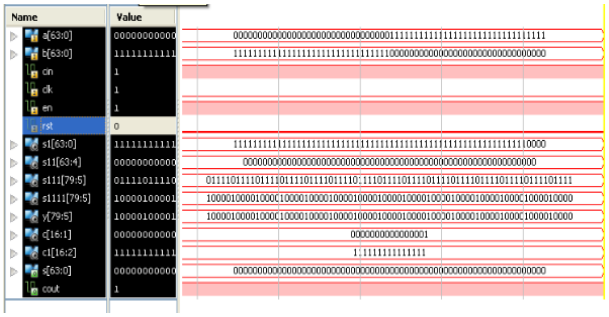

Fig.V: Simulated results for Linear KSA.

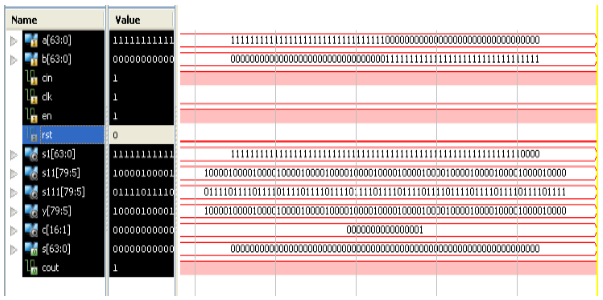

Fig.VI: Simulated results for Modified KSA using BEC

TABLE.V: Summary results for Linear KSA

Logic Utilization	Used	Available	Utilization
Number of Slices	784	4656	16%
Number of 4 input LUTs	744	9312	7%
Number of bonded IOBs	197	232	84%

TABLE.VI: Summary results for Modified KSA using BEC

Logic Utilization	Used	Available	Utilization
Number of Slices	756	4656	16%
Number of 4 input LUTs	711	9312	7%
Number of bonded IOBs	197	232	84%

VII. CONCLUSION

A simple approach is presented in this paper to reduce the area of Linear KSA architecture. The reduced number of gates ofthis work offers the great advantage in the reduction of area. The modified KSA architecture issimple and efficient architecture for VLSI hardware implementation in the aspect of low area. The results show that the modified KSA has a slightly larger delay than the Linear KSA.

VIII. FUTURE SCOPE

Area delay product of regular 64-bit Linear KSA and Modified KSA using BEC can be experimentally performed.

IX. REFERENCES

[1] Sajesh Kumar, U, Mohamed Salih K.K and Sajith K. "Design and Implementation of Carry Select Adder without using Multiplexers" 2012 IEEE.

[2] O.J.Bedrij, "Carry-select adder" IRETrans Electron, Comput, PP.340-344,1962.

[3] Santosh Elangadi and Suhas Shirol "Design and Characterization of High Speed Carry Select Adder" 2348-4748, volume 1, Issue 6, July 2014.

[4] B. Ramkumar and Harish M Kittur "Low-Power and Area-Efficient Carry Select Adder"371-375, Vol. 20, No. 2, February 2012.

[5] K.BalaSindhuri, N. Uday Kumar, D.V.N. Bharathi, B.Tapasvi. "128-Bit Area – Efficient Carry Select Adder" IJRASET

[6] A Verilog HDL Primer by J.Bhaskar

Tapasvi B received his B.Tech degree in Electronics and communication engineering from Swarnandhra College of Engineering and Technology, Narsapur. At present he is doing M.Tech at SRKR Engineering College, Bhimavaram. His areas of interest are Very Large Scale Integrated Circuits and Communication Systems.

BalaSindhuri K received her B.E degree in Electronics & communication Engineering from S.R.K.R Engineering college,Bhimavaram and M.Tech degree in VLSI System Design from Shri Vishnu Engineering College for Women,Vishnupur,Bhimavaram.At present, She is working as an Assistant Professor at SRKR Engineering College, Bhimavaram. She has 4 years of teaching experience. Her area of interest is Very Large Scale Integrated Circuits. She has published 5 research papers in International and National Conferences.

Chaitanya Varma I is currently studying 4/4 B.E. in the stream of Electronics and Communication Engineering from S.R.K.R. Engineering College, Bhimavaram.

Udaya Kumar N received his M.Tech degree in Microwave Electronics from University of Delhi South Campus and is pursuing Ph.D degree in DIP at Jawaharlal Nehru Technological University, Hyderabad. At present he is working as Professor at SRKR Engineering College, Bhimavaram. He has 22 years of teaching experience and guided many UG & PG projects. His areas of interest are Digital Image Processing and Digital Signal Processing. He has published more than 20 research papers in International and National Conferences. One of his papers has been published as a book chapter in the research book published by Springer. He also co-authored several text books for engineering and diploma students. He is a member of IEEE and Fellow of IETE.