Low Voltage Stress-Induced-Leakage-Current in Ultrathin Gate Oxides

Paul E. Nicollian, Mark Rodder, Douglas T. Grider, Peijun Chen, Robert M. Wallace, Sunil V. Hattangady
Texas Instruments Incorporated
Silicon Technology Development
MS 3737, P.O. Box 650311,
Dallas, Texas 75265
Tel: (972)-995-2820. Fax: (972)-995-2770. email: nicoll@spdc.ti.com

ABSTRACT

Stress-Induced-Leakage-Current (SILC) is an important concern in ultrathin gate oxides because it may impose constraints on dielectric thickness scaling. We show that for oxides less than ~3.5 nm thick, interfacial traps generated from direct tunneling stress result in a sense voltage dependent SILC mechanism that can dominate the gate leakage current at low operating voltages. Unlike tunneling through oxide traps, tunneling via interfacial states is strongly sense voltage dependent, with the peak degradation occurring near operating voltage in ultrathin gate oxide technologies. The leakage current resulting from this interfacial trap tunneling mechanism can be orders of magnitude larger compared to bulk oxide trap tunneling.

I. INTRODUCTION

SILC is an increase in gate oxide leakage current resulting from the application of a stress voltage or current [1-4]. It is an important concern in scaling gate oxide thickness because it can decrease DRAM refresh times, degrade EEPROM data retention, and increase MOSFET off-state power dissipation.

The SILC effect is illustrated in Figure 1 (from Ref. 4). After stress, a significant increase in gate oxide leakage current appears. This current increase is primarily observed when the measure (sense) voltage is in the direct tunneling regime, where the voltage across the oxide is less than about 3 V (the Si-SiO_2 barrier height). It can be seen that the relative increase in current is not strongly dependent on the sense voltage in the direct tunneling regime (gate voltages less than about 3.5 V for the MOSFET in Figure 1). The SILC effect diminishes as the device enters Fowler-Nordheim conduction [4,5,6]. SILC arises from the generation of bulk traps in the oxide during stress, leading to higher direct tunneling currents due to trap-assisted-tunneling [3,4]. A band-diagram for SILC illustrating inelastic trap-assisted tunneling through bulk oxide traps is shown in Figure 2 (from Refs. 5,6). An inelastic tunneling event is a physical process where the energy of the tunneling species is reduced relative to the anode Fermi level. SILC transport is thought to be an inelastic tunneling process because of the resultant decrease in quantum efficiency [5] and apparent increase in Fowler-Nordheim barrier height [6].

An energy of about 5 V is required during stress to generate the bulk oxide trap states that cause SILC [4]. This energy threshold has been correlated to the release of a hydrogen-like species at the anode interface that is believed to be a precursor of trap creation [7]. We will show that for stress voltages below 5 V and for gate oxide thickness less than ~3.5 nm, SILC is caused by tunneling via the interfacial traps created from stress, rather than through bulk oxide traps.

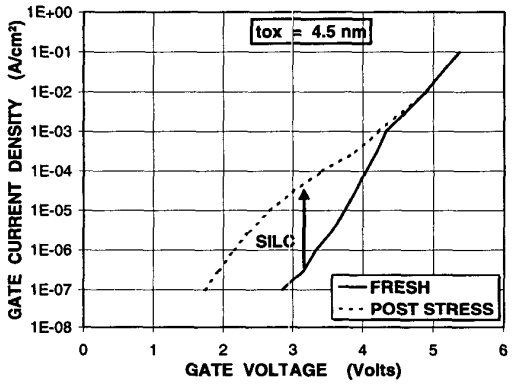

Figure 1. Fresh and post-stress I-V curves, illustrating SILC effect. From DiMaria and Cartier [4].

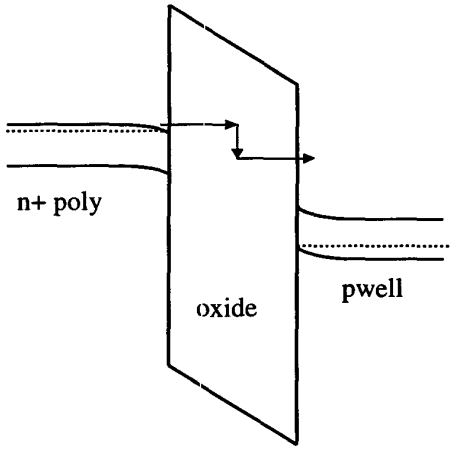

Figure 2. nMOS band diagram for $-V_G$ illustrating inelastic trap-assisted tunneling through bulk oxide traps; causing SILC. From Takagi et al [5], Rosenbaum and Register [6].

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II. EXPERIMENT

Constant voltage stress is performed on nMOS and pMOS capacitors fabricated using a short flow or full-flow dual-poly cMOS process [8]. The stress is periodically interrupted to perform an I-V sweep. A quasi-static ramp rate is maintained during current sense to minimize transient effects [3]. Stress times range from 1 to 20,000 seconds.

The gate oxides are thermally grown SiO_2 films with thickness ranging between 2.0 nm – 4.0 nm. Oxide thickness, voltage, and field are obtained from quantum C-V device simulations [9]. The C-V simulations are matched to experimental data. Gate oxide areas are on the order of $5x10^{-5}$ to $1x10^{-3}$ cm^2. All measurements are taken at room temperature.

III. RESULTS

It has been shown that the SILC generation rate is determined by the gate voltage, independent of doping type or stress polarity [10]. Stressing both the nMOS and pMOS devices at the same voltage means that the well of one device is accumulated, while the other is inverted. In ultrathin gate oxides, the oxide electric field can be significantly lower for the device that is accumulated, since the voltage drop across the oxide will be roughly 1 V lower. The inverted device can be subjected Fowler-Nordheim tunneling stress, while the accumulated device is under direct tunneling stress. We apply these principles to evaluate the behavior under both high and low field stress.

Fresh and post-stress I-V characteristics of nMOS devices with 2.8 nm thick gate oxide are shown in Figure 3. The oxides were stressed for 1 second at incrementally higher voltages until soft breakdown (SBD) occurred. In this portion of the experiment, a short stress interval was chosen to maximize the range of electric fields used during stress to facilitate the observation of SILC mechanism threshold energies. A measure (sense) voltage dependent low voltage SILC (LV-SILC) effect is observed prior to breakdown, indicating that the current increase is not due to either trap-assisted tunneling via oxide traps or, to charge trapped in the oxide. As the onset of $-V_G$ F-N tunneling is around –5 V for the device shown in Figure 3, the LV-SILC effect cuts off at voltages significantly below the F-N tunneling threshold. The fresh and post-stress I-V curves for 3.3 nm and 3.7 nm nMOS oxides are shown in Figures 4 and 5. Comparison of Figures 3-5 shows that the low voltage SILC effect diminishes as oxide thickness is increased, and is no longer apparent in the 3.7 nm film. Concurrently, the nearly sense voltage independent SILC that is characteristic of trap-assisted tunneling through oxide traps begins to appear when the maximum stress voltage increases above 5 V, as shown in Figure 4.

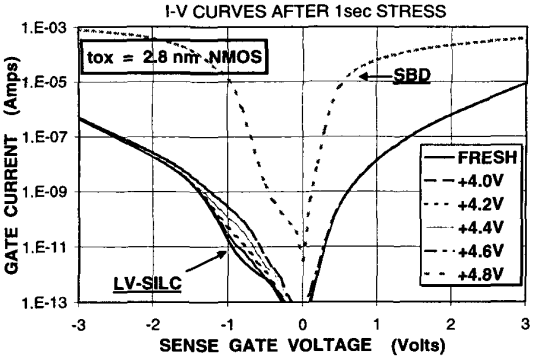

Figure 3. Fresh and post-stress I-V curves for 2.8 nm nMOS oxides. The devices were progressively stressed to higher voltages at 1 second intervals. A sense-voltage dependent LV-SILC effect is observed.

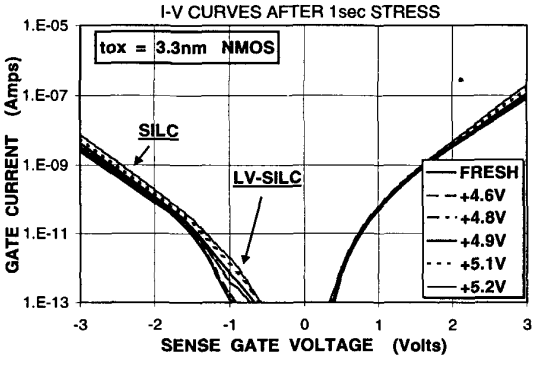

Figure 4. Fresh and post-stress I-V curves for 3.3 nm nMOS oxides. The devices were progressively stressed to higher voltages at 1 second intervals. There is a transition from LV-SILC to conventional SILC when the stress exceeds 5 V.

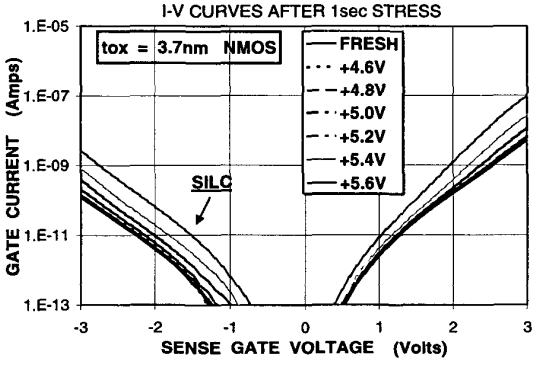

Figure 5. Fresh and post-stress I-V curves for 3.7 nm nMOS oxides. The devices were progressively stressed to higher voltages at 1 second intervals. LV-SILC is not observed at this gate oxide thickness.

The effect of measure delay time on the low voltage SILC effect is shown in Figure 6. The voltage is stepped in 100 mV increments, with the delay time ranging from 0.1 to 50 seconds per step. The LV-SILC phenomenon is not significantly affected by step delay time. This indicates that this is not a transient effect. The SILC increase as a function of stress time for a 2.8 nm nMOS device is shown in Figure 7. The device was stressed at high field in inversion in the Fowler-Nordheim regime. The current measured at stress voltage shows little change; further indicating that the current increase observed at low sense voltages is not due to charging (filling) of traps in the oxide.

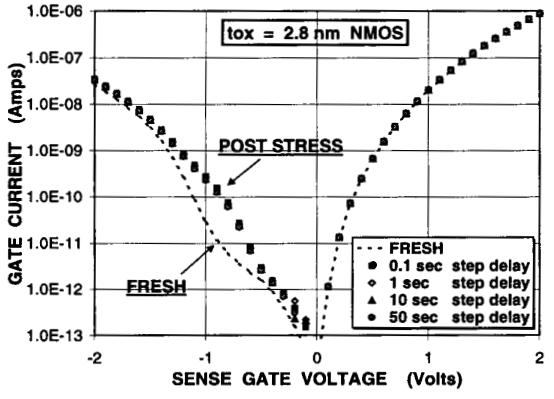

Figure 6. Fresh and post-stress I-V characteristics, illustrating the effect of step delay time on LV-SILC.

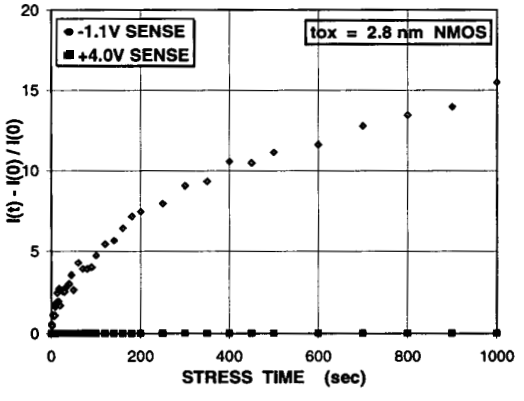

Figure 7. Normalized nMOS current increase for –1.1 V and +4.0 V sense after stress in the F-N regime at +4. 0 V.

Low voltage SILC is generated for both positive and negative gate polarity stress, as illustrated in Figure 8 for 2.8 nm nMOS oxides. This indicates that the LV-SILC phenomenon can occur whether the poly or the substrate is the anode, and occurs for both off-state (accumulation) and on-state (inversion) stress. The low voltage SILC phenomenon occurs in both nMOS and pMOS devices, as shown in Figure 9. Note that LV-SILC can result in >100X increase in leakage current. Peak degradation occurs at sense voltages near VFB for both nMOS and pMOS devices, and is detected only when the sense voltage is about +/-1V from VFB. **As the gate voltage is approximately equal to the separation in anode and cathode Fermi levels [11], this means that the LV-SILC effect is occurring ONLY when energy states within the anode and cathode bandgaps are within the same range of electrostatic potential.** This strongly indicates that the LV-SILC effect is due to tunneling via interfacial traps. We have verified that interface traps are created in our devices during stress by measuring gate controlled diode generation currents (not shown).

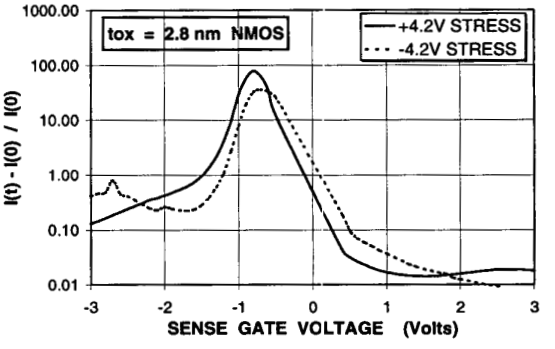

Figure 8. Post-stress I-V curves for 2.8 nm nMOS oxides, showing that LV-SILC occurs for both +/- V_G stress.

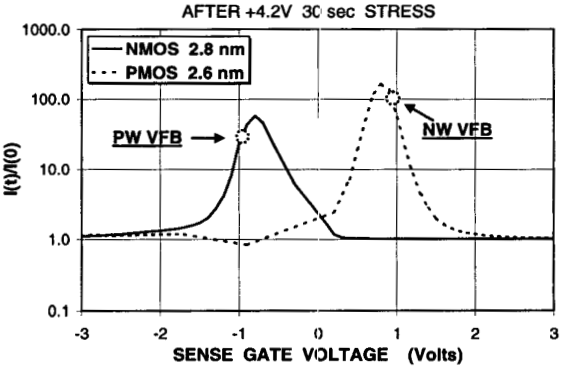

Figure 9. Post-stress I-V curves comparing nMOS and pMOS. In both cases, peak degradation occurs near VFB. Current increase is primarily observed when the sense voltage is within +/- 1V of VFB.

IV. MODEL

The band diagram for the proposed LV-SILC mechanism in nMOS devices is shown for V_G slightly less (more negative) than VFB (pwell accumulated) in Figure 10. Only states that are energetically favorable for conduction are shown. The transport process is: 1) electrons are emitted from

traps near the n+ poly interface to interfacial traps near the pwell interface, then 2) are subsequently injected into the pwell conduction band. Only states below the cathode (n+ poly) Fermi level can emit tunneling electrons, and only states above the anode (pwell) Fermi level can capture electrons. The band diagram for V_G slightly greater than VFB (pwell depleted-weakly inverted) is shown in Figure 11. In this case, 1) electrons tunnel from trap states near the pwell interface to traps near the n+ poly interface, then 2) are subsequently emitted into the n+ poly conduction band. Only states below the pwell Fermi level can emit electrons, and only states above the n+ poly Fermi level can capture electrons. Note that traps must be present at both anode and cathode interfaces for LV-SILC to occur. Also, if the electron captured in an anode trap site relaxes to an energy that is significantly below the silicon conduction band, little current increase would be observed. Therefore, the LV-SILC mechanism must be either an elastic transport process, or an inelastic process with a small relaxation energy. We have not yet conclusively resolved this issue.

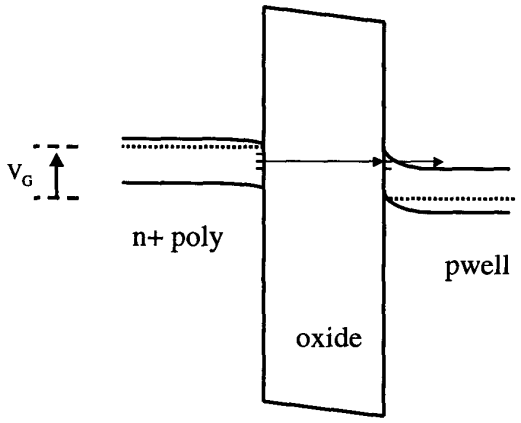

Figure 10. nMOS band diagram for LV-SILC. V_G is just < VFB. Only trap states that are energetically favorable for transport are shown.

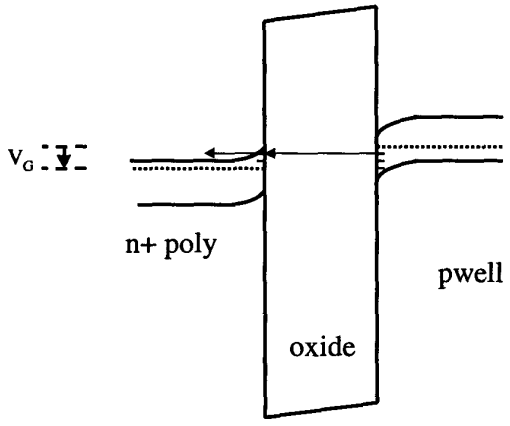

Figure 11. nMOS band diagram for LV-SILC. VFB < V_G < 0V. Only trap states that are energetically favorable for transport are shown.

For nMOS, if V_G is more than 1 volt more negative than VFB, LV-SILC transport is not energetically favorable, because all of the cathode energy states are at a higher energy than the anode conduction band. Nominal direct tunneling becomes the dominant mechanism, where electrons tunnel from n+ poly (accumulated) conduction band to pwell conduction band, and low voltage SILC is not observed (Figure 12). Similarly, if V_G is more than 1 volt more positive than VFB, then electrons tunnel from the pwell (inverted) conduction band to n+ poly conduction band, and interfacial traps have similarly little effect. For pMOS, complementary arguments can be made to elucidate the low voltage SILC mechanism.

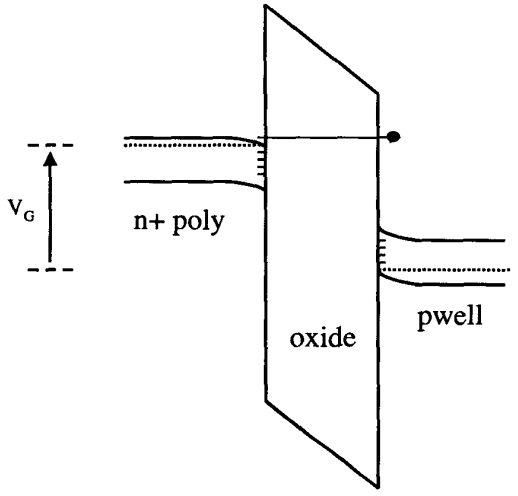

Figure 12. nMOS band diagram for nominal direct tunneling for $-q\phi_B < V_G <$ VFB -1V. LV-SILC is insignificant under these bias conditions.

V. DISCUSSION

The LV-SILC effect occurs for either stress polarity, but is only detected when the sense voltage is near VFB. During this sense condition, the Si-SiO_2 interface is accumulated and the device is in the off-state. The effects of LV-SILC (caused by interface traps) and conventional SILC (caused by oxide traps) can be resolved by sensing in the off-state (accumulated well) and on-state (inverted well) respectively. A plot of normalized SILC versus fluence for a 2.8 nm nMOS device stressed at +4 V is shown in Figure 13. It can be seen that the current increase is a factor of 500X higher for the LV-SILC effect compared to conventional bulk oxide trap SILC. Sense voltage independent SILC effects due to trap-assisted tunneling through bulk oxide traps are still present, but result in much lower degradation relative to LV-SILC. Monitoring LV-SILC by sensing near VFB provides greatly increased sensitivity to changes in the device resulting from stress.

The gate current versus stress time is shown for a typical 2.0 nm pMOS oxide in Figure 14. The device was stressed in the direct tunneling regime at an oxide field of 9 MV/cm (oxide voltage of 1.8 V). The current was sensed at a gate voltage of 1.32 V (maximum operating voltage for 1.2 V

technology). The LV-SILC mechanism causes the device to exceed off-state leakage current requirements during direct tunneling stress. Because only a fraction of the total gate oxide area in an inverter circuit is biased in the off-state, it is not entirely clear whether the LV-SILC effect will actually be a limiting factor in logic technology scaling.

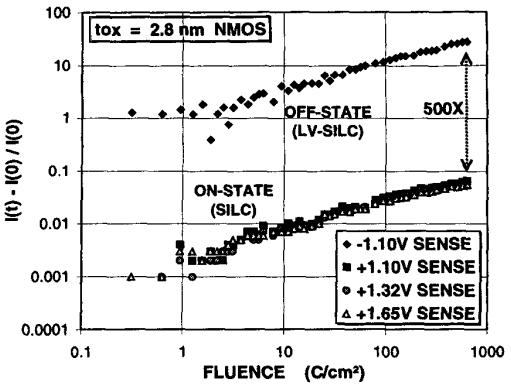

Figure 13. Leakage increase in 2.8 nm nMOS device after +4.0 V stress. The effects of interfacial states, which give rise to sense-voltage dependent LV-SILC are monitored by sensing in the off-state. The effects of bulk oxide traps, which cause conventional sense-voltage independent SILC can be separated out by sensing in the on-state. Normalized current increase is much higher for LV-SILC.

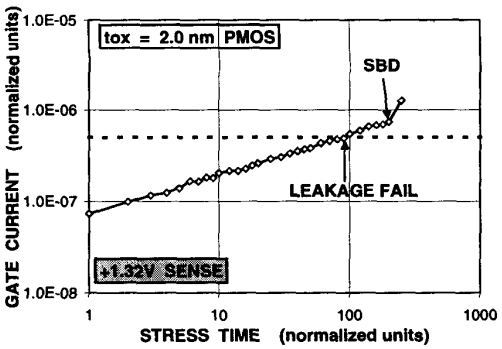

Figure 14. Gate current vs. stress time for a typical 2.0 nm pMOS device. The oxide was stressed in the direct tunneling regime. The dashed horizontal line represents the low power leakage limit. LV-SILC causes the device to exceed the low power leakage requirement before soft breakdown occurs.

VI. CONCLUSIONS

We have shown that for stress voltages below 5 V and for gate oxide thickness less than 3.5 nm, SILC is caused by tunneling via interfacial traps, rather than through bulk oxide traps. It is not a transient effect. This phenomenon is still observed under direct tunneling stress conditions. Unlike tunneling through oxide traps, tunneling via interfacial traps is strongly sense voltage dependent. Peak degradation occurs at sense voltages near VFB. The effect is only observed at sense voltages that are within 1 volt of VFB, since tunneling via interfacial states is energetically favorable only in this bias range. Since VFB in dual poly processes is about –1 V for nMOS and +1 V for pMOS, this mechanism may be an important consideration in sub-1.2 V technologies that operate in this regime, as peak degradation occurs near operating voltage.

ACKNOWLEDGEMENTS

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