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Research Article

Power Analysis of Sense Amplifier Designs for low voltage Memories

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Abstract

A memory array structure consists of matrix of SRAM (Static Random Access Memory) cells in which each memory cell in an array structure can be accessed by row and a column decoder. Sense amplifier plays a vital role in memory array structure.The job of a sense amplifier is to sense the bit lines and retrieve the stored data in a memory.Reducing the power consumption of the sense amplifier reduces the power consumption of the whole circuit.The above explained operation can be carried out using Synopsys-Custom Designer tool by applying some optimization techniques like stack, sleep transistor sleepy stack and leakage feedback techniques.

Keywords: Sense amplifier; Power; Low voltage; Memories.

Introduction

During the desktop PC (Personal Computer) design era VLSI (Very Large Scale Integration) design efforts have focused primarily on optimizing speed to realize computationally intensive real-time functions such as video compression, gaming, graphics etc. As a result, we have semiconductor ICs (Integrated Circuits) that successfully integrated various complex signal processing modules and graphical processing units to meet our computation and entertainment demands [1]. The strict limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements. While wireless devices are rapidly making their way to the consumer electronics market, a key design constraint for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries.

Modern System-on-Chip demands for more power. In both logic and memory, Static power is growing really fast and Dynamic power kind of grows. Overall power is dramatically increasing. The growing market of portable (e.g., cellular phones, gaming consoles etc) is battery-powered electronic systems demands microelectronic circuits design with ultra-low power dissipation [2].

As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. Hence the techniques to reduce power dissipation are not limited to dynamic power [3]. Power optimization in a processor can be achieved at various abstract levels. Total Power dissipated in a CMOS (Complementary Metal Oxide Semiconductor) circuit is sum total of dynamic power, short circuit power and static or leakage power [4]. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product.

Today workstation and computers are demanding faster memories in an effort to enhance system performance. A memory array consists of a matrix of SRAM cells in which each cell can be accessed by a column and row decoders by using word line and bit lines [5]. Bit line may be bit and bit bar lines. Normally, RAM memory is divided into two types namely SRAM and DRAM. Static Random Access Memory is a type of semiconductor memory that uses bistable

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latching circuitry to store each bit. SRAM is faster than DRAM. The main advantages of SRAM are that there is no need for periodic refreshment and it consumes low power [6].

The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for sense amplifiers. Sense amplifier is one of the important peripheral circuits in the memory as it strongly influences the memory access times. It retrieves the stored data from the memory array by amplifying small differential voltage to a full logic signal that can be further used by digital logic [7]. The different sense amplifier designs were designed using synopsys EDA (Electronic Design Automation) tool and compared with various power reduction technique based sense amplifier designs.

Conventional Designs

Current Conveyor-based Sense Amplifier

The current conveyor-based sense amplifier was consists of four identical PMOS transistors which is shown in figure 1 is connected in a feedback structure. It is assumed that the complementary bit-lines (BL and BL') are pre-charged to VDD and all four PMOS transistors operate in saturation region during the read cycles. The current conveyor is enabled by triggering the column select (CS) signal low. Since all four transistors are in saturation, their source-to-drain currents are only dependent on their gate-to-source voltages. As a result, voltage at the bit- line terminals (VBL and VBL') is the same and equal to (V1 + V2). The current conveyor therefore has the ability to convey the differential current from the bit-lines to the data-line without waiting for the discharging of the highly capacitive bit-lines [8].

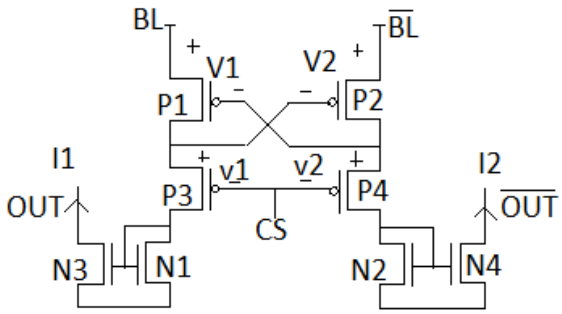

Figure 1. Current conveyor based Sense amplifier

Alpha-Latch based Sense Amplifier

The NMOS transistor N5 is used to the amplifier off during standby thus saves power. When the sense amplifier is activated by the enable signal (EN), the differential input from the complementary bit-lines induces a differential trans-conductance in N3 and N4. As a result, voltage and current differences will appear at the drains of N3 and N4, i.e., the sources of N1 and N2. Since the CS signal turns off N6, the flip-flop structure will latch and full swing voltages will be available at nodes A and B, turning one of the transistors N7 and N8 on while the other is off. During standby, EN' is kept high to turn P3 and P4 off. During operation, both P3 and P4 are turned on but one of N7 and N8 is turned off, thus only one current will flow to the data-lines to the output of SRAM [9]. The following figure 2 shows the design of Alpha latch based sense amplifier.

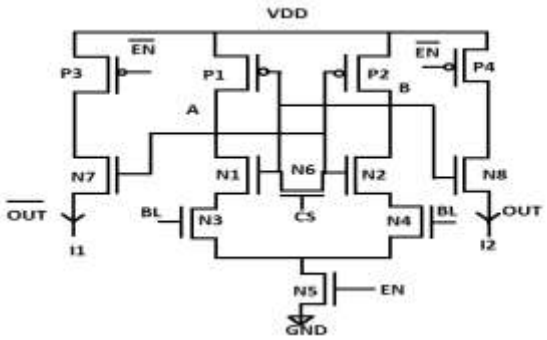

Figure 2. Alpha Latch based Sense amplifier

Current Mirror based Sense Amplifier

Sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip. The job of a sense amplifier is to sense the low power signals from a bit line which represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory. Modern sense-amplifier circuits consist of 2 to 6 (usually 4) transistors early sense amplifiers for core memory sometimes contained as many as 13 transistors. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. It is one of the only analog circuits in a computer's memory subsystem. The following figure 3 shows the design of current mirror based sense amplifier [10].

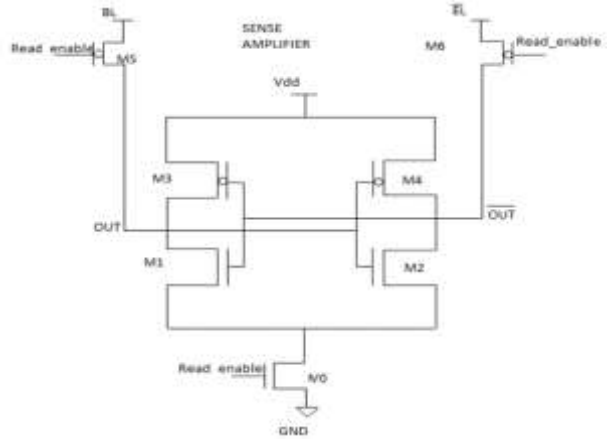

Figure 3. Current mirror based Sense amplifier

Power Reduction Methods

Stack technique

A stack technique is one of the optimization technique that is adopted for reducing the power consumption in sense amplifiers. Here in this technique instead of one transistor two transistors are used and the power level is greatly minimized. This technique is based on the fact that natural stacking of MOSFET helps in achieving leakage current which is shown in the figure 4 The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect. An effective way to reduce leakage power in active mode is stacking of transistor [11].

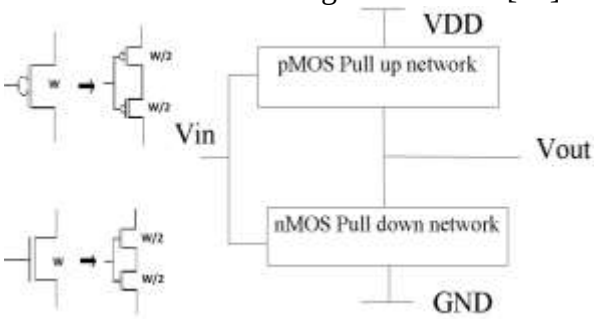

Figure 4. Stack technique

Sleep Transistor Technique

This is a State-destructive technique which cuts off either pull up or pull down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-V_{th} sleep transistors between pull up networks and Vdd and pull down networks and gnd while for fast switching speeds, low-Vth transistors are used in logic circuits are shown in figure 5 Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep. The sleep transistor turn off the circuit by cutting off the power rails in idle mode thus can reduce leakage power effectively [11].

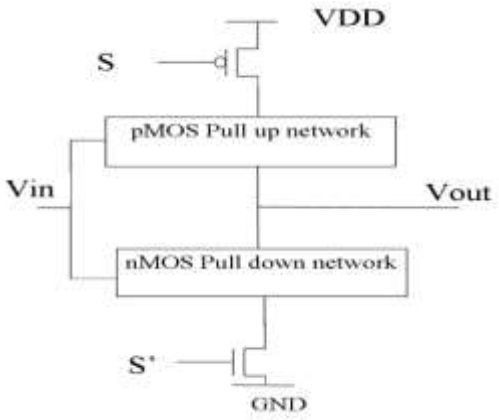

Figure 5. Sleep transistor technique

Sleepy Stack Technique

The forced stack and the sleep transistor techniques are combined to get the sleepy stack structure which is shown in the figure 6. The function of sleep transistors in sleepy stack is same as of the sleep transistor in sleep transistor technique. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current .The drawback of this technique is increase in area [12].

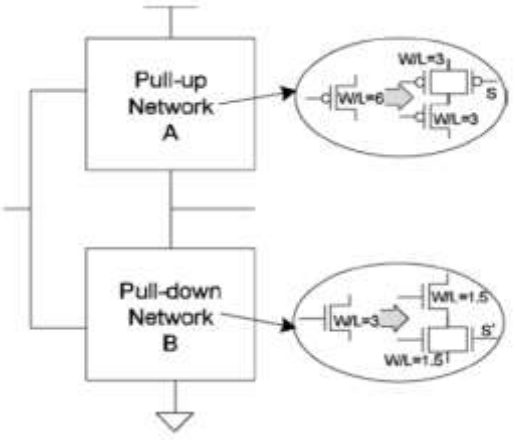

Figure 6. Sleepy Stack technique

Leakage Feedback Technique

The leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the two transistors are driven by the output of an inverter which is driven by output of

the circuit implemented utilizing leakage feedback. As shown in figure 7. A PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail [13].

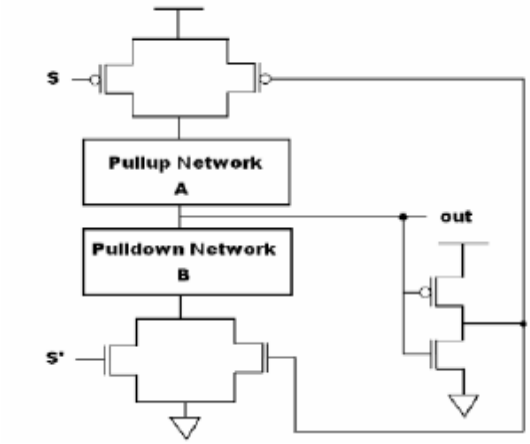

Figure 7. Leakage Feedback technique

Results and discussion

The various designs of memory are simulated and verified using Synopsys custom designer tool under 100 nm technology. The sample designs of alpha latch based sense amplifier using power reduction techniques are given below. The complete comparative power analysis of various sense amplifier results are also given.

Alpha latch based using stack technique

The figure 8 shows the schematic view of alpha latch based using stack technique in Custom Designer Schematic Editor.

Output of Alpha latch based using stack technique

The figure 9 is the output of alpha latch based using stack technique and it is simulated in Wavelet Analyzer using Custom design. The input values are bl=10010110, blbar=01101001 and the output values obtained are out =10010110, out bar=01101001. The enable signals were given accordingly which enables the respective transistors.

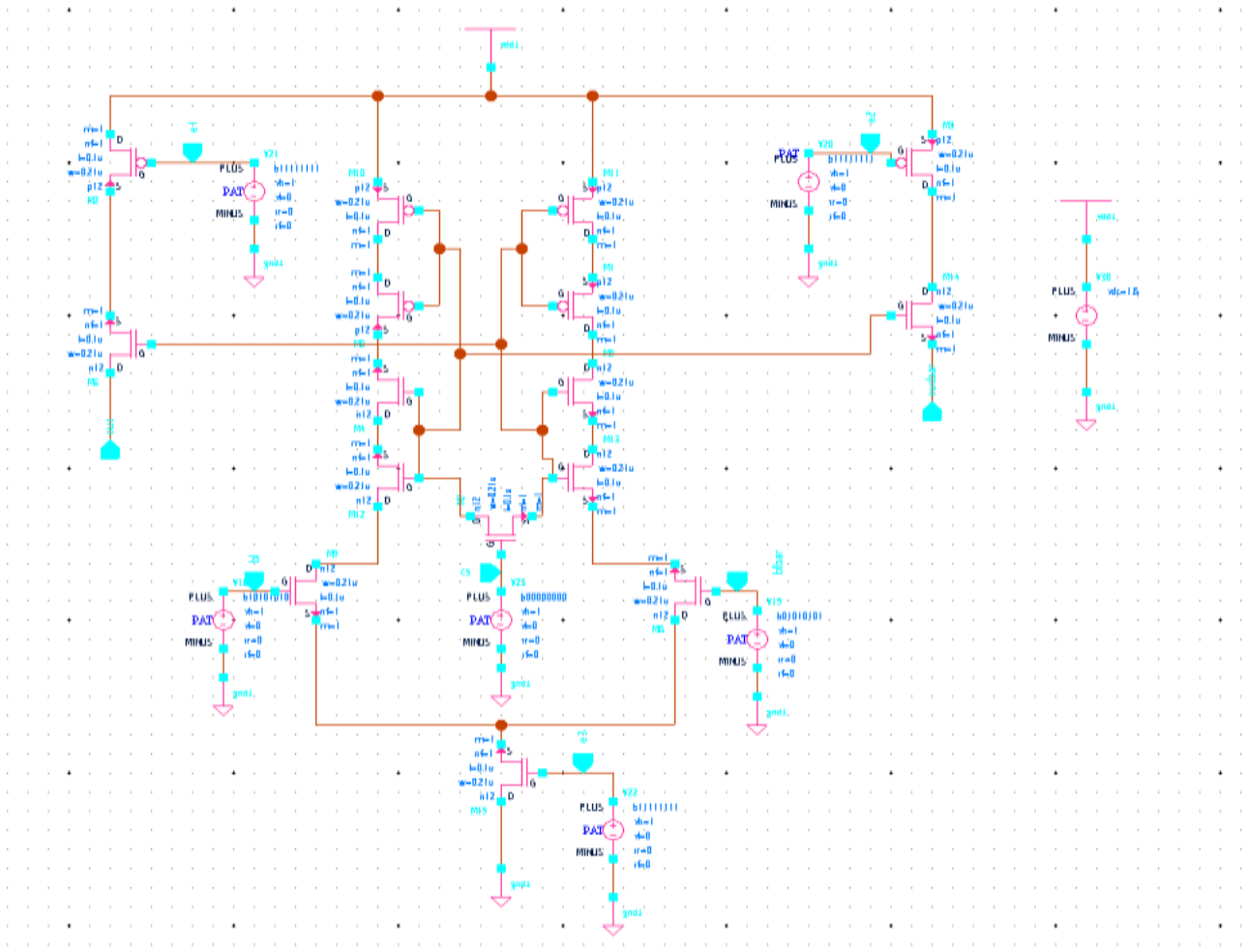

Figure 8. Schematic view of alpha latch based using stack technique

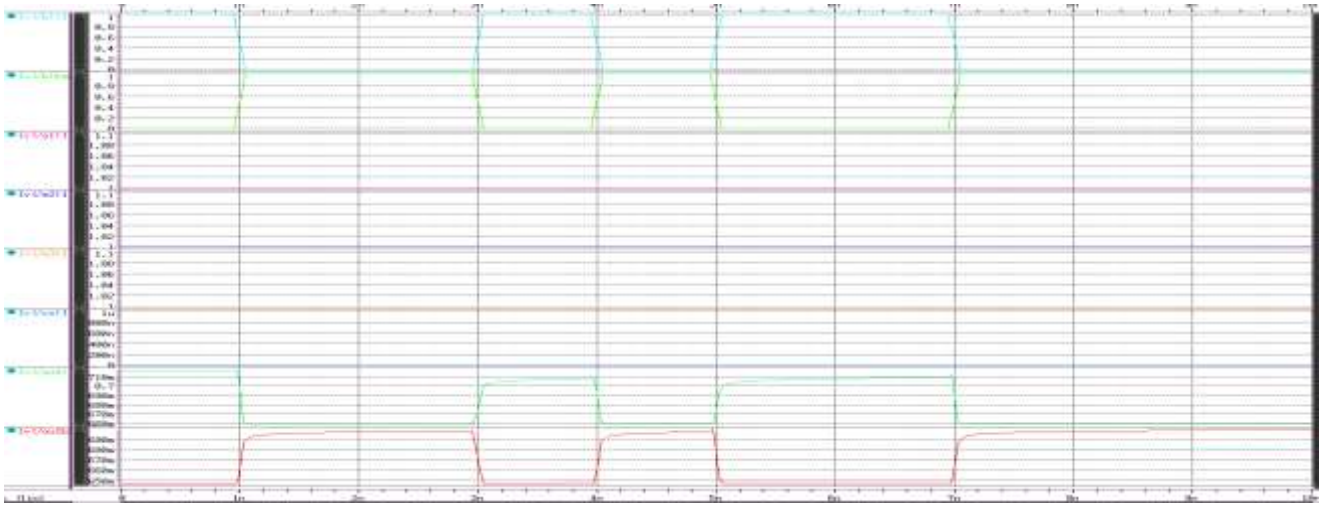

Figure 9. Output of alpha latch based using stack technique

Alpha latch based using sleep transistor technique

The figure 10 shows the schematic view of alpha latch based using sleep transistor technique in Custom Designer Schematic Editor. The sleep transistors turn off the circuit by cutting off the power rails so that the power consumed by the circuit is reduced to a determined level.

Output of alpha latch based using sleep transistor technique

The figure 11 is the output of alpha latch based using sleep transistor technique and it is simulated in Wavelet Analyzer using Custom design. The input values are bl=11001100, blbar=00110011 and the output values obtained are out =11001100, out bar=00110011. The enable signals were given accordingly which enables the respective transistors.

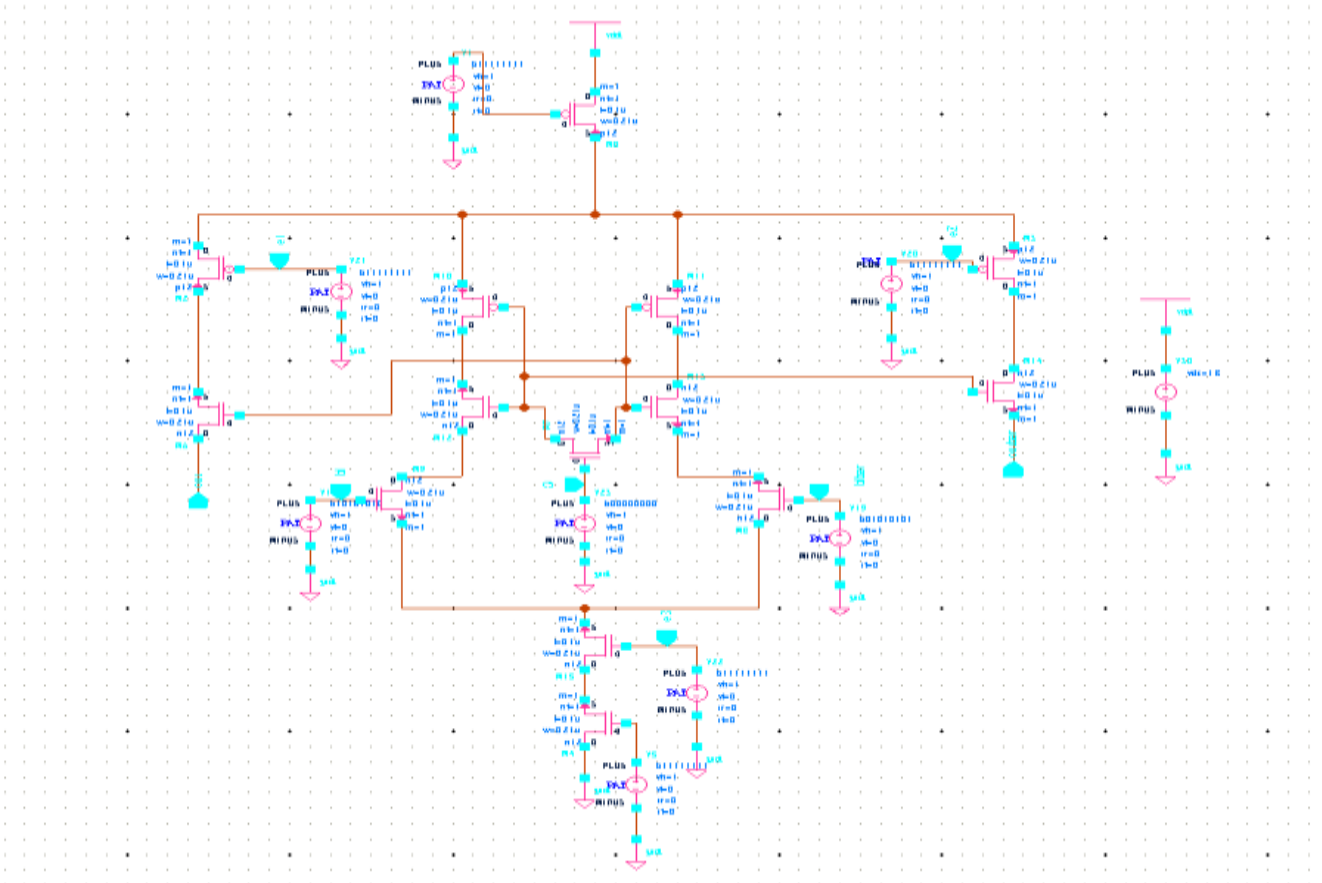

Figure 10. Schematic view of alpha latch based using sleep transistor technique

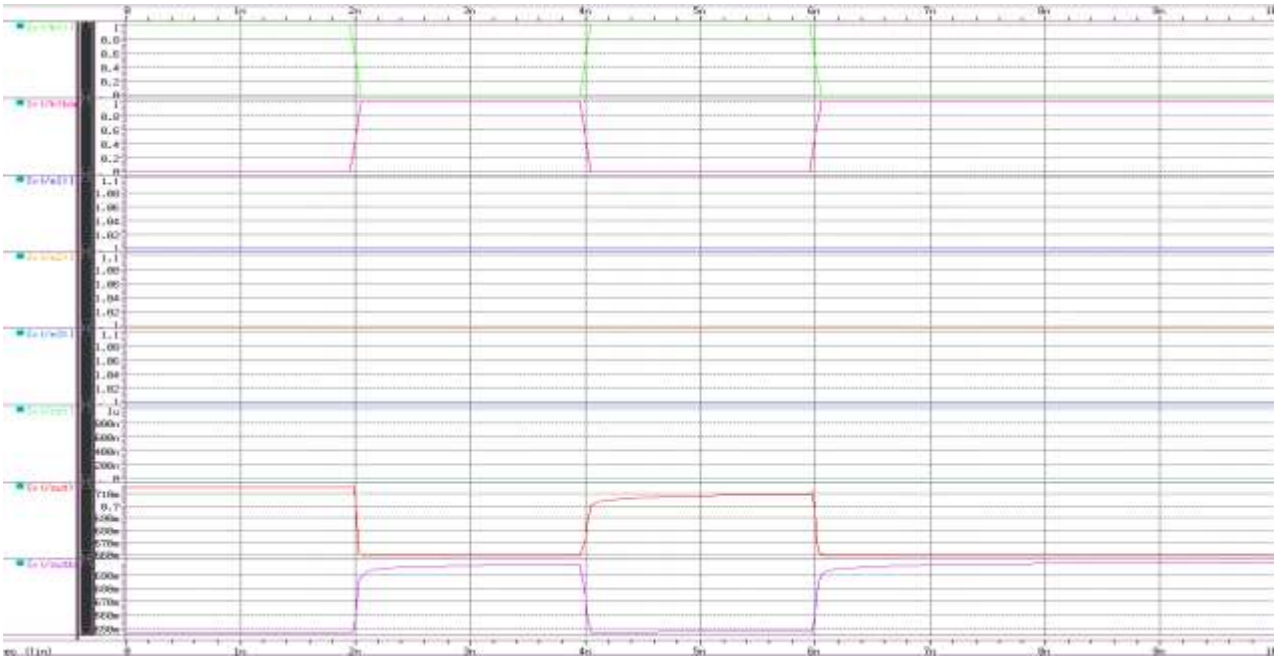

Figure 11. Output of alpha latch based using sleep transistor technique

Alpha latch based using sleepy stack technique

The figure 12 shows the schematic view of alpha latch based using sleepy stack technique in Custom Designer Schematic Editor.

Output of Alpha latch based using sleepy stack technique

The figure 13 is the output of and it is simulated in alpha latch based using sleepy stack technique in Wavelet Analyzer using Custom design. The input values are bl=10101010, blbar=01010101 and the output values obtained are out =10101010, out bar=01010101. The enable signals were given accordingly which enables the respective transistors.

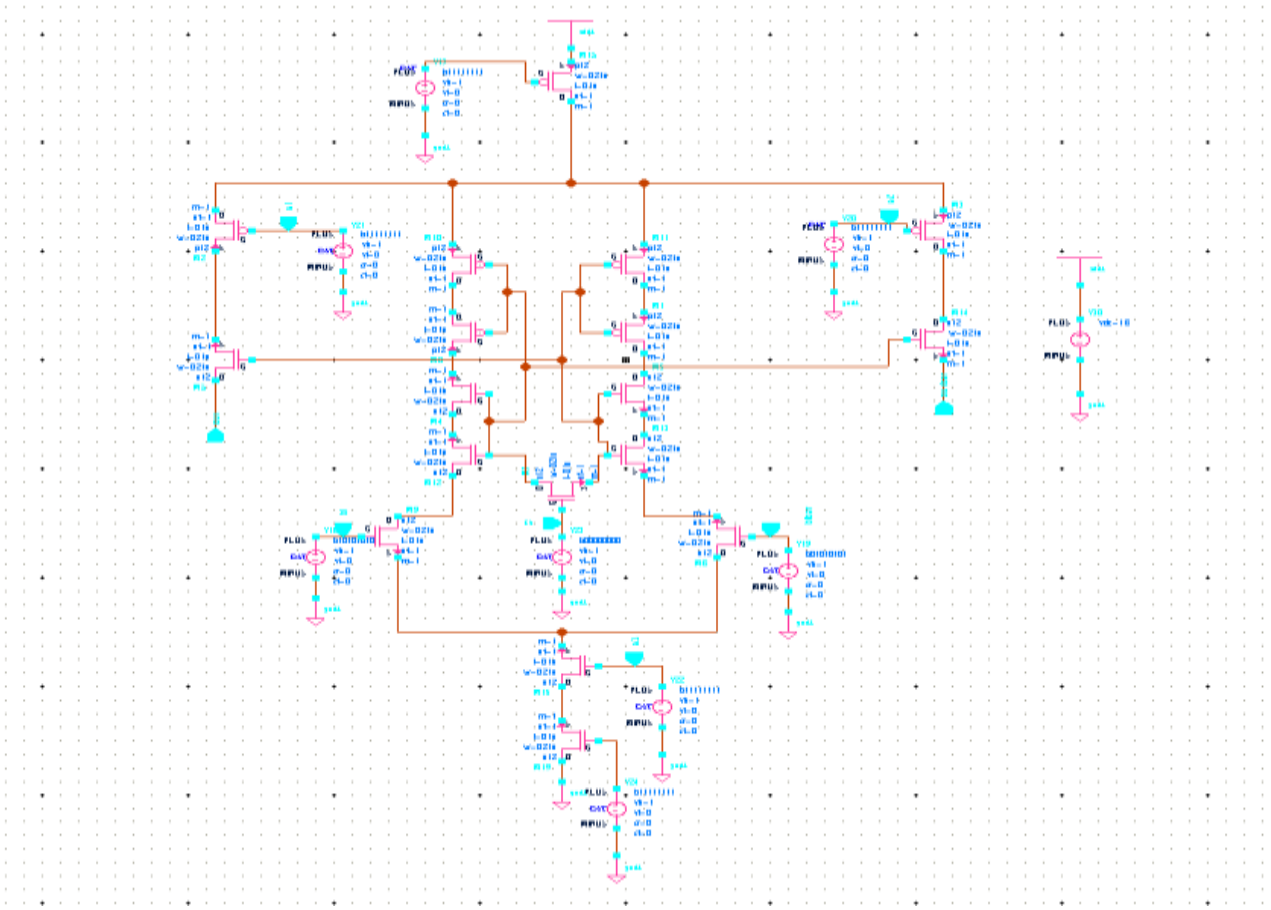

Figure 12. Schematic view of alpha latch based using sleepy stack technique

Figure 13. Output of alpha latch based using sleepy stack technique

Alpha latch based using leakage feedback technique

The figure 14 shows the schematic view of alpha latch based using leakage feedback technique in Custom Designer Schematic Editor.

Output of Alpha latch based using leakage feedback technique

The figure 15 is the output of alpha latch based using leakage feedback technique and it is simulated in Wavelet Analyzer using Custom design. The input values are bl=01101001, blbar=10010110 and the output values obtained are out =01101001, out bar=10010110. The enable signals were given accordingly which enables the respective transistors. The table 1 shows the power calculation for sense amplifiers.

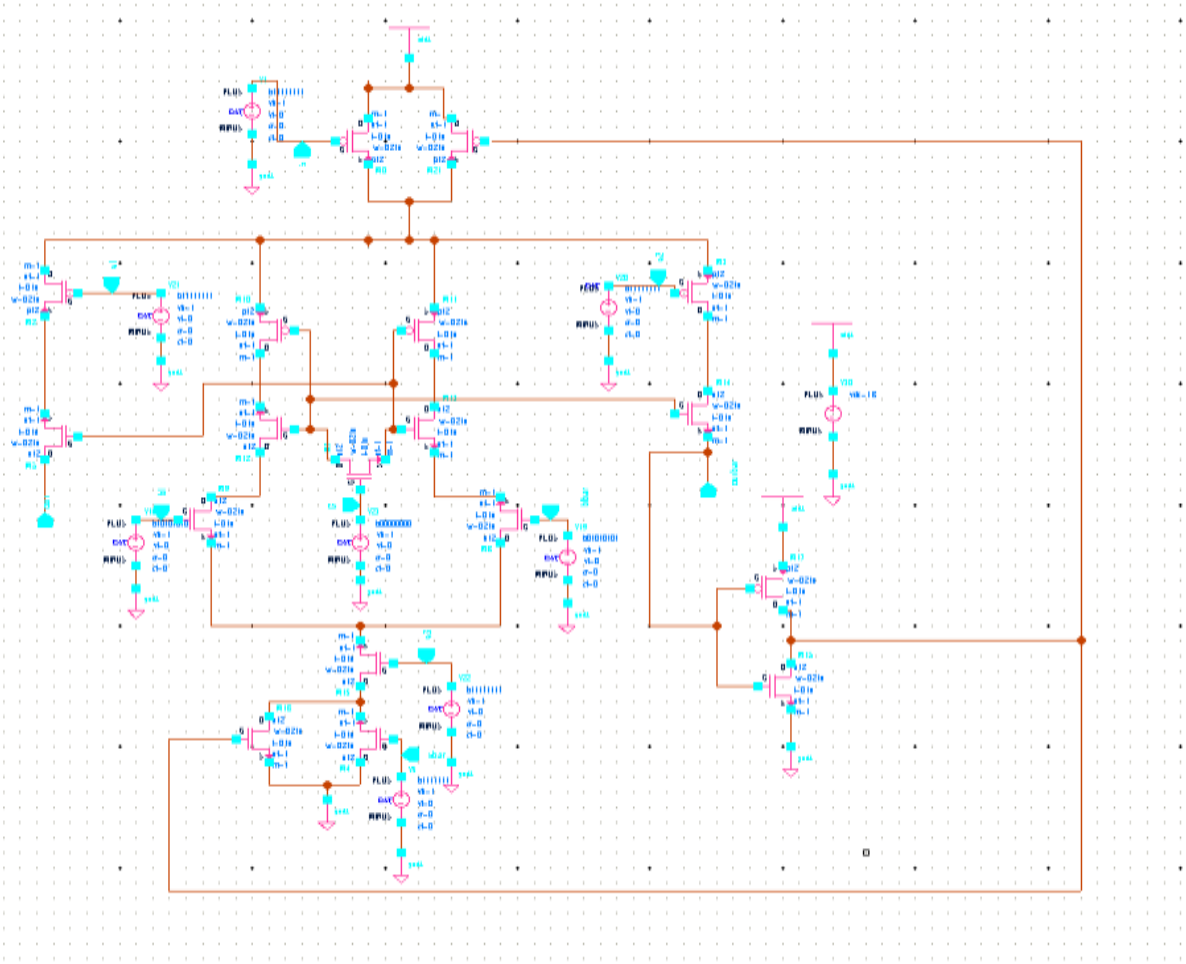

Figure 14. Schematic view of alpha latch based using leakage feedback technique

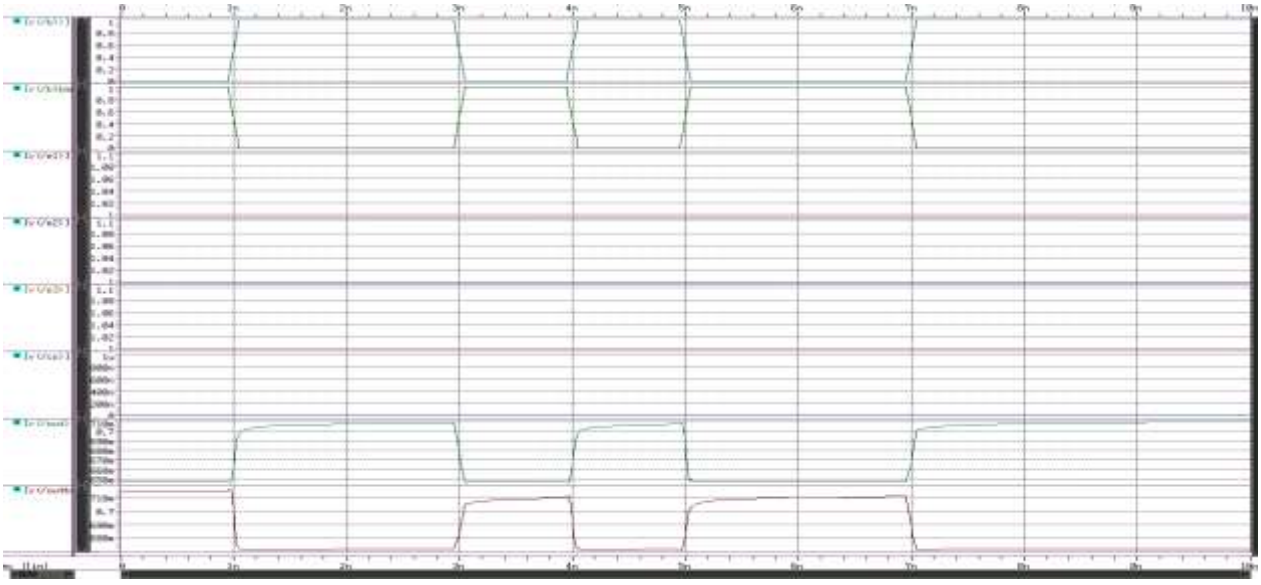

Figure 15. Output of alpha latch based using leakage feedback technique

Table 1. Power computation for sense amplifiers at different supply voltages

Different sense amplifier designs	Power Dissipation (Micro Watts)			
	1.2V	2V	2.5V	2.9V
Alpha latch based sense amplifier	22.7	39.8	61.4	86.7
Alpha latch based sense amplifier with stack technique	10.8	21.2	34.9	52.2
Alpha latch based sense amplifier with sleep transistor technique	8.3	18.7	20.3	32.6
Alpha latch based sense amplifier with sleepy stack technique	7.1	17.4	19.7	28.8
Alpha latch based sense amplifier with leakage feedback technique	7	16.8	18.5	28
Current mirror based sense amplifier	34.7	42.3	53.6	74.3
Current mirror based sense amplifier with stack technique	17.3	20.2	31.4	58.6
Current mirror based sense amplifier with sleep transistor technique	14.7	18.6	28.7	50.6
Current mirror based sense amplifier with sleepy stack technique	12.6	15.6	23.4	39.6
Current mirror based sense amplifier with leakage feedback technique	12.2	14.7	22.6	37.9

Conclusions

In the present work stack technique, sleepy stack technique and leakage feedback technique are adopted in current mirror based and alpha latch based sense amplifier which helps in the reduction of power consumed by sense amplifiers. The power is reduced to a desirable extent .Thus on reducing the power consumed by sense amplifiers ,the entire circuit's power is successfully reduced as well as delay during read operation in memory is minimized. This project is being used under 100 nm technologies with the help of Synopsys custom designer tool. In Future, this proposed sense amplifier which consumes low power can be used in automotive current monitoring, notebook computers, DC motor controls, battery chargers. This architecture can be further modified to achieve very low read delay and low power consumption.

Conflicts of Interest

Authors declare no conflict of interest.

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