Implementation of Mitigating Techniques for the Analysis of Delay Degradation to Reduce NBTI Effect in VLSI Circuits

B. SAIRAM
UG Student, Dept. of ECE, GVPCOE(A)

G. D. D. VAMSI
UG Student, Dept. of ECE, GVPCOE(A)

CH. D. DEEPTHI
UG Student, Dept. of ECE, GVPCOE(A)

B. MOHAN
UG Student, Dept. of ECE, GVPCOE(A)

Dr. V. LEELA RANI
Associate Professor, Dept. of ECE, GVPCOE(A)

Abstract: Nowadays, Transistor aging is major reliability concern for Nano scale CMOS technology that significantly reduce the operation life time for VLSI circuits. Negative Bias Temperature instability (NBTI) is a major contributor to the transistor aging that effects the CMOS devices and it is more prone to PMOS devices. Magnitude of the threshold voltage also increases due to NBTI in the MOS devices which leads to increase in gate delay. The above induced delay degradation effects the critical path timing analysis in the design which leads to failure of the circuit functionality. This paper presents various mitigating techniques to reduce the NBTI induced delay degradation which improves reliability of the ICs. Duty cycle variation method and Transistor Network Restructuring methods are implemented in this paper. Sleep Transistor insertion method is also proposed in this paper to reduce effects due to NBTI stresses. Various circuits are simulated using HSPICE tool with 45nm characterization library based on PTM (Predictive Technology Model) transistor model. From the simulation results it is observed that the proposed sleep transistor insertion method exhibits less delay degradation over 10 years compared to other existing methods like duty cycle method and transistor network restructuring method.

Keywords: *Negative Bias Temperature Instability (NBTI), Stress, Recovery, Duty Cycle Variation Method, Transistor Network Restructuring Method, Sleep transistor Insertion Method.*

I. INTRODUCTION

The circuit reliability, usually measured by "Failure-in-Time (FIT)", has become a critical concern for nanoscale technologies [1]. Advancements in technology scaling lead to increased leakage currents and aging effects. These are becoming critical concerns in present day nanoscale technologies [2].

This paper elaborates the Negative Bias Temperature Instability (NBTI) effect which is currently one of the major factors causing reliability degradation [3-7]. It is caused by the combination of negative biased gate voltage and elevated temperatures, Negative Bias Temperature Instability (NBTI) effect causes a significant loss in circuit performance and lifetime. The NBTI effect can incur an increase in threshold voltage as much as 50mV that results in approximately 10% increase in delay over 10 years [3].

Negative Bias Temperature Instability (NBTI) Effect

NBTI effect is predominant in PMOS devices as they are negatively biased when they are conducting [2]. Besides temperature, the other root factor that promotes the NBTI effect is the electric field that sets up across the gate-oxide when gate-to-source voltage is applied. In traditional technologies, the NBTI is not a severe problem because the electric field across gate oxide is small. However, in present day highly scaled technologies, the gate-oxide are made thinner and thinner. Applying a supply voltage which is not proportionally downscaled for thinner gate-oxide sets up a strong electric field across it [1]. Such a strong electric field is enough to cause atomic disruptions at elevated temperatures, which leads to NBTI effect.

NBTI effect is caused by disassociation of Si-H bonds at the substrate and metal-oxide (Si/SiO2) interface. The Hydrogen diffuses into the substrate in a temperature dependent reaction leaving behind the interface traps [3,4]. The interface traps are interfacing trivalent silicon atoms with an unsaturated valence electron, that are formed at the Si-SiO2 interface. The Interface traps are referred to as permanent due to their extremely slow recovery time. The formation of interface traps causes variations in fixed charge density and interface-trapped charge density results in threshold voltage degradation [4]. The variation in threshold voltage has an adverse effect on drain-to-source current, propagation delay and on frequency of operation. Thus, NBTI effect ultimately results in the failure of

the device. Over the time, there evolved several mitigating and compensating techniques to reduce NBTI effect in PMOS devices. This paper presents the implementation of various mitigating techniques like Duty Cycle Method and Transistor Network Restructuring Method. Sleep Transistor Insertion method is also proposed in this paper to reduce NBTI stress. This paper is organized as follows: Section I introduces about NBTI, section II gives the related work, section III proposes a new method and section IV presents results and analysis.

II. RELATED WORK

DUTY CYCLE VARIATION METHOD

Every PMOS device effected by NBTI effect undergoes two phases, the stress phase and the recovery phase [4]. A device undergoes stress phase when it is in on state and it is in recovery phase when the device is in off state. In recovery phase, the stressed device undergoes a reverse mechanism of NBTI to recover its stress. Thus, the mutually exclusive probabilities of the input signal to turn on and turn off the device governs the stress phase, and the recovery phase.

Input signal with different duty cycle variations is shown in Fig. 1. If a traditional input signal with 50% duty cycle is applied to the device the recovery time compensates the stress time and the NBTI effect remains unaffected. On the contrary, by applying an input signal with probability of off time more than probability of on time, say like in 75% duty cycle for a PMOS device, the recovery phase is larger than the stress phase. Hence, the device undergoes comparatively low stress resulting in reduced NBTI effect over the time. Thus, Duty Cycle Variation method aims at reducing dynamic NBTI effect by attaining larger recovery phase by altering the duty periods of the input signal.

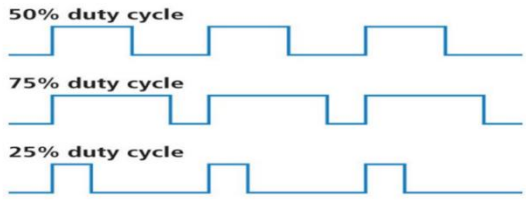

Fig. 1 Different Duty Cycle Variations

TRANSISTOR NETWORK RESTRUCTURING METHOD

Different logic functions can be designed with various transistor network structures. Fig. 2 shows logically equivalent 3 input AND-OR-INVERT gates after transistor network restructuring is applied. Such networks exhibit different power consumption and delay behaviours with identical logic functions. Hence, they suffer with different levels of delay degradation [2]. It is already stated above, that stress imparted on a device is directly proportional to the probability of the input signal to turn on the device. By applying all the input signals with equal probabilities, PMOS transistors that are connected directly to the power supply suffer more stress than the ones that are not directly connected to the power supply. Thus, this method aims at restructuring the transistor network to reduce the number of transistors that are directly connected to the power supply.

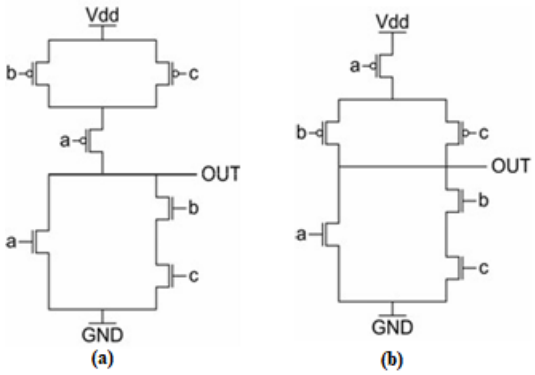

Fig. 2 (a) 3 input AND-OR-INVERT gate (b) 3 input AND-OR-INVERT gate with Network Restructuring [2]

Besides network restructuring, implementing a logic function in NOR realization is preferred than NAND realization [2]. This is because in NOR realization, transistors in the pull-up network are in stack unlike in NAND realization where they are in parallel. When the transistor stack is considered, unlike in parallel structure the stress on each PMOS transistor stack does not only depend on its signal probability but also on the probabilities of inputs to other devices above it, in the stack. On restructuring the transistors in stack experience less stress all together and in turn gives less delay degradation.

III. PROPOSED METHOD

SLEEP TRANSISTOR INSERTION METHOD

In Sleep Transistor Insertion Method, internal nodes or gate outputs are forced to specific logic values. Sleep Transistor Insertion Method can be implemented by additional control circuitry at the output of each controlled gate as shown in Fig. 3.

Sleep Transistor Insertion Method forces the states of individual node or gate outputs to specific logic value. In this technique, a gate can be modified to allow its output to be forced to either high or low level. For logic gates like NAND having parallel pull

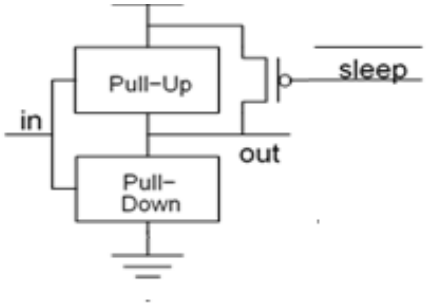

Fig. 3 Sleep Transistor Insertion Method

up circuits, the source node of each PMOS transistor is at HIGH i.e. at logic 1 and each transistor is stressed whenever the input is logic 0. PMOS transistors connected to power supply are affected more with stress than other transistors in the stack. Consider a two input NAND gate, where output gives logic '1' when one of its input is logic '0'. For a test case of "00" at the input of two input NAND gate, both PMOS transistors in pull up circuit are stressed with logic '0' at their gate inputs respectively. In this test case, second input of the NAND gate which is carrying logic '0' has no priority in generating logic '1' at the gate output. Hence, this second input node can be forced to logic '1' to make the respective PMOS transistor stress free. The proposed sleep transistor insertion method forces such nodes and makes PMOS transistor stress free for NBTI reduction.

IV. RESULTS AND ANALYSIS

Fig. 4 to 8 are the test circuits considered for verification of existing and proposed methods. Tables 1 to 5 presents the simulation results of test circuits for duty cycle method, transistor network restructuring and Sleep transistor insertion methods over the 10 years. Simulation results explores that proposed method has achieved less delay degradation over 10 years compared to existing methods. Table 6 gives the comparison of all methods after 10 years. Thorough investigation of proposed method on different benchmark circuits proves that proposed method has achieved less NBTI delay degradation compared to all other methods.

TEST CIRCUITS

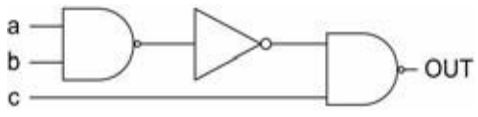

Fig. 4 Three input AND-OR-INVERT gate

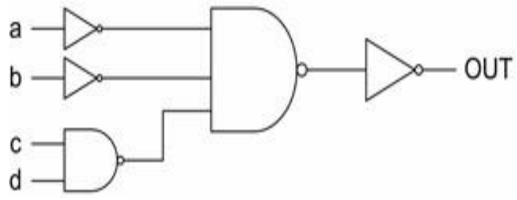

Fig. 5 Four input AND-OR-INVERT gate

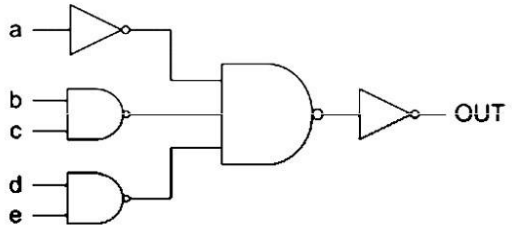

Fig. 6 Five input AND-OR-INVERT gate

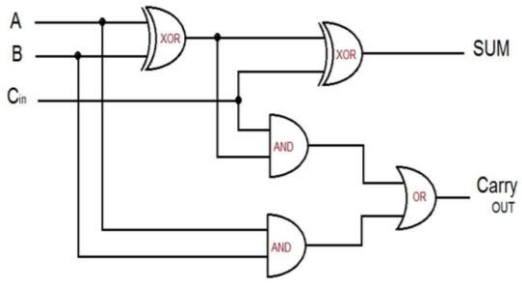

Fig. 7 Full Adder

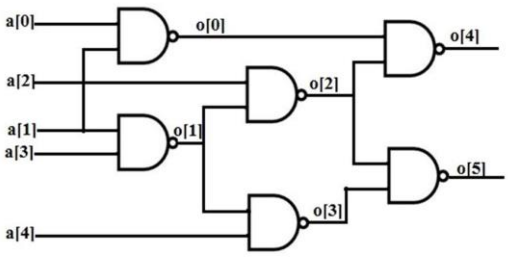

Fig. 8 C17 Benchmark circuit

SIMULATION RESULTS

Table 1. Simulation results of Three input AND-OR-INVERT gate

Test Circuit	Year Wise Analysis	Duty Cycle Variation Method		Transistor Network Restructuring Method	Sleep Transistor Insertion Method
		50% duty cycle	75% duty cycle		
		Delay (ns)	Delay (ns)	Delay (ns)	Delay (ps)
Three input AND-OR-INVERT gate	Current Year	6.2040	5.0632	4.2236	14.795
	After 3 Years	6.2056	5.0700	4.2257	15.638
	After 5 Years	6.2064	5.0745	4.2269	17.946
	After 7 Years	6.2073	5.0778	4.2279	22.927
	After 10 Years	6.2078	5.0819	4.2290	25.337

Table 2. Simulation results of Four input AND-OR-INVERT gate

Test Circuit	Year Wise Analysis	Duty Cycle Variation Method		Transistor Network Restructuring Method	Sleep Transistor Insertion Method
		50% duty cycle	75% duty cycle		
		Delay (ns)	Delay (ns)	Delay (ns)	Delay (ps)
Four input AND-OR-INVERT gate	Current Year	9.2169	6.5405	6.5140	8.5059
	After 3 Years	9.2420	6.5479	6.5299	12.598
	After 5 Years	9.2457	6.5480	6.5323	21.427
	After 7 Years	9.2480	6.5498	6.5342	23.576
	After 10 Years	9.2509	6.5508	6.5362	24.462

Table 3. Simulation results of Five input AND-OR-INVERT gate

Test Circuit	Year Wise Analysis	Duty Cycle Variation Method		Transistor Network Restructuring Method	Sleep Transistor Insertion Method
		50% duty cycle	75% duty cycle		
		Delay (ns)	Delay (ns)	Delay (ns)	Delay (ps)
Five input AND-OR-INVERT gate	Current Year	14.577	10.191	10.155	7.1417
	After 3 Years	14.610	10.216	10.160	7.4351
	After 5 Years	14.614	10.218	10.160	13.358
	After 7 Years	14.617	10.220	10.161	15.298
	After 10 Years	14.620	10.223	10.161	30.691

Table 4. Simulation results of Full Adder

Test Circuit	Year Wise Analysis	Duty Cycle Variation Method		Transistor Network Restructuring Method	Sleep Transistor Insertion Method
		50% duty cycle	75% duty cycle		
		Delay (ns)	Delay (ns)	Delay (ns)	Delay (ps)
Full Adder	Current Year	10.295	6.9647	6.9522	19.390
	After 3 Years	10.297	6.9669	6.9529	27.247
	After 5 Years	10.298	6.9678	6.9533	32.433
	After 7 Years	10.298	6.9684	6.9537	41.290
	After 10 Years	10.298	6.9694	6.9543	64.673

Table 5. Simulation results of C17 Benchmark Circuit

Test Circuit	Year Wise Analysis	Duty Cycle Variation Method		Transistor Network Restructuring Method	Sleep Transistor Insertion Method
		50% duty cycle	75% duty cycle		
		Delay (ns)	Delay (ns)	Delay (ns)	Delay (ps)
C17 Benchmark Circuit	Current Year	14.153	6.2695	3.3529	30.104
	After 3 Years	14.158	6.2711	3.3578	42.872
	After 5 Years	14.158	6.2713	3.3585	55.603
	After 7 Years	14.159	6.2714	3.3590	74.790
	After 10 Years	14.160	6.2716	3.3597	95.556

Table 6. Comparison of Delay Degradation after ten years

Test Circuit	Duty Cycle Variation Method		Transistor network restructuring method	Sleep Transistor Insertion method
	50% duty cycle	75% duty cycle		
	Delay (ns)	Delay (ns)	Delay (ns)	Delay (ps)
3 input AND-OR-INVERT gate	6.2078	5.0819	4.2290	25.337
4 input AND-OR-INVERT gate	9.2509	6.5508	6.5362	24.462
5 input AND-OR-INVERT gate	14.620	10.223	10.161	30.691
Full Adder	10.298	6.9694	6.9543	64.673
C17 Benchmark circuit	14.160	6.2716	3.3597	95.556

V. CONCLUSION AND FUTURE SCOPE

Delay degradation due to NBTI effect is a threat to the reliability of VLSI CMOS circuits. NBTI prediction and analysis at the early stages of the design flow can increase the performance and ensure reliability of the circuit. In this paper the simulation-based analysis of the NBTI was considered, and it was used to evaluate the NBTI impact on different CMOS test circuits. Duty Cycle Method, Transistor Network Restructuring method and proposed Sleep transistor insertion method are presented in this paper to minimize the impact of NBTI stress. Placement of Sleep transistors in proposed method allows the outputs of a gate to be forced to a specific value which lead to reduction in static NBTI induced delay. Thorough investigation of proposed method proves that proposed method has achieved less NBTI delay degradation compared to existing methods This concept of NBTI can also be tested on larger Fan-In test circuits. Effects of Positive Bias Temperature Instability (PBTI) can be estimated in future.

VI. REFERENCES

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