SRAM Designing using FinFET Technology- A review

Pulkit Gupta[1], Shweta Agrawal[2]

[1]*M.tech Scholar,Pulkit Gupta, ShriRam College Of Engineering & Management, Banmore, Morena (M.P.) India*

[2]*Assistant Professor, Shweta Agrawal, ShriRam College Of Engineering & Management, BanmoreMorena (M.P) India*

Abstract- CMOS technology is the most feasible semiconductor technology but it fail to perform as per expectations beyond and at 32nm technology node due to the short channel effects. Multigate FET technology like FINFET is successor of MOSFETs at 32nm and beyond. In this paper, we have reviewed SRAM designing using FinFET Technology and a Introduction about FinFET Technology is presented.

Keywords- FinFET, SRAM, 32nm

I. INTRODUCTION TO FINFET TECHNOLOGY

FinFET, generally called Fin typeField Effect Transistor, is a sort of non-planar or "3D"transistor used as a piece of the outline of present day processors. As in earlier, planar outlines, it depends on a SOI (silicon on encasing) substrate. Regardless, FinFET outlines similarly use a coordinating channel that climbs over the level of the encasing, influencing a thin silicon to structure, formed like an edge, which is known as a passage terminal. [1] This sharp edge shaped cathode empowers various ways to chip away at a singular transistor... Regardless of the way that present conduction is in the plane of the wafer, it isn't completely a planar gadget.[2] Or perhaps, it is insinuated as a semi planar device, since its geometry in the vertical heading (viz. the adjust stature) in like manner impacts device lead. Among the DG-FET composes, the FinFET is the slightest requesting one to produce.

II. SRAM Cell

A low power SRAM cell might be composed by utilizing cross-coupled CMOS inverters. The most imperative favorable position of this circuit topology is that the static power dispersal is little; basically, it is restricted by little spillage current. Different points of interest of this outline are high commotion resistance because of bigger clamor edges, and the capacity to work at bring down power supply voltage. The significant impediment of this topology is bigger cell estimate. [3]The circuit structure of the full CMOS static RAM cell .The memory cell comprises of basic CMOS inverters associated consecutive, and two access transistors. The entrance transistors are turned on at whatever point a word line is actuated for perused or compose task, interfacing the cell to the corresponding bit line segments. A run of the mill 6T SRAM cell is made up six transistors.[4] Two sets of inverters are associated with the end goal that the yield of one is nourished to the contribution of the other and the other way around. This input association balances out the capacity hubs in the cell. Two different transistors are utilized as access transistors and are associated with the capacity hubs (Q and QB) of the two inverters. The signs word line (WL), bit line (BL) and bitlinebar (BLB) control the task of the cell. At the point when WL is high, the entrance transistors are turned on giving the entrance to the capacity hubs [5].For read mode, both bl and blb are high and for compose mode they are either 0 and 1 or 1 and 0, comparing Q and Qbar are put away, in both read and compose case, world line is high, for hold mode, world line is low. Figure 1 shows SRAM Design and figure 2 is SRAM cell using FinFET.

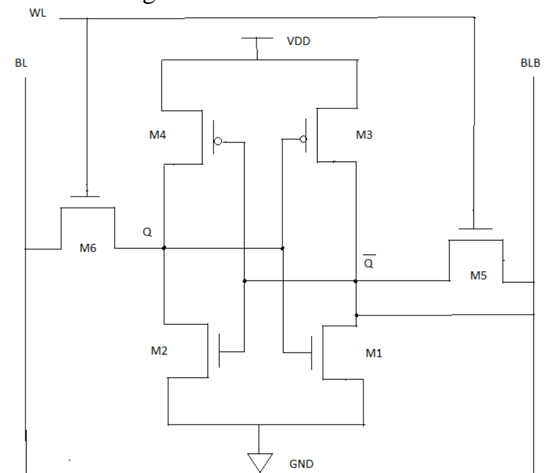

Fig.1: SRAM Design

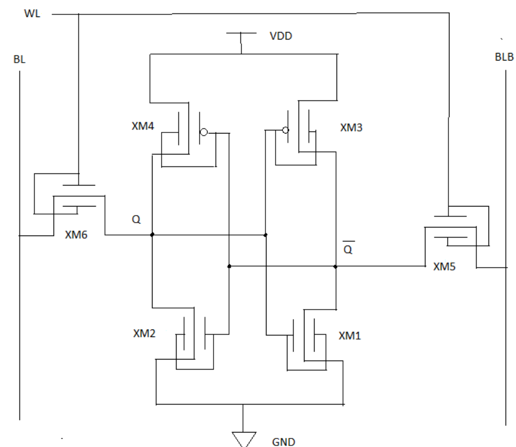

Fig.2: SRAM Design cell using FinFET

III. CONCLUSION

The fundamental plan go for VLSI (very-large-scale integration) architects is to meet execution prerequisites inside a power spending plan. Hence, control productivity has expected expanded significance. This task investigates how

FINFET innovation is a substitute for mass CMOS innovation past 32nm innovation hub and offer intriguing deferral control tradeoffs. Hence, FinFET is a promising substitute for MOSFET in the SRAM cell design below 32nm.

IV. REFERENCES

[1]. Ajay N. Bhoj, and Niraj K. Jha, “Design of Logic Gates and Flip-Flops in High-performance FinFET Technology” IEEE Transactions on very large scale Integration (VLSI) systems, pp. 1-14, 2013.

[2]. R.Rajprabu,V. Arun Raj, R. Rajnarayanan, S. Sadaiyandi, V. Sivakumar, “Performance Analysis of CMOS and FinFET Logic” IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) vol. 2, no. 1), pp. 01-06 , 2013

[3]. SudarshanPatil, V S KanchanaBhaaskaran, “Optimization of Power and Energy in FinFET Based SRAM Cell Using Adiabatic Logic” International Conference on Nextgen Electronic Technologies: Silicon to Software, pp. 394-402, 2017.

[4]. Vivek Kumar, VikasMahor, and Manisha Pattanaik, “Noval Ultra Low Leakage FinFET Based SRAM Cell” IEEE International Symposium on Nanoelectronic and Information Systems (iNIS),pp. 89-92,2016.

[5]. Nidhi Sharma,“ Ultra Low power Dissipation in 9T SRAM Design by Using FinFET Technology” International Conference on ICT in Business Industry and Government (ICTBIG), pp.1-5, 2016.

[6]. C. B. Kushwah, DeveshDwivedi, Sathisha N, Krishnan S Rengarajan, “A Robust 8T FinFET SRAM Cell with Improved Stability for Low Voltage Applications” 20th International Symposium on VLSI Design and Test (VDAT),pp. 1-6, 2016.

[7]. Navneet Kaur, Hitesh Pahuja, Neha Gupta, SudhakarPanday, and Balwinder Singh, “Low Power FinFET Based 10T SRAM Cell” Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH),pp. 227-233, 2016.

[8]. Neha Yadav and Ashish Kumar Singhal, “Modelling and Performance Analysis of Various FinFET Based Design Techniques for XOR and XNOR Circuits at 45 Nano meter Regime” International Journal of Advanced Electronics & Communication Systems, vol. 2, no.9, pp. 780-785, 2014.

[9]. Khushboo Mishra and ShyamAkashe, “Design different topology for reduction of low power 2:1 multiplexer using FinFET in nanometre technologies” International Journal of Nanoscience, vol. 12, no. 4, pp. 1-12, 2013.

[10]. Young Bok Kim ,Yong –Bin Kim, and Fabrizio Lombardi, “New SRAM Cell Design for Low Power and High Reliability using 32nm Independent Gate FinFET Technology” IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems, pp. 25-28, 2008.