Implementation of Low Power Vedic Multiplier

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Abstract—In upcoming years power minimization has become an important aspect in the circuit designing .One such device named Multiplier used in many applications like image processing, filter designing and in designing Arithmetic Logic unit is taken up in this paper for optimization of the power . The proposed multiplier is designed using URDHVA TIRYAKBHYAM algorithm, an ancient technique that is used in Vedic sciences. This multiplier here is designed using adder that is implemented from reversible logic. The Designed of the proposed multiplier is implemented in 90nm technology using CADENCE VIRTUSO tool. A significant power reduction has been observed in the designed multiplier as compared to the earlier ones.

Keywords—*Vedic Multipier,low power design, CMOS, reversible logic*

I. INTRODUCTION

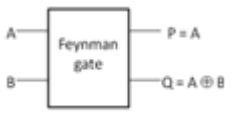
With the increase in advancements in VLSI technology the demand for low power and high speed circuits have been increased significantly. One such key component used in many applications like image processing, low power circuit designing ,filter designing and microprocessors is the multiplier .The speed and efficiency of the multiplier depends on the computational steps that are required for the generation of partial products and the power performance further depends upon the type of the adders used .The algorithm selected for designing the multiplier also defines the performance parameter of it .A lot of research has been done in this field but still there is scope of improvement in this field as far as power is considered . There always exist a tradeoff between power and delay parameter .Working on one will effect inversely on the other but in this paper we are considering power as a major factor in performance calculation of the multiplier .The Vedic mathematics was derived from the Indian scriptures and Vedas by Swami Bharati Krishna Maharaja after eight years of discovery of Vedas

A. Reversible gate

Logically a gate is said to be reversible if it consists of equal number of outputs and inputs .It can also be said that a reversible logic gate has one to one mapping as compared to the earlier irreversible gates. The other advantage of reversible gate is the input can be restored from the output value that saves the unused power.

Up till now several logically reversible gates have been proposed. There are approximate 44 reversible gates that are designed till now Out of them a few that are used in our research are Feynman gate[9], Toffoli gate[9],DFG gate,NOT gate, and Peres gate[9]

A brief comparison of the functionalities of these gates have been shown in figs.1-4.These reversible gates are normally 2 x2 and 3x3 in nature. This means there are 2 inputs –and 2 output in 2 x2 gate similarly a 3x 3 reversible gate will have 3 input and 3 outputs .Besides 2 x2 and 3x3 there also exist 4x4 reversible gate one such example of it is BVF. Various types of combinational circuits can be designed using these reversible gates and there performance can be analyzed.



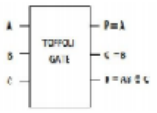
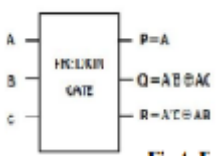


Fig.1.Feynman gate [9] Fig 2.Toffoli gate [9]



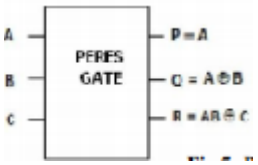


Fig.3.Fredkin gate [9] Fig 4. Peres gate

Many Binary Adders have been designed using these gates .A few of the Adders that can designed using the reversible logic are Carry Look ahead Adder, Carry save adder, Carry Skip Adders and Carry Select adder. Two numbers

B. Terms used in defining the performance of reversbile logic

Commonly used terms in reversible logic designing are Garbage output (GO)-this is basically the unused port in the circuits. In Designing of the circuits GO should be kept minimum .The other parameters that is used is the number of constant inputs. In any circuit designing ,to obtain the required functionality of the system ,the number of inputs that are kept constant i.e either set to 0 or 1 gives the number of CI(Constant inputs).Many other parameters like Transistor and Gate count can also be obtained of the reversible logic gates on implementation. Quantum cost or QC is yet another important parameter that plays an important role in designing the circuits .Besides these parameters there exists some design constraints that are associated with it [9] .Firstly the reversible logic does not allow fan-outs. Second main constraint of these gates is the reversible logic should have minimum number of constant inputs. The other Design constraints of these gates include use of minimum logic depth or minimum gate levels. The

Design should also be optimized to produce minimum garbage and quantum cost besides providing least power .However working on power always gives a tradeoff between delay so the application required defines the parameters that are needed to be optimized as incase of today's world the low power and portable devices are in demand . Area calculation also plays a significant role in layout designing of the circuits. In recent researches the reversible logic serves as a replacement for the proposed .On the contrary because of extensive use of multipliers in computer systems many circuits have been proposed for implementation of the multipliers taking an example in, Haghparast et al. Have proposed a two –part multiplier that is reversible in nature. In the first part of it he has explained the generation of the partial products while the second part of it does the addition with taking into account the previous results of partial products .This design uses an array of 16 PG gates for the generation of partial products and then addition is done using a circuit that consists of PG[9] and HNG gate[3] .Many other designs have been proposed by other researches .The only difference that exists in these circuits is the type of reversible gate used in generation of partial products and the sub circuit used for the addition of the partial products. There are two ways by which power consumption takes place in the multiplier. First is static power due to leakage currents in the circuits and second is dynamic power due to either switching activities or due to charging and discharging of the capacitances. Switching component is mostly responsible for power dissipation in multipliers. .

C. Vedic multplier

Multiplication of two numbers involves shifting of multiplier bits and subsequent addition[8] .The Vedic Multiplier that we have designed is of 4 bit and is implemented using Carry select adder that is designed using reversible logical gates having least power .The Vedic multiplier designed here is based on URDHVA TRIYAKBHAYAM algorithm .This method of multiplication is used as it reduces the calculations or the number of steps used in multiplications besides increasing the speed of the circuit .'Urdhva and Tiryakbhyam ' are the two words that are derived from Sanskrit literature .Basically 'Urdhva' means 'Vertically' and 'Triyakbhyam' means 'crosswise'[1]. So in Vedic multiplier vertical crosswise multiplication is performed as shown in the fig2. The figure shown below depicts the algorithm used for the multiplication and generation of partial products .This algorithm can be implemented for binary numbers, hex, and decimal number system .In this paper we have Proposed a Vedic multiplier for binary multiplication of two numbers [1]

The fig. shows an algorithm to multiply two numbers example 101 and 110.following steps are carried out in multiplication

Various steps in Algorithm [1]

1. First take the right hand digits and do the multiplication. This multiplication provides us LSB of the answer digit
2. The LSB digit of the top numbers is then multiplied by the second bit from the bottom number and the least significant bit from the bottom number is then multiplied by the second bit of the top number .These values are then added .
3. Then LSB of the bottom number is then multiplied with MSB of the top number ,LSB of the top number is also multiplied with the MSB of the bottom one and then further multiply the second bit of both further adding them both
4. Now just move one place to the left ,the step here is similar to the second step .Here we will be multiplying the second digit of the number with the MSB of the second number
5. The last step is multiply the LSB of both numbers together to obtain the final product value.

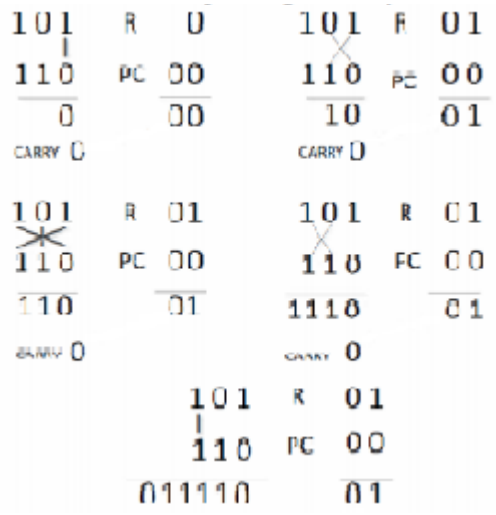


Fig.5 4x4 Multiplication using URDHVA TRIYAKBHAYAM algorithm [1]

To design a 4 x4 low power Vedic multiplier we have used 4- 2x2 Vedic multiplier that makes use of 4 Toffoli gate, 2 Peres gates. Besides that for addition of partial products we have used 3 Carry Select Adders that can be implemented using reversible logic gates .Finally a FRG(Fredkin gate) is used for designing a multiplexer The delay that is calculated is on rising edges and its value is 483.1ps while the power calculated while implementation is 2.458 mw. As there is a tradeoff between power and delay parameters so working on one will inversely affect the other parameters also

- A line diagram For Urdhva Multiplication of 2, 3 and 4 digits is shown in Fig 6.

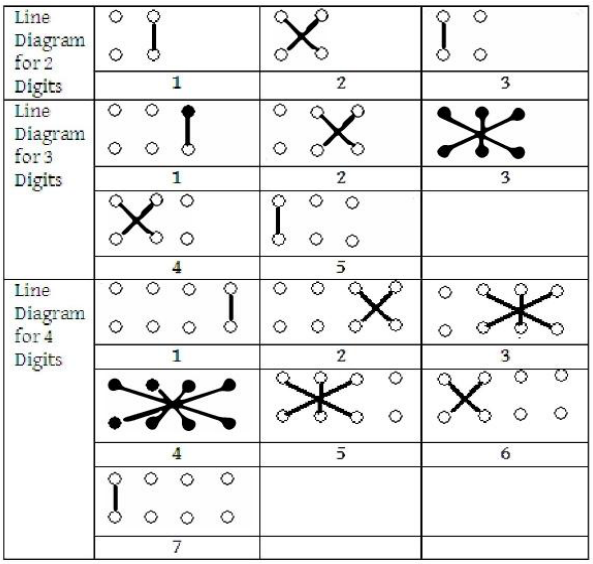


Fig.6.Line Diagram for 2, 3 and 4 digit Multiplication

- The computational power calculated of the Vedic multiplier using reversible gate is found to be less as compared to the conventional and other Vedic multipliers .The Table 1 and Table 2 shows different power analysis carried out for multipliers

Multiplier type	Delay
4x4 existing Vedic multiplier (design1)	14.517(ns)
4x4 Vedic multiplier (design2)	12.825(ns)
Proposed 4x4 Vedic multiplier	483.1ps

Table 1. Comparison of Different multipliers based on delay

Multiplier type(4x4)	Power	Delay
Array [3]Multiplier	56mw	22.035ns
Vedic [3]Multiplier design 3	52mw	16.910ns
CMOS technology	13.538mW	Not mentioned
Proposed Vedic Multiplier	2.458mw	483.1ps

Table 2. Comparison A graph within a graph is an "inset," not an "insert of different multipliers in terms of

D. Simulation results of 4 bit proposed multiplier

The simulation of the 4 x4 Vedic multiplier is carried on Cadence Virtuoso tool and waveforms were saved for differ rent multiplicands.

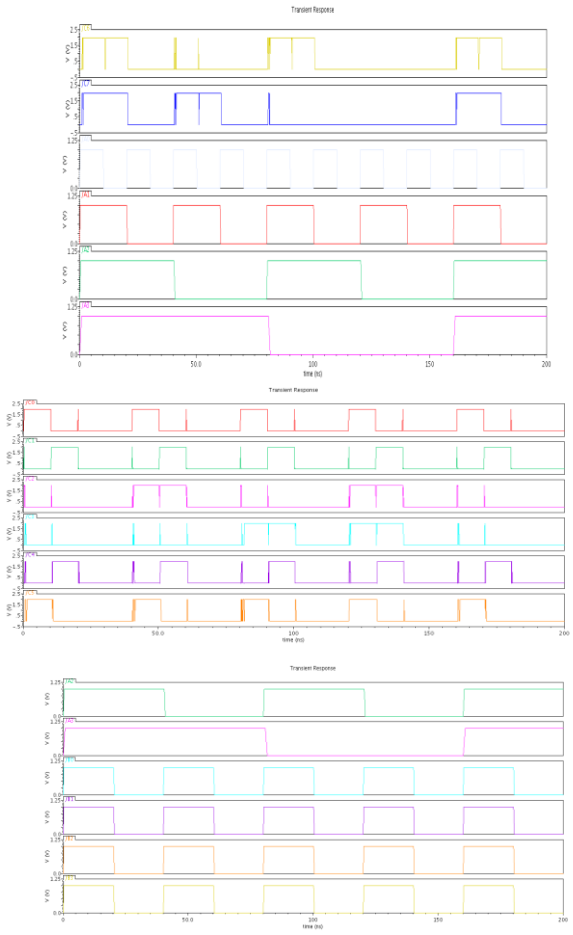


Fig.7.The output of proposed Vedic multiplierimplemented in Cadence Virtuose Tool at 90nm technology

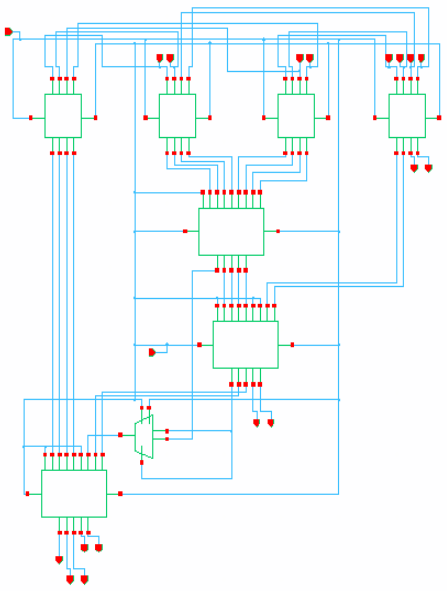


FIG.8. IMPLEMENTATION OF 4X4 VEDIC IN CADENCE VIRTUOSO AT 90NM

II. ACKNOWLEDGMENT

I acknowledge with deep sense of gratitude and invaluable time along with the sincere guidance given by my guide Prof.Narwant Singh Grewal, Guru Nanak Dev Engineering College, Ludhiana .A sincere gratitude to Dr.Sandeep Singh Gill, HOD, Department of Electronics and Communication Engineering, GNDEC, Ludhiana .I extend my regards to my family under whose guidance I was able to complete my work.

III. REFERENCES

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