A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator

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***Abstract*— A passive 2nd-order sigma-delta modulator using switched-capacitor based filters was designed, fabricated, and tested. A novel 2nd-order single feedback path topology is used. All circuitry is optimized for low power operation through the use of minimum size MOSFETs, component reduction and topology choice. The modulator was fabricated in On Semiconductor's C5 500-nm process. The implementation achieves a typical SNDR of above 50 dB for tested frequencies of 10 Hz to 3 kHz and has a peak SNDR of 57.8 dB, which corresponds to an ENOB of 9.3 bits. With a 2.5 V supply, the power consumption of the sigma-delta modulator is 6.75 µW. The modulator achieves a FOM of 1.78 pJ/step.**

I. Introduction

Currently, the vast majority of integrated circuit (IC) research and development is being done with deep nanometer CMOS processes. However, there is still room for further circuit refinement in older submicron processes, such as On Semiconductor's 500-nm C5 process. These older processes are still popular because of proven reliability in medical and automotive applications as well as their low cost. One major disadvantage in these older processes is higher power consumption due to large feature sizes. This results in a challenge for an IC designer who is trying to reduce power consumption while being limited to an older process. The proposed sigma-delta modulator provides a solution for a low power, 10-bit sigma-delta (∑-Δ) based data converter implemented on older submicron processes.

Sigma-delta analog to digital converters (ADC) are popular for high resolution, relatively low-frequency data conversion. The primary reasons for their popularity are the heavy reliance on digital components, low cost, and ease of implementation. Currently, most ∑-Δ ADCs use active integrators based on amplifiers. The rationale for this is to achieve resolutions predicted by ideal equations and simulations. Unfortunately, the use of an active integrator results in sacrificing a high portion of a power budget to biasing circuitry required by the amplifier. Replacing the active integrator with passive switched-capacitor (SC) based components can significantly reduce the power consumption of a ∑-Δ modulator. This allows a ∑-Δ ADC to be competitive with a low power successive approximation register (SAR) ADC.

II. Passive SC ∑-Δ Modulator Topology

The topology chosen for this ∑-Δ modulator is one that has been proven to be a good solution for passive topologies with a single feedback path [1]. Generally, passive ∑-Δ modulators are limited to 2nd-order noise shaping and this particular topology achieves this with only one feedback path. The continuous-time (CT) version of this topology is shown in Fig. 1. This is similar to the simplest possible 1st-order ∑-Δ topology but with an added RC filter within the loop. The main reason that this topology is better is that it reduces the voltage swing at the integration node which more closely approximates an ideal active integrator. The transfer functions are explained in detail in [1]. A disadvantage of the modulator in [1] is that it consumes static power due to the lumped passive components. Replacing the resistors with switched-capacitors eliminates static power consumption other than leakage currents. Another disadvantage of the modulator in [1] is that the component values are fixed. The components optimize the modulator for a particular bandwidth and clock frequency. Since the resistance of switched-capacitor values scale with clock frequencies, the corner frequencies of the filters scale as well. For example, if a low clock frequency is used, the filter will have a low corner frequency that is well suited for low input frequencies. For higher clock frequencies, the converse is true. The use of switched-capacitors in this topology results in an elegant design where clock, input, and filter corner frequencies are optimized.

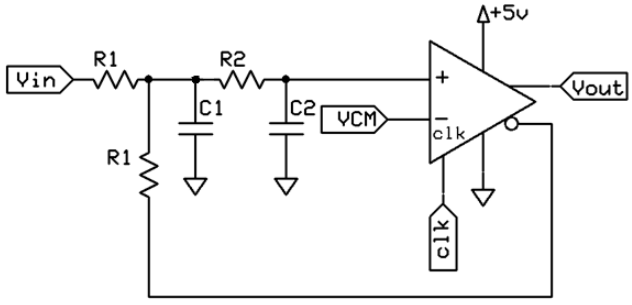

Fig. 1. CT 2nd-order ∑-Δ modulator.

The basic switched-capacitor resistor building block is shown in Fig. 2. This is a simple transmission gate (TG) based SC resistor. The equation for equivalent resistance is given in Fig. 2 with f_s as the clock frequency. Two non-overlapping (NL) clocks and their inverses are required for the proper operation of this type of SC resistor. Using TGs as the switches allows a rail-to-rail input range. They are also more linear than pass gate based switches. The disadvantage of a TG is that power consumption is higher than a pass gate and the inverted clock phases required for the PMOS devices.

Despite this, the linearity afforded by the use of TGs is worth the small increase in power use.

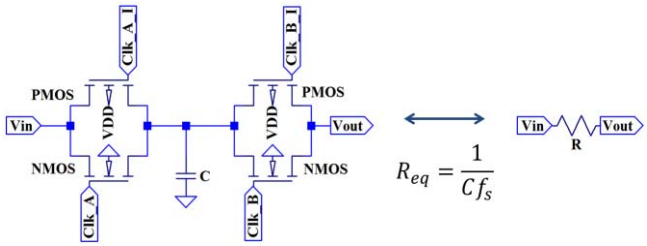

Fig. 2. TG based SC resistor.

A block diagram of the full modulator is shown in Fig. 3. The passive network seen in Fig. 1 is replaced with a switched-capacitor filter block composed of poly-poly capacitors and switched-capacitor resistors of the type shown in Fig. 2. The non-overlapping clock generator is used to create two clock phases, A and B. Two inverters are used to create the complementary clocks required by the PMOS devices in the switched-capacitor filter. The final component of this block diagram is the clocked comparator with complementary outputs. The inverted output is used to provide the required negative feedback.

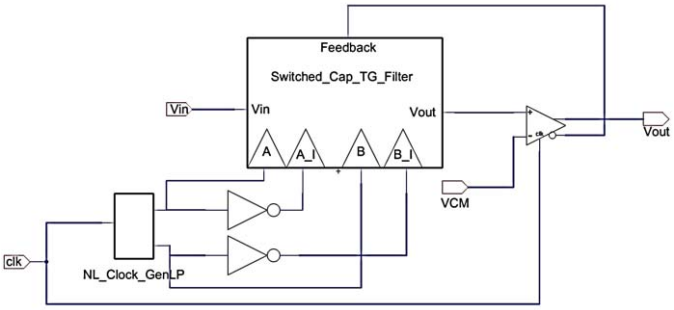

Fig. 3. Block diagram of 2nd order ∑-Δ modulator.

III. Circuit Design and Layout

In order to minimize power consumption, two main design choices were used whenever possible. These are to use minimum sized MOSFETs and to keep the number of parts as low as possible. Generally, NMOS and PMOS devices for digital logic are sized such that the transconductance is equal, resulting in equal drive strength and a switching point of half the supply voltage. In this design, NMOS and PMOS devices are the same size which results in the NMOS devices having higher drive strength. This is not a significant detriment to the performance of this circuit since most elements are clocked. All devices have a drawn length of 0.6 µm and a drawn width of 1.8 µm except for two long-length MOSFETs used in the input stage of the comparator which have a length and width of 1.8 µm.

The heart of the ∑-Δ modulator is the clocked comparator. There are a plethora of topologies to choose from. Since the goal in this case is low power, a memory sense amplifier topology was chosen [2]. Memory sense amplifiers need to be low power because they are used in high densities in DRAM chips. The circuit schematic of the clocked comparator is shown in Fig. 4. The circuit is composed of a cross-coupled latch connected to an S-R latch, which allows the output to change only on the rising edge of the clock. The output inverters are used for buffering the output signals. A voltage applied to either input NMOS device pulls down the voltage at the source of the device above it. This results in an increase in v_{gs} which causes the cross-coupled latch to switch. The length of the input devices must be long enough to create a sufficient voltage drop for this to occur. In order to reduce contention current, the input devices have long 1.8 µm channel lengths. All other devices are minimum size. When switching, the input devices form a direct path to ground. Using a long channel length limits the current that can flow to ground through this path. Another benefit to the long length is reduced kickback noise.

One limitation of this type of clocked comparator is the resolution of the inputs. This circuit can respond to input signal differences of a few millivolts. Below this level, the outputs will not switch. If the error signal from the summing junction is too small, then the modulator output can be stuck in a dead zone. This is one advantage of 2nd-order and higher ∑-Δ topologies. The error signal is more random, which limits the time that the modulator is stuck in a dead zone. However, the particular 2nd-order topology used in this design has another means by which to create a dead zone. The additional RC loop filter composed of R2 and C2 shown in Fig. 1 attenuates the input signal further by filtering it. In a previous work [1], it was shown that R2 and C2 should be as large as possible for improved SNDR. This approximates an ideal integrator more closely by reducing the voltage swing at the output of the integrator node. The expense of this is that the comparator must be able to resolve smaller input differences. Therefore, there is a trade-off in the amount of filtering and the resolution of the comparator. It is not possible to improve the resolution of this type of comparator without the use of pre-amps. The use of a pre-amp is discouraged as it will draw static power due to its biasing circuitry. An amplifier would be better utilized as an active integrator rather than as a means to improve the gain of a comparator. Therefore, the trade-off in limited comparator resolution and the resulting final modulator resolution must be accepted as a consequence of low power design.

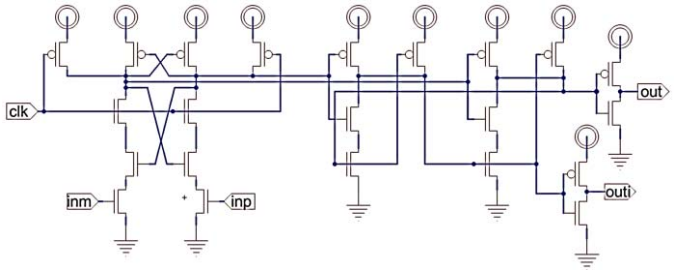

Fig. 4. Schematic of clocked comparator.

The design of the switched-capacitor filtering block is straightforward. The TG based SC resistor in Fig. 2 is substituted for each resistor in the CT design shown in Fig. 1. This type of SC resistor is sensitive to parasitics and charge injection. The effects of charge injection are negligible due to the large size of the capacitors. Furthermore, in this topology the relative matching between capacitors is important, not the actual values. Since parasitics apply proportionately to the size of the capacitor, the relative matching is not affected. The capacitors in these SC resistors are sized such that the value for R2 is 10 times larger than R1. The values for C1 and C2 are 10 pF. All capacitors are implemented using two layers of polysilicon in the C5 process. All TGs are minimum size to reduce power consumption. Although this results in unequal switching points, it does not matter since only full logic level signals are applied to the gates. For a nominal clock frequency of 1.024 MHz, the values for R1 and R2 are 1 MΩ and 10 MΩ, respectively. This results in corner frequencies of 16 kHz and 1.6 kHz, respectively. It is important to select a proper clock frequency so that there is enough bandwidth for the desired signal. Otherwise, the capacitors can be resized based on the desired input signal. This can be determined through the transfer functions given in [1], since the added loop filter causes behavior that may not be intuitively understood. In many cases, it is best to empirically determine the ideal filter characteristics through simulations.

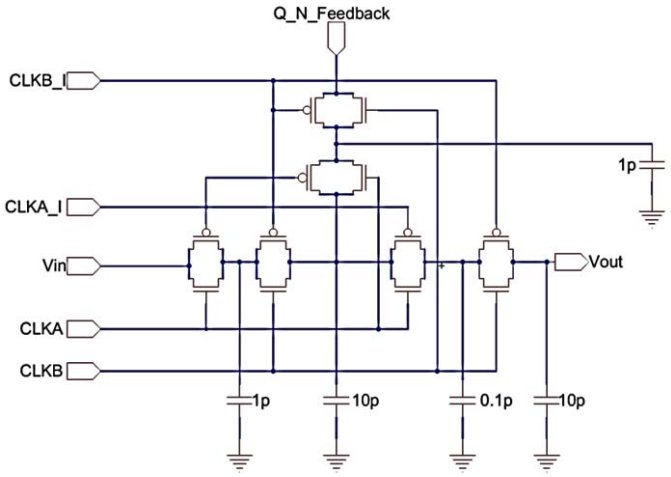

Fig. 5. Schematic of switched-capacitor filter block.

The SC resistors in this circuit require a non-overlapping clock generator. This is accomplished by using two cross-coupled NOR gates with delaying inverters to prevent clock edges from overlapping. The schematic of the NL clock generator is shown in Fig. 6. There are only two delay elements (inverters) in each clock phase. This was done to reduce power consumption. Generally, NL clocks use more delay elements and also use buffers at the outputs to prevent loading effects from changing the propagation time [3]. It was determined through layout-based simulations that output buffers were not required and that this design with only two inverters per phase is satisfactory for this application. All logic is made up of minimum size MOSFETs.

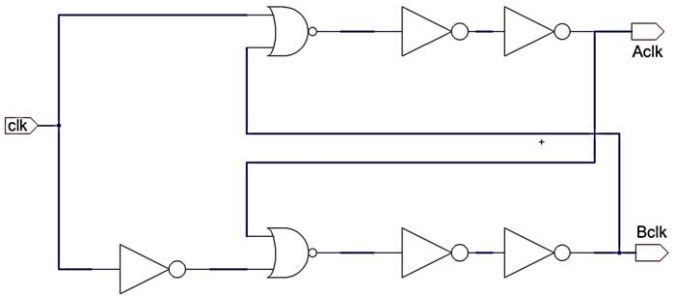

Fig. 6. Schematic of NL clock generator.

The full layout of the proposed ∑-Δ modulator was done using the Electric VLSI software. The dimensions of the layout are 405 µm by 385 µm. Since the main goal was to verify circuit operation, no particular effort was made to minimize the layout area. It should be possible to significantly reduce the area through the use of good routing practices. The vast majority of the area is occupied by the large 10 pF capacitors which can be a disadvantage of a passive ∑-Δ modulator. The chip was fabricated through the MOSIS service in On Semiconductor's C5 process. A micrograph of the portion of the chip containing the proposed ∑-Δ is shown in Fig. 7.

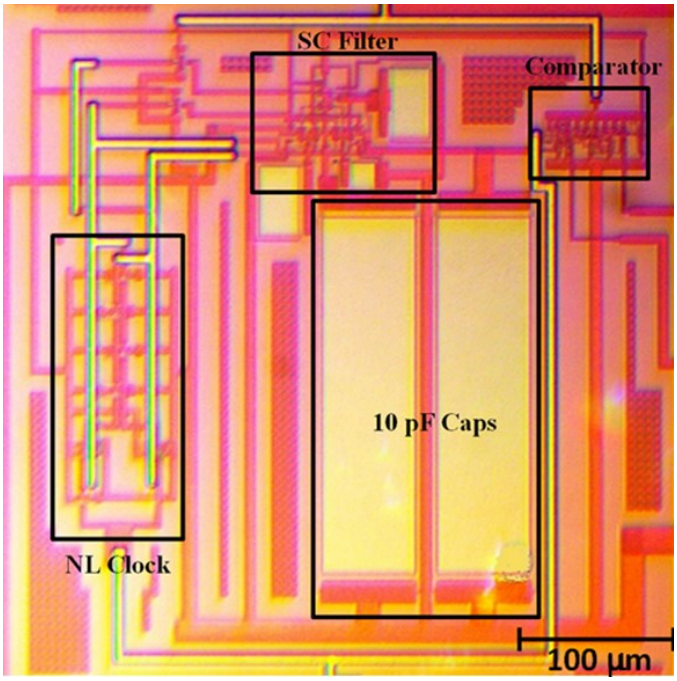

Fig. 7. Micrograph of complete ∑-Δ modulator.

IV. INTEGRATED CIRCUIT TEST RESULTS

The fabricated IC was tested in order to quantify its power consumption and signal-to- noise and distortion ratio (SNDR). A wide range of supply voltages were tested, but the

best performance was found to occur at 2.5 V. This makes the circuit well suited for LVCMOS logic levels. A low distortion function generator was used for the input signal which was a 0.75 V sine wave with a 1.25 V DC offset. The 1-bit output of the modulator was converted back to an analog approximation using a 2nd-order RC filter. The corner frequency of this filter was set such that for any given input frequency, the bandwidth is large enough to include the first five harmonics to give an accurate indication of SNDR. The output from this filter was analyzed using the FFT function of a 14-bit, 20 MHz PC based oscilloscope. The SNDR was calculated from this data. The resulting plot of SNDR as a function of input frequency is shown in Fig. 8. For each data point, the clock frequency was changed so that the corner frequency of the SC filters is above the input signal and its first five harmonics to ensure a realistic SNDR value. The peak SNDR of 57.6 dB occurred for an input frequency of 400 Hz, a clock frequency of 1.024 MHz, and a signal bandwidth of 3 KHz. This corresponds to an effective number of bits (ENOB) of 9.3. Under these conditions, the supply voltage and current were 2.5 V and 2.7 µA respectively, resulting in a power consumption of 6.75 µW.

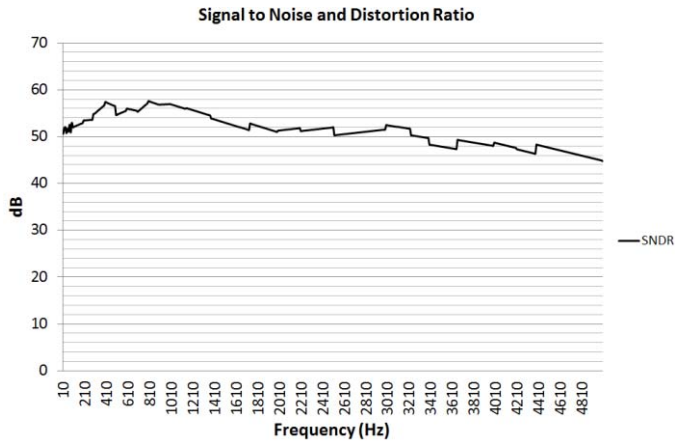

Fig. 8. Measured SNDR.

The measured performance of the proposed 2nd-order ∑-Δ modulator was compared to two other designs as shown in Table I. Passive ∑-Δ modulators are not very commonly found in the literature, so comparisons are made to two active designs that are described as low power. Although the resolution is higher for these two designs, the power consumption of the proposed ∑-Δ modulator is the lowest of the three. While the FOM of the proposed design is worse, it is important to note that this design is implemented in a 500 nm process while the other designs are in 90 nm and 130 nm processes.

TABLE I. COMPARISON TO OTHER WORKS

Parameter	Proposed 2nd-Order SC ∑-Δ Modulator (this work)	2nd-Order SC ∑-Δ Modulator in [4]	3rd-Order SC ∑-Δ Modulator in [5]
Process	500 nm	90 nm	130 nm
Resolution (ENOB)	9.3 bits	10.48 bits	12.3 bits
Signal Bandwidth	3 kHz	10 kHz	20 kHz
Clock Frequency	1.024 MHz	1.28 MHz	3.2 MHz
Power Consumption	6.75 µW @ 2.5 V	17.14 µW @ 1 V	63 µW @ 0.4 V
FOM	1.78 pJ/step	0.60 pJ/step	0.31 pJ/step

V. CONCLUSION

The ∑-Δ modulator proposed in this paper offers good resolution suitable for a nominal 10-bit ADC while consuming less than 10 µW of power for a typical range of clock frequencies. The presented circuit should find use in a wide variety of applications where limiting power consumption is the highest priority. Furthermore, the implementation in a 500-nm CMOS process allows IC designers restricted to older processes to further reduce power and remain competitive with newer CMOS processes. A suitable application for this ∑-Δ modulator is in battery-powered medical electronics since the C5 process on which it is implemented is qualified for medical use. The design presented should scale well to smaller processes and allow for even greater reduction in power consumption.

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