A Survey on Reversible Logic Gates

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***Abstract*—**These days energy loss is an important factor to be considered, so reversible logic gates are used due to low power consumption and less heat dissipation. Reversible logic gates have various applications in Nanotechnology, CMOS design, Optical computing, Digital signal processing etc. Main purposes of designing reversible logic gates are reduction in number of gates, Quantum cost, garbage output etc.

Keywords: *Reversible logic gates, Quantum cost, Reversible logic, QCA.*

I. INTRODUCTION

Reversibility: The Boolean function F(y1; y2,...ym) with multiple outputs of m boolean variables is called reversible if the number of outputs are equal to number of inputs. Reversibility in computing implies that information about the computational states should never be lost.

Reversible logic: It involves the use of reversible gates which have same number of inputs and outputs and they can be made to run in backward direction also. Each input in the circuit is associated with some energy. If a bit is lost that is number of bits at the output are less as compared to the inputs ,then energy associated with the corresponding bit is dissipated in the form of heat. Since in reversible circuits no bit loss is there hence ideally in reversible circuits no power dissipation occurs. But practically some power dissipation do occur, which is much lesser than the conventional logic.

Parameters related to reversible gates:

A) Garbage outputs: The number of outputs added to make an n input-k-output function reversible is called garbage. Whenever it is necessary to make equal number of inputs and outputs, additional inputs or outputs can be added.

Input + constant input = output + garbage.

B) Quantum cost: The cost of the circuit in terms of the cost of a primitive gate is called Quantum cost. It is calculated knowing the number of primitive reversible logic gates required to realize the circuit. Quantum cost of 1x1 reversible gate is zero and 2x2 reversible gate is 1.

C) Number of constant inputs: This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

II. BASIC REVERSIBLE LOGIC GATES

A) Feynman Gate: Figure 1 shows 2*2 Feynman gate .The input vector is I(A, B) and the output vector is O(P, Q). Since a fan-out isn't allowed in reversible logic, this gate is helpful for duplication of the desired outputs.

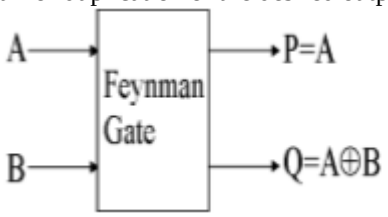

Fig.1: Symbol of Feynman gate

B) Double Feynman Gate (F2G): Figure 2 shows a 3*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R).

Fig.2: Symbol of Double Feynman gate

C) Fredkin Gate: Figure 3 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R).

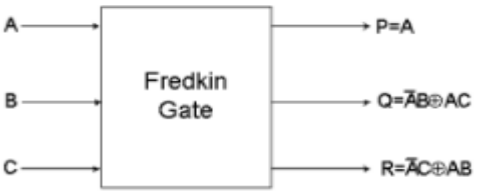

Fig.3: Symbol of Fredkin gate

D) Peres Gate: Figure 4 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R).

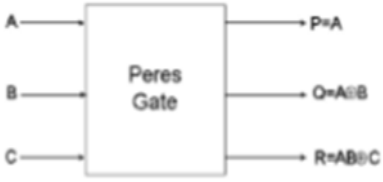

Fig.4: Symbol of Peres gate

E) Tofolli Gate: Figure 5 shows a 3*3 Tofolli gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R).

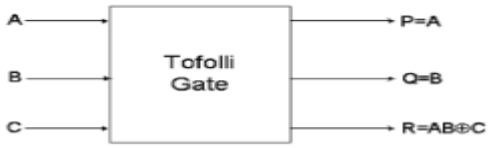

Fig.5: Symbol of Tofolli gate

III. Quantum-dot Cellular Automata (QCA)

A quantum-dot cellular automata is a finite state machine consisting of a finite or infinite grid of quantum-dot cells. A quantum-dot cell is a set of four quantum dots located at the corners of the cell and an electron pair. [6] By providing tunneling junctions with potential barriers, which are raised to prevent electron movement and lowered to permit electron movement, three states can occur. When barriers are low, the electrons can localize on any dot and the Null state occurs, but when the barrier is raised, the cell is polarized and the other two states can occur. These two states represent the logic "1" and "0".

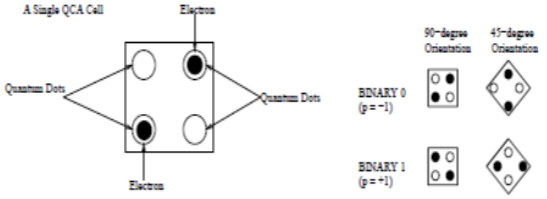

Fig.6: QCA Cells and Their Orientation

Clocking plays a key role in controlling the QCA logic functionality. In order to have active computation, signals pass through clocking zones, which represent areas where this computation is occurring. These clocking zones are a direct consequence of the QCA device physics. The clocking zones create the electric field which lowers and raises the potential barriers that allow the free electrons to tunnel or not. The clocking zones are physically adjacent, so the computation must proceed from one to the next in sequential order. As a particular clocking zone is performing a computation, the clocking zone before it must hold its outputs steady, and the clocking zone after it must perform no computation. Various reversible logic gates based on QCA can be shown as below:

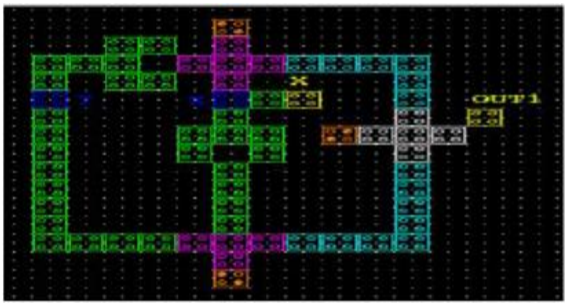

Fig.7: QCA based Feynman gate

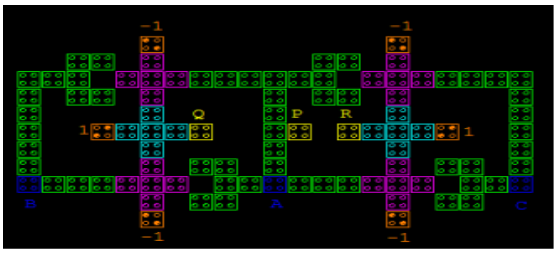

Fig.8: QCA based double Feynman gate

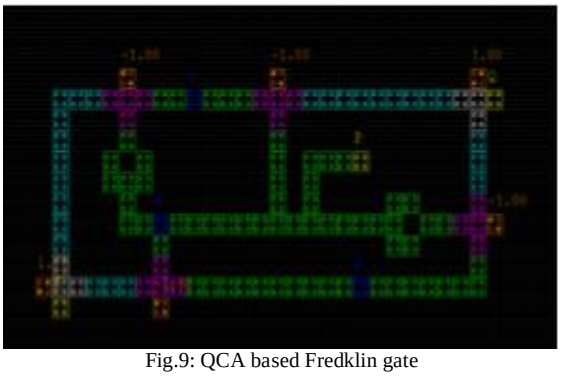

Fig.9: QCA based Fredklin gate

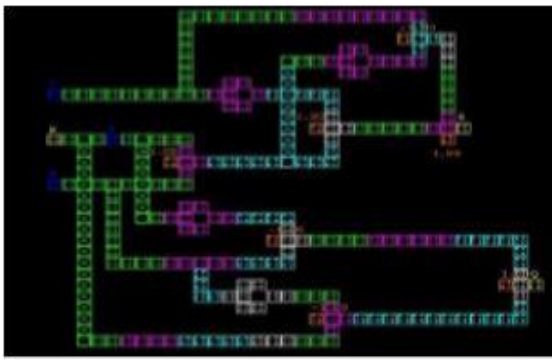

Fig.10: QCA based Peres gate

IV. LITERATURE SURVEY

In year 2008, Majid Mohammdi et.al presented that quantum gates are required to implement the binary reversible logic gates. Quantum gates V and V+ were represented in truth table forms. A new behavioural model to represent the V and V+ quantum gates was proposed. This model was used to simulate the quantum realization of reversible circuits. [1]

In year 2010, P. K. Lala et al proposed three types of adders, ripple carry, carry skip, and carry look-ahead, using a new reversible gate R. Results showed that the new gate results in more efficient adders in terms of gate count than those using the Fredkin gate. The number of reversible gates required was reduced from 5 to 4 using reversible gate R. [2]

In year 2010, Pijush Kanti Bhattacharjee proposed different logic gates like Majority Voter (MV), NOT, And-Or-Inverter (AOI), Nand-Nor-Inverter (NNI) etc. under QCA nanotechnology. A new method for realizing adder circuit in binary reversible logic was invented. A general equation for the minimum number of gates required to an

arbitrary number of input variables, causing synthesis of adder circuits, was achieved. It provided a significant reduction in hardware cost and switching delay compared to the other existing techniques. He also observed that the implementation of adder circuit design with QCA based AND-NAND and OR-NOR gates is more advantages than that of general logic gates design like AND, OR, NOT, EX-OR, CMOS etc. and QCA gates like MV, NOT, NNI etc. [3]

In year 2011, Prashant .R.Yelekar et al proposed a basic reversible gate to build more complicated circuits which can be implemented in ALU, some sequential circuits as well as in some combinational circuits. They also gave brief idea to build adder circuits using the basic reversible gate like peres gate and TSG gate. They have presented an approach to realize the multipurpose binary reversible gates. The proposed asynchronous designs have the applications in digital circuits like a Timer/Counter, building reversible ALU, reversible processor etc. [4]

In year 2012, Mr. Devendra Goyal presented VHDL CODE of all Reversible Logic Gate, which was used to design VHDL CODE of any sequential circuit. The VHDL codes made were simulated and synthesised in Xilinx software. [5]

In year 2013, S. Saravanan et al reviewed and implemented the basic gates in quantum cellular automata. Implementation was done in QCA Designer provided by University of British Columbia. They concluded that the system was drastically reduced in size and hence power consumption was decreased as per principle of low power VLSI design. The offset placement of cell gave a reduced output signal but signal was more precise and fine edged for layout where there was no offset between the cells that is cells were organized either horizontally or vertically.[6]

In year 2013, Arvind Kumar et al proposed a 2 to 4 decoder using fredkin gates. They reduced the power consumption of 4 to 16 decoder using reversible logic. By making use of fredkin gates in similar manner any n to 2n decoder can be designed. The software used for viewing RTL schematic of the decoder circuit was Xilinx ISE 8.2i. They worked on reduction of power consumption by using this technique as compared to conventional 4 to 16 decoder. The circuit used 15 constant inputs and four garbage outputs. [7]

In year 2014, Papiya Biswas et al proposed the basics of reversible logic gate and their implementation in Quantum cellular automata. They presented the primitive reversible gates such as Feynman Gate, Fredkin Gate, DKG Gate, MRG Gate etc. which were gathered from literature. This paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power cmos, nanotechnology, cryptography, optical computing, and DNA computing, digital signal processing (DSP), quantum dot cellular automata, and computer graphics. [8]

In year 2014, M.Amulya et al proposed the reversible logic synthesis for the n-to-2n decoder, where n is the fault tolerant Fredkin and Feynman double gates. They presented algorithm for designing the generalized decoder. In addition, several lower bounds on the number of constant inputs, garbage outputs and quantum cost of the reversible fault tolerant decoder were proposed. They proposed reversible fault tolerant decoder by using fault tolerant gates with constant inputs and quantum cost. The proposed fault tolerant decoder was showed correctly with the transistor implementation. [9]

In year 2014, K.V Manoj et al proposed a quantum price economical reversible full adder gate and Reversible Decoder. This gate worked on an individual basis as a reversible full adder &amplifier Decoder unit and needed just one clock cycle. They presented primitive gates such as Feynman Gate, Fredkin Gate, Double Feynman Gate, Peres Gate etc. [10]

In year2014, p.Vanusha et al proposed a novel 4*4 reversible gate named Peres Full Adder Gate (PFAG) , that is, it had 4-input lines and 4-output lines. The hardware complexity of this gate was less compared to the existing ones and it required only one clock cycle. The quantum cost of this gate was only 8. This paper led to implement some of the reversible logic gates and their applications. [11]

In year 2015, Sukhjeet Kaur et al proposed a design of Encoder using Feynman and Fredkin reversible logic gates. They explained various reversible logic gates and the important parameters. Various types of encoders were proposed and there simulation results were carried out in the Xilinx software. They calculated Quantum cost of different types of reversible encoders .Quantum cost of 4:2, 8:3 and 16:4 reversible encoder was 8,19 and 48 respectively. [12]

V. CONCLUSION AND FUTURE WORK

Various reversible logic gates have been introduced by various researchers as reversible computing has great significance in reducing complexity of digital circuits. In future, by using these gates we can design any of combinational or sequential circuit with numerous advantages over conventional gates such as, low power, low complexity, less delay, high speed etc.

VI. REFERENCES

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