100X, 100T Series
GaN Controller Module, Optional Leads
SMT, Non-Inverting (Negative Analog Input)

ACTUAL SIZE 

XSYSTOR

PRODUCT FLYER
August 2015

General Description

The 100 Series GaN Controller is a multi-functional circuit capable of operating and protecting all depletion -mode transistors. The non-inverting analog input accepts negative control voltage to produce negative gate bias voltage. It has universal features that allows 360° board placement with little or no line crossovers in the motherboard. A single power supply is enough for the 100 to provide dynamic control, but it will also accept negative power sources for current boost. Little or no filtering is needed in heavy RF environments. The 100 works seamlessly with 300 and 400 Series MOS switches that have compact footprints for locating near the transistor drain choke. Demonstrators and Kits containing combinations of Bias Controllers and MOS Switches are available for evaluation and fast prototyping.

Features

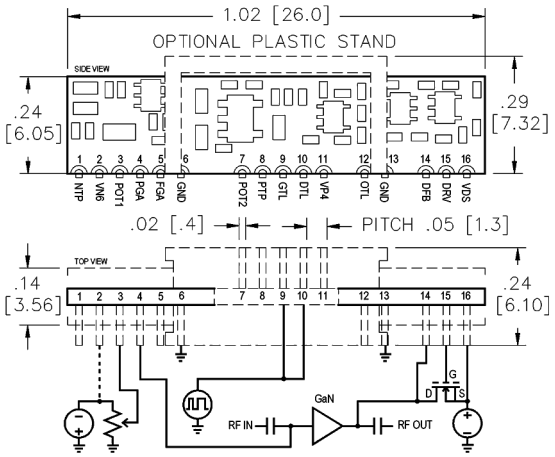
- Protects GaN devices from any Power ON/OFF sequence of internal and external supplies.
- Generates own Negative and Logic voltages from <80V supply OR accepts them for current boost.
- Gate Voltage Bias has Fixed Gate OR Pulsed Gate configuration.
- Drain-Gate switching features Master -Slave PWM OR Independent Control at gate or drain of device.
- Output drive to external MOSFET switching circuits comes in TTL OR Open Drain (<300mA).
- Temperature compensation is activated from either local OR remote temp sensor feedback.
- >25dB EMI/RFI Rejection at all I/O ports except from auxiliary taps.
- <500 nsec total delay from V_Logic to V_Drain with applicable switch.
- Optional pins, 0.05" [1.27 mm] pitch.
- Available in tape & reel.
- RoHS* Compliant

Specification Snapshot

Parameter	Min	Max
Supply (+) Voltage	+28 V	+80 V
Supply (-) Voltage	-6 V	0 V
Logic Voltage	-0.3 V	+4.0 V
Analog (-) Adjust Voltage	-6 V	0 V
Gate Bias Threshold Shutdown	-2.6 V	-1.4 V
Output Drive Voltage, Open Drain	0 V	+60 V
Output Drive Current, Open Drain		300 mA
Output ON Propagation Delay		120 ns
Output ON Fall Time, Active Low		120 ns
Output OFF Propagation Delay		80 ns
Output OFF Rise Time, Active Low		80 ns
Gate ON Propagation Delay		160 ns
Gate ON Rise Time		60 ns
Gate OFF Propagation Delay		160 ns
Gate OFF Fall Time		60 ns
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of TTL to 10% of Open Drain Output with pull-up resistor. Rise/ Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Typical Connection Diagram



PIN	LABEL	DESCRIPTION
1	NTP	Aux Negative Voltage Tap
2	VN6	Optional Neg (-) Supply
3	POT	Gate Voltage Input Adjust
4	PGA	Pulsed Gate Voltage Output
5	FGA	Fixed Gate Voltage Output
6	GND	Ground
7	POT	Connected to Pin 3
8	PTP	Aux Positive Voltage Tap
9	GTL	Gate Pulse Logic Enable
10	DTL	Drain Pulse Logic Enable
11	VP4	Optional Logic (+) Supply
12	OTL	Active-Low TTL MOS Driver
13	GND	Ground
14	DFB	MOS Drain Feedback
15	DRV	Open Drain MOS Driver
16	VDS	High Voltage Supply

Ordering Information

100X02R6 100T02R6 100X02R0 100T02R0 100X01R4 100T01R4	UNIVERSAL GaN CONTROLLER, NEGATIVE ANALOG INPUT, SINGLE DC (<80V) SUPPLY, VGS SHUTDOWN AT -2.6V, -2.0V, OR -1.4V. INDEPENDENT OR SEQUENTIAL SWITCHING OF DRAIN AND GATE
120X02R6 120T02R6	100 WITH NO GATE SWITCHING CAPABILITY
124X02R6 124T02R6	100 WITH NO GATE SWITCHING, NO INTERNAL NEGATIVE AND LOGIC (+5V) SUPPLIES

ADDITIONAL MODELS:
120X02R0, 120T02R0, 120X01R4, 120T01R4, 124X02R0, 124T02R0, 124X01R4, 124T01R4

X = STANDARD CONFIGURATION
T = OPT PINS AT 0.05" [1.3mm] PITCH

XSYSTOR INC.
18000 STUDEBAKER RD SUITE 700 MS 723
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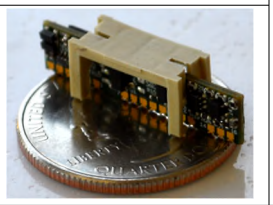
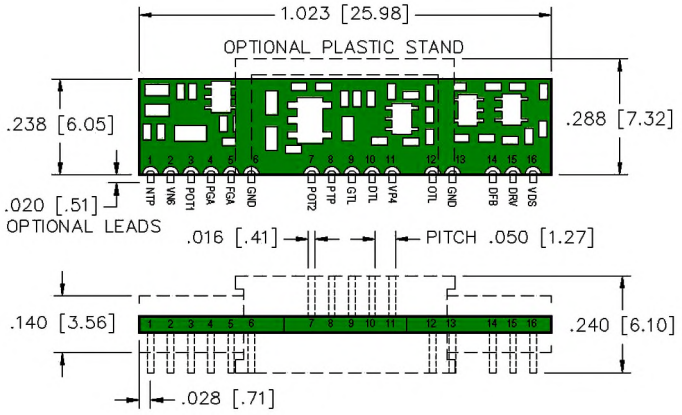
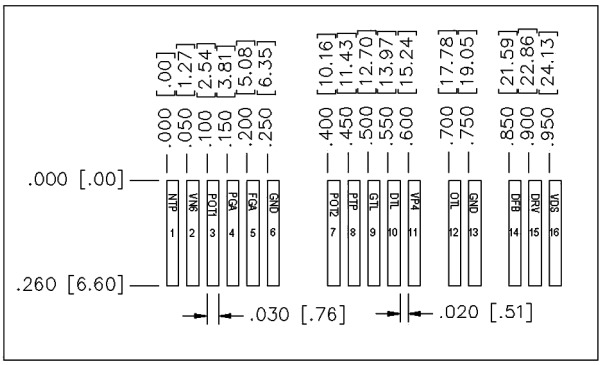


Outline & Land Pattern

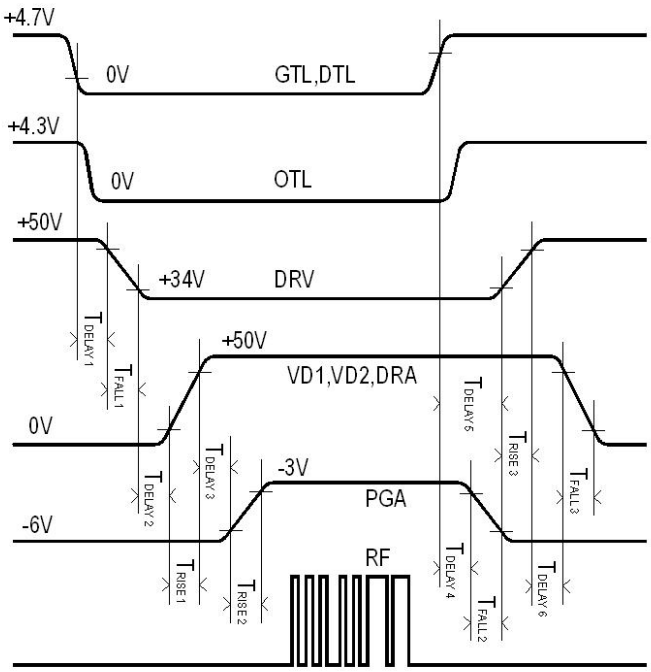




TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED

Typical Timing Diagrams

Refer to Application Note XAN-2 for further details.



Controller I/O Pin Descriptions

WARNING
—Do not connect Outputs together unless specified to do so.
—Do not ground unused Outputs. Leave open.
—Familiarize with the maximum rated voltages and currents.

NTP has –4.3V output from a voltage inverter. It is intended to be tapped if needed, by a >10KΩ potentiometer to establish the -Vgs input to the POT pin of the 100 series.

VN6 input is connected to the system negative supply of less than –6V. Although the 30mA output of the voltage inverter may suffice in most instances, an external supply is helpful for gate current boost of large GaN in saturation.

POT input receives negative voltage for the 100 series or positive voltage for the 200 series. Then the value is either inverted or not to approximately the same level reaching the transistor gate.

PGA output produces a square waveform triggered by TTL signal to pin GTL. It provides gate bias to GaN HEMT at a level set from POT pin and down to V_pinchoff established from the voltage inverter (-4.3V) or from pin VN6.

FGA output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.

PTP has +4.3V output from a voltage regulator. It is also intended to be tapped if needed, by a >10KΩ potentiometer to set operating voltage for POT pin of the 200 series.

GTL input is an independent, active-low TTL signal (<4.7V) that controls gate switching of the device. It is tied together with DTL pin for sequential pulse-width modulation at both gate and drain of the GaN. This is not used for sub-models.

DTL input is the primary logic enabler that controls the drain switching end of the transistor. When tied with GTL pin, the active-low TTL (<4.7V) switches the drain voltage ON first and would remain there until the gate voltage signal undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during Vdd ramping up & down.

VP4 input is connected to the system logic supply of ≤ 5V. If none is available, the internal voltage regulator kicks in unless the feature is not included in sub-models.

OTL output is an active-low TTL drive signal reserved for future switches with high/low-side drivers. Leave pin open.

DFB input monitors the presence of drain voltage when the MOS switch is ON. It is only used if gate switching is desired; otherwise, leave pin open for sub-models.

DRV output connects to the gate input of MOSFET switch module. The open drain port can handle up to 300mA, or be connected to multiple switching units.

VDS input receives up to +80V from the same supply that powers the GaN HEMT. This source generates negative and logic voltages internal to the 100 and 200 models.

Switch I/O Pin Descriptions

INP input connects directly to the Controller DRV output.

OUT is a low-side driver output which connects to MOSFET gates VG1 and VG2.

VG1, VG2, GAT are gate inputs that receive signals from DRV output of Controller. For a general purpose switch like the 410, the DRV pin can be tied to VG1 & VG2, while bypassing INP & OUT pins.

VD1, VD2, DRA are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.

VS1, VS2, SOU are source inputs that take up to +80V supply. Larger storage capacitance are attached here.

Model Number Color Code

0	1	2	3	4	5	6	7	8	9