What's Your PCB IQ?

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Quiz #3
Can you tell your PTH from a Hole in The Ground?

Take The Printed Circuit Girls and Geeks' 10-Question Pop Quiz on PTHs.

QUESTIONS

The term PTH is an abbreviation for:a. Plated Through Holeb. Pin Through Holec. Paste Through Holed. Partial Through Hole
e. None of the above
f. All of the above

2) The aspect ratio of a PTH is calculated as the ratio of hole's length to its diameter and is a measure of its manufacturability and reliability. What is the maximum acceptable mechanically drilled aspect ratio?
a. 5:1
b. 8:1
c. 10:1
d. 16:9
e. None of the above

3) The minimum copper plating thickness in a PTH should be:
a. 0.8 mils
b. 1.0 mils
c. 20 microns
d. 25 microns
e. none of the above

4) IPC classifies electronic products into three groups:

- Class 1 – General; meets minimum functionality requirements
- Class 2 – Dedicated service; long life and no downtime is desired
- Class 3 – High performance; mission-critical systems where downtime is not an option and the environment can be harsh

The latest revision of IPC workmanship standards, IPC-A-610-E or "Rev E" for short, calls out minimum vertical hole fill for Class 2 PTH solder joints as:
a. 75% on signal holes and 50% on ground holes
b. 75% on both signal and ground holes
c. 50% on both signal and ground holes
d. 75% on signal and the lesser of 50% or 1.9mm on ground holes

e. the lesser of 50% or 1.9mm on both signal and ground
f. none of the above

5) IPC 610-E stipulates what minimum vertical hole fill for Class 1 boards?
a. 75% on signal holes and 50% on ground holes
b. 75% on both signal and ground holes
c. 50% on both signal and ground holes
d. 75% on signal and the lesser of 50% or 1.9mm on ground holes
e. the lesser of 50% or 1.9mm on both signal and ground
f. none of the above

6) True or False: Getting PTHs to fill with solder is more difficult with Lead-free solders than tin-lead ones.

7) To help achieve acceptable hole fill with lead-free solders, ground planes should be:
a. Evenly distributed near the top and bottom layers of the PCB
b. Evenly distributed in the middle 50% of the PCB
c. Evenly distributed in the top 50% of PCB
d. Evenly distributed throughout the entire PCB stack up
e. Ground planes can be eliminated completely - they're really just design overkill

8) To help achieve acceptable hole fill with lead-free solders which of the following ground tie designs works best?
a. 1 spoke 0.030” wide
b. 4 spokes 0.005” wide
c. 4 spokes 0.010” wide
d. solid connection
e. none of the above

9) True or False: the copper in the barrel must dissolve into the solder to form a reliable joint.

10) The area of the PTH that gets affected first by excessive copper dissolution is:
a. The annular ring on the solder side
b. The knee on the solder side
c. The middle of the barrel
d. The annular ring on the top side of the board
e. None of the above

ANSWERS

1) A - Plated Through Hole. And if you got this one wrong, then you have just proven that you clearly cannot tell the difference. If you guessed B, Pin Through Hole, and want to argue that pins do in fact go in the holes, you are partially correct, but not all

holes are designed to accept pins. Ones that aren't are called vias; they are plated through holes that connect signals to different layers of the board. If you guessed C, Paste Through Hole, you are probably thinking of the intrusive reflow assembly process, which is also referred to as Pin-in-Paste (PIP) or Paste-in-Hole (not PIH – it's a bad acronym). The PIP process prints solder paste in the PTH before the pin is inserted. And finally, if you guessed Partial Through Hole, these also do exist. They're called blind or buried vias, and connect internal layers without going all the way through the PCB. Both are plated or metallized. Blind vias connect one external layer with one or more internal layers; buried vias connect internal layers only.

The only correct answer here is "A". It's too bad that there's no partial credit on this quiz. If you didn't answer "A" you got this question wrong.

2) C - 10:1. Holes with higher aspect ratios present two distinct problems: one in manufacturing and one in the field. In manufacturing, holes that have aspect ratios greater than 10:1 are difficult to properly drill and plate. In the field, thermal expansion causes them to crack, creating intermittent opens that are extremely difficult to find.

If 16:9 sounds familiar, that's because it's the aspect ratio of high definition television and modern computer monitors. If that was your guess, then you might want to consider spending a little less time reading the AV forum and a little more time reading the TechNet.

3) A and C...they're the same! 0.8 mils or 20 microns is the bare minimum you want to specify. If your PCB is thicker than 0.062" thick, and it is wave soldered using lead-free solders, you may want to spec 1 mil or 25 microns to guard against copper dissolution.

So score yourself a correct answer no matter what you guessed. That should compensate for the lack of partial credit on this month's easiest quiz question.

4) D - 75% on signal and the lesser of 50% or 1.9mm on ground holes. The new specification was released in April, 2010, and provides a bit of relief for thick PCBs that present difficulty getting minimum hole fill of 50% with lead-free solders. If you do the math, 1.9mm does not affect basic PCBs in the 0.062" to 0.135" range. Where it does buy some relief is on the really thick PCBs – since 1.9mm is roughly 75mils, it means that any PCB that's over 0.150" thick now has a new minimum fill requirement, if it is class 2 and connected to a ground plane.
Class 3 assemblies still require a minimum of 75% hole fill for all holes, regardless of their internal connections.

5) F - None of the above. This is a trick question! There is no stipulation on vertical fill for Class 1 PCBs because most are single sided and therefore do not have PTHs to fill. The workmanship standard for these holes is a 270 degree circumferential fillet on the solder side of the board.

6) True. Lead-free solder alloys wet more slowly than tin-lead ones, so it takes longer to wick up the barrel of the hole. To make mattes worse, the lead-free solders are processed at temperatures much closer to their solidification point than tin-lead, so they often freeze before reaching the top of the hole, especially when the hot solder passes an internal ground plane that robs the heat from it.

A 2008 study published by Celestica's Craig Hamilton showed that it is actually more difficult to meet class 2 hole fill requirements with lead-free solders than it is to meet class 3 hole fill requirements with tin-lead solder. The study was aimed at understanding PCB and solder pallet design requirements, and examined hole fill as a function of clearance around the perimeter of the connector (pad-to-pad spacing). Look at the SnPb Class 3 and Pb-Free Class 2 columns in the chart below. It is always easier to reach Class 3 hole fill with tin-lead than Class 2 with lead-free. While more clearance helps lower the defect rates (shown in dpmo), it is always easier to meet 75% vertical fill with tin-lead than 50% vertical fill with lead-free.By a long shot.

Pad-to-Pad Spacing	SnPb Class 2	SnPb Class 3	Pb-Free Class 2	Pb-Free Class 3
0.250	0	0	181	7623
0.200	0	0	2722	14338
0.150	0	1451	8711	36842
0.100	181	5989	11797	49002
0.050	4174	15245	21779	66062

Source: Hamilton, C., et al [1]

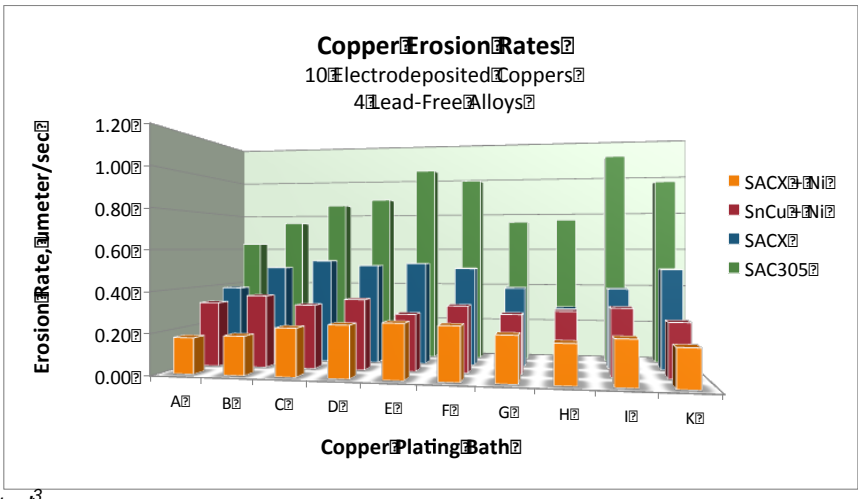
7) D - Evenly distributed throughout the entire stackup. Another study published by Hamilton in 2010[2](this is one smart dude) suggests “moderate connection to internal copper is in fact helpful in transferring heat into the barrels.” Where’s the worst place to locate ground planes? Smack in the middle of the stackup. That’s where they’ll get the least amount of preheat and are most likely to stop the wicking solder dead in its tracks.

8) A, B or C!The same 2010 study showed that ANY ground tie configuration EXCEPT SOLID can achieve acceptable hole fill. So designers, please take note: *Assemblers need relief!* Without thermal relief, the PCB has to spend so much time in the wave that it runs the risk of copper dissolution.

9) True – the copper must dissolve. The copper-tin intermetallic compound that is formed during soldering is the "glue" that holds the two dissimilar metals together. A solder joint is not considered reliable unless a thin layer of intermetallics is present. So some dissolution of the copper is required to form a good solder joint.

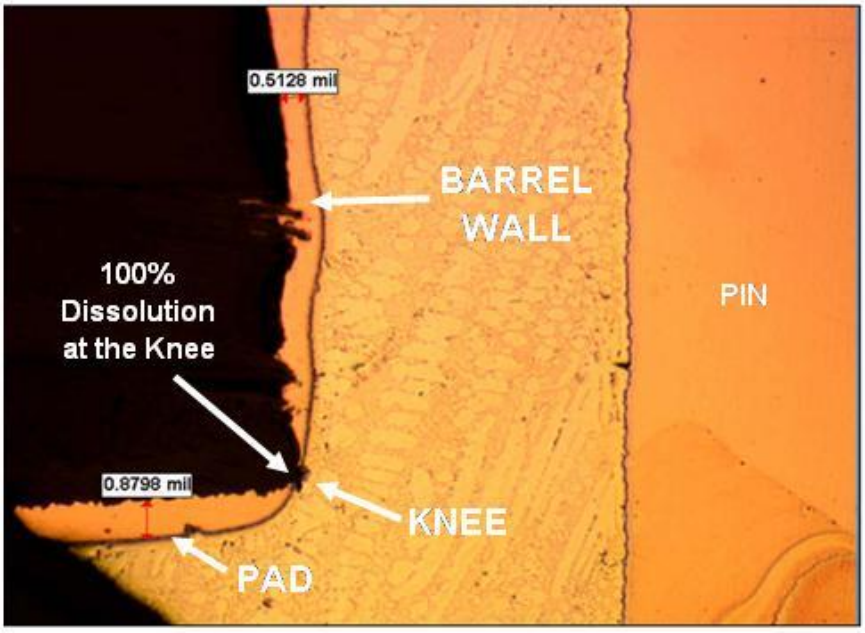
The troubles begin when too much copper is dissolved and reliability is threatened. Lead-free solder alloys dissolve copper much more quickly than tin-lead, and the ones with higher silver and lower nickel contents are particularly notorious for this

phenomena. And here's a special kicker, just to make the problem more difficult and mysterious - different copper platings from different baths dissolve at different rates, and we still don't know why! The chart below is from a 2008 study of ten different plating baths, and they all dissolved at different rates.



Source: Shea, et al[3]

10) B – The knee. The part of the barrel where the wall meets the pad at 90° is called the knee of the joint, and it is the most susceptible to copper dissolution, as shown in the photo.



Source: Hamilton, C, et al[4]

There is currently no specification on the minimum thickness of the remaining copper because

1) Excessive dissolution was never really considered an issue until lead-free solder hit the scene in the mid-2000s.

2) Nobody has published any studies that characterize exactly how much damage you can to do to a PTH while soldering it and still prove its long-term reliability. They're too busy focusing their efforts on *preventing* the damage.

This photo was published by (you guessed it!) Hamilton in 2006.In a 2009 publication[5], he showed cracks propagating through the thinned knee area, resulting in an open connection, and offers the following design guideline: **whenever possible, do not route traces on the bottom layer.**This makes the design robust against dissolution: if there are no connections to break, then there are no concerns about breaking them.

While the PCB Girls & Geeks might not be experts on everything, we sure know where to locate the experts for our readers.

SCORING

If you've been taking the PCB fab quizzes regularly, you know the "drill" on scoring: *add one point for every right answer; subtract one point for every wrong answer.*

How did you score?Let's compare your level of knowledge with hole fill based on IPC classifications:

6-10: Class 3 - Just like the highest reliability and performance classification provided by our standards, you are well grounded, full of knowledge, and can be expected to hold up even in high stress environments. We'll trust you to design our aircraft and under hood electronics any time.

3-5: Class 2-Your knowledge level is basically good enough for every day use, and should hold up just fine in environments that don't apply too much stress. I think you had better stick with desktop computers and gaming systems for now. But you show promise; keep taking the PCB quizzes, and soon you'll be "classed up" to a level 3.

0-2: Class 1 -The depth of your knowledge is extremely shallow, just like the solder on a single-sided PCB. Further more, you are not well connected, and your knowledge is as flimsyas paper-phenolic composite - a single drop test and you're toast. For now, you should probably keep to designing kids' toys and cheap universal remote controls for fear of shifting the curve on Taguchi's loss function. But keep reading the quizzes, because Rome wasn't built in a day, and there is still hope for you - at least your score wasn't a negative number.

If you scored a negative number, oryou're "in the hole," then you are what we refer to as an *unsupported* hole, but you can just go by U-hole, for short. FYI, an unsupported hole is one that's not plated through (since you did manage to get more answers wrong than right, we felt the definition was necessary for you to fully comprehend the insult). It will probably take at least a year of PCB quizzes just to get you "out of the hole."

Regardless of your score on this quiz, **you will be a hero** to your product managers and assemblers if you design your PTHs with the proper thermal relief and ground plane locations. Trust us – we're Geeks.

References:

1) *Hamilton, C., et al, "Selective Soldering DOE to Develop DFM Guidelines for Lead and Lead-Free Assemblies," Proceedings of SMTA International, 2008.*

2) *Hamilton, C., et al, "High Complexity Lead-Free Wave and Rework: The Effects of Material, Process and Board Design on Barrel Fill" Proceedings of SMTA International, 2010.*

3) *Shea, C., et al,"The influence of the PCB Fabrication Electrodeposition Process on Copper Erosion During Wave Soldering, Second Report, 4 Lead-Free Alloys," Proceedings of SMTA International, 2008.*

4) *Hamilton, C., et al,"A Study of Copper Dissolution in During PTH Rework Using a Thermally Massive Test Vehicle,"Proceedings of SMTA International, 2006*

5) *Hamilton, C., et al, "Reliability Assessment of Alternative Lead-Free Alloys Used During Wave and Rework," Proceedings of the Pan Pacific Microelectronics Symposium, 2009.*