4-Mbit (1M x 4) Static RAM

Part Number: DPA71046DV3302A

The DPA71046D02A is a high-performance CMOS static RAM organized as 1M words by 4 bits.

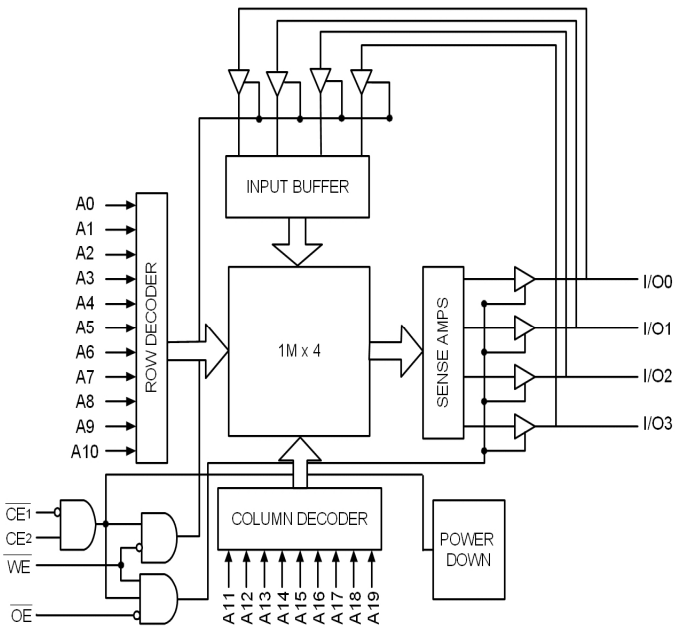
Writing to the device is accomplished by enabling the chip (by taking $\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW.

Reading from the device is accomplished by enabling the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) as well as forcing the Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH.

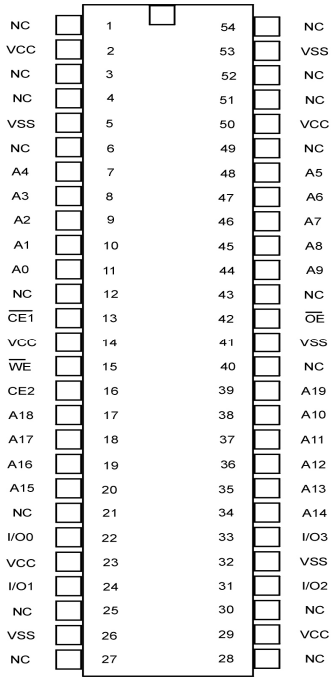
The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

- **-55˚ to +125˚ operating temperature**
- **High speed**
  - **t_{AA} = 12 ns**
- **Low active power**
  - **I_{CC} = 90 mA @ 12 ns**
- **Low CMOS standby power**
  - **I_{SB2} = 10 mA**
- **2.0 V data retention**
- **Supply voltage**
  - **3.3 V dc**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$ and CE_2 features**
- **54-pin SO ceramic flatpack, same footprint as 54-pin TSOP II**
- **Custom packaging is available**
- **This product uses Cypress CY7C1046DV33 die and is tested to meet military and space operational environment requirements**

Logic Block Diagram



Pin Configuration



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