Influence of annealing temperature on electrical properties of PbSe/n-Si heterojunction devices

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Abstract - In the present work, p-PbSe thin films were prepared by using thermal evaporation technique at room temperature on n-type silicon substrate under vacuum of $10^{-6}$ mbar. Thickness of the film is 600 nm. The fabricated devices were subjected to post-deposition annealing at (303, 333, 363 and 393) K and 45 min. The effect of annealing temperature on the electrical properties of PbSe/n-Si junctions was studied. The electrical properties included the capacitance-voltage (C-V) and current-voltage (I-V) measurements. C-V characteristics suggest that the fabricated devices were abrupt type. The built in potential ($V_{bi}$) was determined by extrapolation from $1/C^2$-V curve to the point (V=0). It was equal to (0.7V) at room temperature and was calculated under different annealing temperatures, while from I-V measurements, the ideality factor ($\beta$) is calculated.

خليفة
في هذا البحث، حضرت أغشية رقيقة من p-PbSe بطريقة التبخير الحراري في الفراغ في درجة حرارة الغرفة تحت ضغط 10^{-6} مل بار. سمك الغشاء بحدود 600 nm. درس تأثير درجات حرارة التلدين (303, 333, 363 and 393) K على الخصائص الكهربائية للمفرق الالتحادي PbSe/n-Si الكهربائي للمفرق الالتحادي التي شملت خصائص سعة فولتية ($C$) والخصائص تيار-فولتية ($I-V$). ومن قياس ($C-V$) والحال وتم حساب جهد البناء الداخلي ($V_{bi}$) من خلال اخذ امتتاد $1/C^2$-V إلى النقطة (V=0) حيث بلغ ($V_{bi}$) عند درجة حرارة الغرفة، وتم حسابه تحت درجات حرارة تلدين مختلفة، بينما تم حساب عامل المثلثية ($\beta$) من قياسات تيار-فولتية.

Index Terms—Lead selenide; electrical properties; Vacuum deposition; photocurrent.
I. INTRODUCTION

Metal chalcogenide compounds, having a semiconductor nature, are of considerable technical interest in the field of electronics and electro-optical devices. Intensive research has been performed in the past to study the fabrication and characterization of these compounds in the form of thin films. Thus, the interest for Lead Selenide (PbSe) semi conducting thin films is motivated by its application in solar cell technology, IR detectors, photographic plates, lenses and various optoelectronic devices [1-3]. Various methods employed for depositing PbSe thin films are electrochemical deposition, chemical bath deposition, molecular beam epitaxial growth method and vacuum evaporation method. Among the various methods, vacuum evaporation method is the most widely used technique for the deposition of metals, alloys and also many compounds. This involves the evaporation for sublimation of the material in vacuum by thermal energy and allowing the vapor stream of the charge to condense on a substrate so as to form a continuous and adherent deposit of a desired thickness [3-5].

PbSe is a polar semiconductor, which crystallizes in a face center cubic (f.c.c.) lattice of NaCl type. It is characterized by high dielectric susceptibility, high carrier mobility [6], and a narrow band gap (T=293K, PbSe) ~ 1.30 eV [7, 8]. Optical properties in the visible and infrared regions of spectra are related to the electron transitions. The asgrown films show p-type conduction [9, 10]. The aim of the present investigation is to report the electrical properties of heterojunctions of p-type PbSe deposited on n-type silicon substrate at different annealing temperatures.

II. THEORETICAL CONSIDERATIONS

There are different kinds of heterojunction formed between two semiconductors which have different values of energy gap, dielectric constant, electron affinity and work function as well as a difference in lattice constant and this is called lattice mismatch [11]. The capacitance-voltage (C-V) and current-voltage (I-V) are the electrical properties which characterize a heterojunction. These properties of a heterojunction depend strongly on the method of formation and the doping levels of the two semiconductors forming it.

A. The capacitance-voltage characteristics

C-V characteristics can be manipulated to yield a number of parameter such as: type of junction (abrupt or graded), built in potential (V_{bi}), carrier concentration and the width of the junction (depletion layer). The junction
capacitance per unit area of an abrupt anisotype heterojunction can be written as [11, 12]:

\[
\frac{C}{A} = \left[ \frac{e^2 N_n N_p}{2(e N_n + e N_p)} \right]^{1/2} (V_D - V)^{-1/2}
\]  

(1)

Where \( N_n \) and \( N_p \) are the donor and acceptor concentrations respectively, \( \varepsilon_n \) and \( \varepsilon_p \) are the dielectric constant of n and p-type semiconductor respectively, \( V_D \) is the built in potential, \( V \) is the applied voltage, and \( A \) is the area of the junction. The interception of the straight line with the voltage axis represents the built-in potential. The width of the junction can be calculated from the equation [13]:

\[
W = \frac{C_0}{C}
\]  

(2)

where \( C_0 \) is the capacitance at zero biasing voltage and

\[
\varepsilon_s = \frac{(\varepsilon_n \varepsilon_p)}{(\varepsilon_n + \varepsilon_p)}
\]  

(3)

where \( \varepsilon_s \) is the semiconductor permittivity for the two semiconductor materials and \( \varepsilon_n \) and \( \varepsilon_p \) are the dielectric constants of n-and p-type semiconductor, respectively.

B. The current-voltage characteristics

I-V characteristics are studied to explain the electrical properties, and are used to determine the built in junction potential and energy discontinuities in the conduction. These characteristics can be classified as forward or reverse bias. In the forward bias, there are two regions. At low voltage, the current varies exponentially suggesting conduction by thermionic emission. The current through the junction under low bias voltage (0-0.3 V) is given by the following relation [11, 14]:

\[
I = I_s [\exp(qV/\beta k T) - 1]
\]  

(4)

and
\[ I_s = A^*T^2 \exp\left(-q\varphi_b / k_B T\right) \]

(5)

Where \( q \) is the charge on electron, \( V \) is the applied voltage, \( \beta \) is the diode ideality factor, \( k_B \) is the Boltzmann constant, \( T \) is the temperature, \( \varphi_b \) is effective barrier height, \( A^* \) is effective Richardson constant and \( I_s \) is the reverse saturation current. At voltage above \( 0.3 \) V, a non-linear relation of current in junction is obtained and the current magnitude change very small with increasing of the applied bias voltage and this is called diffusion current, which is dominated in this region [15]. The reverse saturation current \( (I_s) \) is determined by interpolation of exponential slope of \( I \) at \( V=0 \). The ideality factor has been calculated using equation [11]:

\[ I_s = I_s \exp\left(qV / \beta k_B T\right) \]

(6)

where \( \beta \) is the ideality factor given by the following equation [15]:

\[ \beta = -q/k_B T \left[ \frac{V}{\ln(I_s)} \right] \]

(7)

II. EXPERIMENTAL PART

Thin films of PbSe having thickness around \((600) \) nm were deposited on n-type silicon \((111) \) by using vacuum coating unit type (Edward E306A). Square-shaped n-type silicon samples, each of \(1 \times 1 \) cm\(^2\) area, of \(1-3 \) \(\Omega\).cm resistivities were prepared using a wire-cut machine. The resistivity and type of conductivity of the silicon substrate were measured using Four-point probe (FPP) technique. The samples were etched with CP4 solution consisting of \((\text{HNO}_3, \text{CH}_3\text{COOH}, \text{HF})\) of ratios \((3:3:5)\) to remove oxides. They were then cleaned by alcohol and ultrasonic machine (Cerry PUL 125 device) for 15 minutes then they were cleaned by water and ultrasonic waves for another 15 minutes. First of all, the gadgets of the vacuum chamber were cleaned by acetone. A clean evaporation source–molybdenum boat–was fixed in the filament.
holder inside the chamber. The source to substrate distance was 15 cm. Stoichiometric PbSe powder having purity around 99.99% was kept in a molybdenum boat. The substrates were cleaned first by acetone. The chamber was evacuated at a pressure more than \(10^{-5}\) Torr by the combination of rotary and diffusion pump. When \(10^{-6}\) Torr vacuum was attained in vacuum chamber, the heater connected to the evaporation source was switched on which in turn slowly heated the source of PbSe to temperatures greater than the melting point. This allowed the evaporation of PbSe material. The thickness of the deposited films was obtained from light-beam Fizeau fringe method. After formation of PbSe film with thickness of 600 nm on silicon substrate the samples are transferred into annealing system using tube quartz furnace. The annealing process was carried out under vacuum pressure below \(10^{-4}\) Torr at conditions (303, 333, 363 and 393) K and 45 min annealing time. Ohmic contacts were fabricated by evaporating 99.999 purity aluminum wires for back and front contact through special mask using Edwards coating system. Measurements included current-voltage (I-V) characteristics in dark and under illumination by halogen lamp of p-PbSe/n-Si heterojunction are done using Keithly Digital Electrometer 616 and DC power supply. The C-V characteristics under reverse biasing at range (0.1-1.2) volt using LCR meter were measured to determine the type of heterojunction (abrupt or graded). The effect of annealing temperature on the electrical properties of the junction was investigated.

### IV. RESULTS AND DISCUSSION

#### A. Current-Voltage Measurements

The results of the current-voltage (I-V) measurements in the dark for PbSe/n-Si heterojunctions prepared at different annealing temperature are shown in fig. (1) (a). These characteristics are very important to describe the heterojunction performance and all heterojunction parameters depended on it. In the former curves, the I-V characteristics were given for samples in forward and reverse bias. In the left hand part, it is clear that the curve contains two
regions of reverse current; the first is the generation region where the reverse current is slightly increased with the applied voltage and this leads to generate electron-hole pairs at low bias. In the second region, a significant increase can be recognized as the reverse bias is increased. In this case, the current is resulted from the diffusion of minority carriers through the junction. We can also note from this figure the rapid increment in the reverse current at high reverse voltage, which is probably due to the leakage current arising from the surface layer [16]. The right hand part results in fig. (1) (a) give the I-V characteristic behavior of the PbSe/n-Si heterojunctions in the forward bias. Two regions are recognized; the first one represents recombination current, the first current is established when the concentration of the generated carrier is larger than the intrinsic carrier concentration \( n_i \), i.e. \( n*p>n_i^2 \), which leads to a recombination process for mass low applicable [17]. The second region at high voltage represents the diffusion or bending region which depends on serried resistance and inPbSe/n-Si heterojunctions represent the tunneling region. From the comparison of the results obtained for PbSe/n-Si prepared at different annealing temperatures, it is recognized that the values of the current improved for (PbSe/n-Si) at 393 K annealing temperature due to increasing the effectiveness of non-participating impurities before annealing, as well as defects annealing and reduce the value of resistivity for the junction. The ideality factor of PbSe/n-Si junctions was estimated at different annealing temperatures and found to be (2.1), (2.3), (1.8) and (1.6), respectively. These values refer to good rectification properties for all prepared junctions. Also we could recognize a significant enhancement in the junction quality with the increase in annealing temperature. The large value of \( \beta \ (>1) \) suggests that in this voltage region, the recombination in these devices occurs primarily in the junction depletion region and/or at the junction interface.

The increases in the current with the increase of annealing temperature will cause rearrangement of the interface atoms and reduce the dangling bond which leads to improving of the junction characteristics. This leads to the increase of the mobility and increase the photocurrent density [18]. Fig. (1) (b) gives J-V
Measurement for forward bias to calculate barrier height ($\Phi_B$) for PbSe/n-Si devices. Depending on the value of the J-V characteristics in the forward bias (fig.(1)) , the value of the saturation current has been obtained. The value of barrier height estimated ($\Phi_B$) for PbSe/n-Si devices has been found to be (0.945, 1.035, 1.087 and 1.111), respectively.

![Image](image.png)

**Fig.1. I-V characteristics of PbSe/n-Si heterojunction in dark at different annealing temperatures.**

**Inset on the right shows J-V characteristics.**

Fig. (2) (a, b, c and d) exhibits the photo electric behavior for PbSe/n-Si devices under illumination condition at different annealing temperatures. Under external reverse bias, depletion region of the device extends and as a result, more incident photons will contribute to the electron-hole pairs generation that takes place in the depletion region. The internal electric filed in the depletion
region causes the electron-hole pairs to separate from each other and this bias becomes large with the applied external bias. From the following figure, we can see the increase in the photo-current with the increasing of incident light intensity, where the large intensity refers to a great number of incident photons and hence, the separation electron-hole pairs increase. From this result, it is recognized that the enhancement in values of the photo current in PbSe/n-Si devices at different annealing temperatures with the same incident light intensity increase. This is due to the increment in the depletion layer width which means a large internal area for carrier separation. That leads to higher photo-current as shown in the following equation [19]:

\[
I_{ph} = q A G (W+L)
\]  

(8)

where A: is area, G: is generation rate, W: is the depletion width and L: is the diffusion length, therefore, when L becomes so short (\(<<W\)) due to the effect of mismatch defects, \(I_{ph}\) will depend essentially on W which in turn depends on bias voltage. Thus, \(I_{ph}\) will increase with increasing the bias voltage.
B. Capacitance-Voltage Measurements

The capacitance-voltage characteristics of PbSe thin films deposited at room temperature and effect of different thermal annealing were carried out.

The junction capacitance variation as a function of reverse bias voltage in the range of (0.1-1.2) volt for PbSe/n-Si heterojunction at different annealing temperatures is shown in fig. (3). this measurement was achieved in frequency (25 kHz). It is obvious that the measured capacitance is decreased with increasing the reverse bias voltage as it is expected from equation (1). The reduction was not linear, the reason is attributed to an increment of the depletion region width which causes an increase of built in potential.
Fig. 3. Junction capacitance as a function of applied voltage for PbSe/n-Si heterojunction at different annealing temperatures.

Additionally, it can be observed from this figure that the capacitance at zero bias voltage ($C_0$) decreases with the increasing of annealing temperatures up to (363, 393) K for prepared junctions and this is attributed to the decrease in the surface states which lead to an increase in the depletion layer and a decrease in the capacitance. In order to determine the type of the formed structure, from C-V measurements under reverse biasing condition the built in potential was determined, the inverse capacitance square ($1/C^2$) is plotted against applied reverse bias voltage for PbSe/n-Si heterojunction at different annealing temperatures as shown in fig. (4). the plots revealed a straight line relationship which means that the junction was of an abrupt type. The interception of the straight line with the voltage axis at ($1/C^2=0$), represents the built in potential [20].

The built in potential ($V_{bi}$), the width of the depletion layer (W) and the bulk Fermi level at different annealing temperatures are calculated and tabulated in the following Table (1). Also, it can observed from Table (1) that the built in potential increases with
increasing annealing temperature as a result of the decrease in the capacitance value and the increase of the depletion width.

![Image](image-url)

*Fig. 4. $1/C^2$ (C = Capacitance per unit area) as a function reverse bias voltage for PbSe/n-Si heterojunction at different annealing temperatures.*

<table>
<thead>
<tr>
<th>Annealing Temperature (K)</th>
<th>$V_{bi}$ (V)</th>
<th>$N_d$ (cm$^{-3}$)</th>
<th>$W$ (µm)</th>
<th>$C$ (nF/cm$^2$)</th>
<th>$E_c - E_f$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R.T</td>
<td>0.7</td>
<td>$1.5 \times 10^{15}$</td>
<td>0.71</td>
<td>12.4</td>
<td>0.245</td>
</tr>
<tr>
<td>333</td>
<td>0.8</td>
<td>$2.3 \times 10^{15}$</td>
<td>0.62</td>
<td>14.2</td>
<td>0.235</td>
</tr>
<tr>
<td>363</td>
<td>0.84</td>
<td>$1.4 \times 10^{15}$</td>
<td>0.81</td>
<td>10.9</td>
<td>0.247</td>
</tr>
<tr>
<td>393</td>
<td>0.86</td>
<td>$1.2 \times 10^{15}$</td>
<td>0.89</td>
<td>9.9</td>
<td>0.251</td>
</tr>
</tbody>
</table>

**CONCLUSION**

PbSe thin films were deposited on n-type silicon substrate at room temperature by using thermal evaporation technique under vacuum of $10^{-6}$ mbar. The thickness of the films was found to be 600 nm measured by light-beam Fizeau fringe method.
The effect of annealing temperature on the electrical properties of PbSe/n-Si junctions which included (C-V) characterization and (I-V) characterization under dark and illumination light were measured. The built in potential ($V_{bi}$) and the ideality factor ($\beta$) can be calculated from C-V and I-V measurements, respectively.

REFERENCES


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